Prashant J. Nair ***The University of British Columbia***

CONTACT

4014, 2332 Main Mall
University of British Columbia
Vancouver, BC Canada V6T 1Z4

✉ prashantnair@ece.ubc.ca
☞ https://prashantnair.bitbucket.io/

WORK EXPERIENCE

Assistant Professor: The University of British Columbia 2019-Present
Affiliate Fellow: Quantum Algorithms Institute 2022-Present

Post-Doctoral Researcher: IBM T.J. Watson Research Center 2017-2019
Future Memory Standards and Exascale Projects.

EDUCATION

Georgia Institute of Technology, Atlanta, Georgia USA
Ph.D., Electrical and Computer Engineering, May 2017

Georgia Institute of Technology, Atlanta, Georgia USA
M.S., Electrical and Computer Engineering, May 2013

University of Mumbai, Mumbai, India
B.Engg., Electronics Engineering, May 2009

RESEARCH INTERESTS

Memory systems, computer architecture, machine learning, security, reliability, sustainability, and quantum computing.

PUBLICATION SUMMARY

In computer architecture and systems, generally speaking, conferences are significantly more impactful than journals. The top conferences have an acceptance rate of <20%.

CONFERENCE PUBLICATIONS

C.1. "Heterogeneous Acceleration Pipeline for Recommendation System Training", *51st International Symposium on Computer Architecture* **(ISCA'24)**
Muhammad Adnan, Yassaman Ebrahimzadeh Maboud, Divya Mahajan, Prashant Nair

C.2. "Keyformer: KV Cache Reduction through Key Tokens Selection for Efficient Generative Inference", *7th Annual Conference on Machine Learning and Systems* **(MLSys'24)**
Muhammad Adnan, Akhil Arunkumar, Gaurav Jain, Prashant Nair, Ilya Soloveychik, Purushotham Kamath

C.3. "Red-QAOA: Efficient Variational Optimization through Circuit Reduction", *29th International Conference on Architectural Support for Programming Languages and Operating Systems* **(ASPLOS'24)**
Meng Wang, Bo Fang, Ang Li, and Prashant Nair

C.4. "FLuID: Mitigating Stragglers in Federated Learning using Invariant Dropout", *37th Conference on Neural Information Processing Systems* **(NeuRIPS'23)**
Irene Wang, Prashant Nair, and Divya Mahajan

C.5. "Structural Coding: A Low-Cost Scheme to Protect CNNs from Large-Granularity Memory Faults", *35th International Conference for High Performance Computing, Networking, Storage, and Analysis* **(SC'23)**
Ali Asgari Khoshouyeh, Florian Geissler, Syed Qutub, Michael Paulitsch, Prashant Nair, and Karthik Pattabiraman

C.6. "SparseFT: Sparsity-aware Fault Tolerance for Reliable CNN Inference on GPUs", *32nd International Conference on Parallel Architectures and Compilation Techniques* **(PACT'23)**

Gwangeun Byeon, Seungtae Lee, Seongwook Kim, Yongjun Kim, Prashant Nair, and Seokin Hong

C.7. "Scalable and Secure Row-Swap: Efficient and Safe Row Hammer Mitigation in Memory Systems", *29th International Symposium on High-Performance Computer Architecture* **(HPCA'23)** [Best Paper Award]
Jeonghyun Woo, Gururaj Saileshwar, and Prashant Nair *Acceptance rate: 25.2%*

C.8. "HuffDuff: Stealing Pruned DNNs from Sparse Accelerators", *28th International Conference on Architectural Support for Programming Languages and Operating Systems* **(ASPLOS'23)**
Dingqing Yang, Prashant Nair, and Mieszko Lis

C.9. "AQUA: Enabling Low-Overhead Mitigation of Row-Hammer at Ultra-Low Thresholds via Hybrid Tracking", *55th International Symposium on Microarchitecture* **(MICRO'22)**
Anish Saxena, Gururaj Saileshwar, Moinuddin K. Qureshi, and Prashant Nair
Acceptance rate: 23.8%

C.10. "Accelerating Recommendation System Training by Leveraging Popular Choices", *48th International Conference on Very Large Data Bases* **(VLDB'22)**
Muhammad Adnan, Yassaman Maboud, Divya Mahajan, and Prashant Nair

C.11. "Hydra: Enabling Low-Overhead Mitigation of Row-Hammer at Ultra-Low Thresholds via Hybrid Tracking", *49th International Symposium on Computer Architecture* **(ISCA'22)**
Moinuddin K. Qureshi, Aditya Rohan, Gururaj Saileshwar, and Prashant Nair
Acceptance rate: 16.7%

C.12. "Randomized Row-Swap: Mitigating Row Hammer by Breaking Spatial Correlation Between Aggressor and Victim Rows", *27th International Conference on Architectural Support for Programming Languages and Operating Systems* **(ASPLOS'22)**
Gururaj Saileshwar, Bolin Wang, Moinuddin K. Qureshi, and Prashant Nair
Acceptance rate: 20%

C.13. "SafeGuard: Reducing the Security Risk from Row-Hammer via Low-Cost Integrity Protection", *28th International Symposium on High-Performance Computer Architecture* **(HPCA'22)**
Ali Fakhrzadehgan, Yale N. Patt, Prashant Nair, and Moinuddin K. Qureshi
Acceptance rate: 30%

C.14. "A Case for Emerging Memories in DNN Accelerators", *24th Design, Automation and Test in Europe Conference and Exhibition* **(DATE'21)**
Avilash Mukherjee, Kumar Saurav, Prashant Nair, Sudip Shekhar, and Mieszko Lis
Acceptance rate: 24%

C.15. "ADAM: Adaptive Block Placement with Metadata Embedding for Hybrid Caches", *38th IEEE International Conference on Computer Design* **(ICCD'20)**
Beomjun Kim, Prashant Nair, and Seokin Hong *Acceptance rate: 28%*

C.16. "2DCC: Cache Compression in Two Dimensions", *23rd Design, Automation and Test in Europe Conference and Exhibition* **(DATE'20)**
Amin Ghasemazar, Mohammad Ewais, Prashant Nair, and Mieszko Lis
Acceptance rate: 26%

C.17. "Thesaurus: Efficient Cache Compression via Dynamic Clustering", *25th International Conference on Architectural Support for Programming Languages and Operating Systems* **(ASPLOS'20)**
Amin Ghasemazar, Prashant Nair, and Mieszko Lis *Acceptance rate: 18.1%*

C.18. "Touché: Towards Ideal and Efficient Cache Compression By Mitigating Tag Area Overheads", *52nd International Symposium on Microarchitecture* **(MICRO'19)**
Seokin Hong, Bulent Abali, Alper Buyuktosunoglu, Michael Healy, and Prashant Nair
Acceptance rate: 22.1%

C.19. "A Case for Multi-Programming Quantum Computers", *52nd International Symposium on Microarchitecture* **(MICRO'19)**
Paulomi Das, Swamit Tannu, Prashant Nair, and Moinuddin K. Qureshi
Acceptance rate: 22.1%

C.20. "SuDoku: Tolerating High-Rate of Transient Failures for Enabling Scalable STTRAM", *49th International Conference on Dependable Systems and Networks* **(DSN'19)**
Prashant Nair, Bahar Asgari, and Moinuddin K. Qureshi *Acceptance rate: 22.1%*

C.21. "Attaché: Towards Ideal Memory Compression by Mitigating Metadata Bandwidth Overheads", *51st International Symposium on Microarchitecture* **(MICRO'18)**
Seokin Hong^{+}, Prashant Nair^{+}, Bulent Abali, Alper Buyuktosunoglu, Kyu-Hyoun Kim, and Michael Healy *Acceptance rate: 21.3%*
$^{+}$ – both authors contributed equally.

C.22. "Morphable Counters: Enabling Compact Integrity Trees For Low-Overhead Secure Memories", *51st International Symposium on Microarchitecture* **(MICRO'18)**
Gururaj Saileshwar, Prashant Nair, Prakash Ramrakhyani, Wendy Elsasser, Jose A. Joao, Moinuddin K. Qureshi *Acceptance rate: 21.3%*

C.23. "SYNERGY: Architecting resilient memories through reliability and security co-design", *24th International Symposium on High-Performance Computer Architecture* **(HPCA'18)**
[MICRO Top-Picks 2019; Honorable Mention]
Gururaj Saileshwar, Prashant Nair, Prakash Ramrakhyani, Wendy Elsasser, Moinuddin Qureshi *Acceptance rate: 20.8%*

C.24. "Taming the Instruction Bandwidth of Quantum Computers via Hardware-Managed Error Correction", *50th International Symposium on Microarchitecture* **(MICRO'17)**
Swamit Tannu, Zachery Mayers, Prashant Nair, Douglas Carmean, Moinuddin Qureshi
Acceptance rate: 18.7%

C.25. "DICE: Compressing DRAM Cache for Bandwidth", *44th International Symposium on Computer Architecture* **(ISCA'17)**
Vinson Young, Prashant Nair, Moinuddin Qureshi *– Acceptance Rate: 19.6%*

C.26. "XED: Exposing On-Die Error Detection Information for Strong Memory Reliability", *43rd International Symposium on Computer Architecture* **(ISCA'16)**
[Partly incorporated into the HBM3 memory protocol]
Prashant Nair, Vilas Sridharan, Moinuddin Qureshi *– Acceptance Rate: 19.6%*

C.27. "Low-Cost Inter-Linked Subarrays (LISA): Enabling Fast Inter-Subarray Data Migration in DRAM", *22nd International Symposium on High-Performance Computer Architecture* **(HPCA'16)**
Kevin Chang, Prashant Nair, Saugata Ghose, Donghyuk Lee, Moin Qureshi, Onur Mutlu
– Acceptance Rate: 22%

C.28. "FAULTSIM: A Fast, Configurable Memory-Reliability Simulator for Conventional & 3D-Stacked Systems", *11th Conference of High-Performance Embedded Architectures and Compilers* **(HiPEAC'16, Invited Paper)**
Prashant Nair, David Roberts, Moinuddin Qureshi

C.29. "AVATAR: A Variable-Retention-Time (VRT) Aware Refresh for DRAM Systems", *45th Annual IEEE/IFIP International Conference on Dependable Systems and Networks* **(DSN'15)**

Moinuddin Qureshi, Dae-Hyun Kim, Samira Khan, Prashant Nair, Onur Mutlu – *Acceptance Rate: 21.8%*

C.30. "Reducing Refresh Power in Mobile Devices with Morphable ECC", *45th Annual IEEE/IFIP International Conference on Dependable Systems and Networks* **(DSN'15)**
Chia-Chen Chou, Prashant Nair, Moinuddin Qureshi – *Acceptance Rate: 21.8%*

C.31. "DEUCE: Write-Efficient Encryption for Secure Non-Volatile Memories", *20th International Conference on Architectural Support for Programming Languages and Operating Systems* **(ASPLOS'15)** [MICRO Top-Picks 2016; Honorable Mention]
Vinson Young, Prashant Nair, Moinuddin Qureshi – *Acceptance Rate: 16.7%*

C.32. "Reducing Read Latency of Phase Change Memory via Early Read and Turbo Read", *21st International Symposium on High-Performance Computer Architecture* **(HPCA'15)**
Prashant Nair, Chia-Chen Chou, Bipin Rajendran, Moinuddin Qureshi

C.33. "Citadel: Efficiently Protecting Stacked Memory from Large Granularity Failures", *47th International Symposium on Microarchitecture* **(MICRO'14)**
Prashant Nair, David Roberts, Moinuddin Qureshi – *Acceptance Rate: 19.4%*

C.34. "ArchShield: Architectural Framework for Assisting DRAM Scaling by Tolerating High Error-Rates", *40th International Symposium on Computer Architecture* **(ISCA'13)**
Prashant Nair, Dae-Hyun Kim, Moinuddin Qureshi – *Acceptance Rate: 19.4%*

C.35. "A Case for Refresh Pausing in DRAM Memory Systems", *19th International Symposium on High-Performance Computer Architecture* **(HPCA'13)**
Prashant Nair, Chia-Chen Chou, Moinuddin Qureshi – *Acceptance Rate: 20.5%*

JOURNALS

J.1. "The Dirty Secret of SSDs: Embodied Carbon", *ACM SIGEnergy Energy Informatics Review, October 2023*
Swamit Tannu and Prashant Nair

J.2. "Exploiting Data Compression for Adaptive Block Placement in Hybrid Caches", *Electronics, 2022*
Beomjun Kim, Yongtae Kim, Prashant Nair, and Seokin Hong

J.3. "FAULTSIM: A Fast, Configurable Memory-Reliability Simulator for Conventional and 3D-Stacked Systems", *ACM Transactions on Architecture and Code Optimization, 2015* **(TACO'15)**
Prashant Nair, David Roberts, Moinuddin Qureshi

J.4. "Citadel: Efficiently protecting stacked memory from TSV and large granularity failures", *ACM Transactions on Architecture and Code Optimization, 2015* **(TACO'15)**
Prashant Nair, David Roberts, Moinuddin Qureshi

J.5. "Architectural Support for Mitigating Row Hammering in DRAM Memories", *Computer Architecture Letters, 2015* **(CAL'15)**
Dae-Hyun Kim, Prashant Nair, Moinuddin Qureshi

J.6. "Refresh Pausing in DRAM Memory Systems", *ACM Transactions on Architecture and Code Optimization, 2014* **(TACO'14)**
Prashant Nair, Chia-Chen Chou, Moinuddin Qureshi

ARXIV PREPRINTS

A.1. "Ad-Rec: Advanced Feature Interactions to Address Covariate-Shifts in Recommendation Networks", *arXiv:2308.14902*
Muhammad Adnan, Yassaman Ebrahimzadeh Maboud, Divya Mahajan, and Prashant Nair

A.2. "MPGemmFI: A Fault Injection Technique for Mixed Precision GEMM in ML Applications", *arXiv:2311.05782*
Bo Fang, Xinyi Li, Harvey Dam, Cheng Tan, Siva Kumar Sastry Hari, Timothy Tsai, Ignacio Laguna, Dingwen Tao, Ganesh Gopalakrishnan, Prashant Nair, Kevin Barker, and Ang Li

A.3. "Heterogeneous Acceleration Pipeline for Recommendation System Training", *arXiv:2204.05436*
Muhammad Adnan, Yassaman Ebrahimzadeh Maboud, Divya Mahajan, and Prashant Nair

A.4. "TQSim: A Case for Reuse-Focused Tree-Based Quantum Circuit Simulation", *arXiv:2203.13892*
Meng Wang, Rui Huang, Swamit Tannu, and Prashant Nair

A.5. "The Dirty Secret of SSDs: Embodied Carbon", *arXiv:2207.10793*
Swamit Tannu and Prashant Nair

Workshop Publications

W.1. "Efficient QAOA Optimization using Directed Restarts and Graph Lookup", **Proceedings of the 2023 International Workshop on Quantum Classical Cooperative**,
Meng Wang, Bo Fang, Prashant Nair and Ang Li

W.2. "Enabling Scalable VQE Simulation on Leading HPC Systems ", **Proceedings of the SC '23 Workshops of The International Conference on High-Performance Computing, Network, Storage, and Analysis**,
Meng Wang, Fei Hua, Chenxu Liu, Nicholas Bauman, Karol Kowalski, Daniel Claudino, Travis Humble, Prashant Nair, and Ang Li

W.3. "Ad-Rec: Advanced Feature Interactions to Address Covariate-Shifts in Recommendation Networks", **MLSys Workshop at NeuRIPS'23**,
Muhammad Adnan, Yassaman Ebrahimzadeh Maboud, Divya Mahajan, and Prashant Nair

W.4. "A Case for Efficient and Scalable Tree-Based Quantum Circuit Simulator", **APS March Meeting**,
Meng Wang, Huang Rui, Swamit Tannu, and Prashant Nair

W.5. "The Dirty Secret of SSDs: Embodied Carbon", **HotCarbon 2022**,
Swamit Tannu and Prashant Nair

W.6. "MLMLP: A Case for Multi-Page Multi-Layer Perceptron Prefetcher", **MLArchSys 2021**,
Ali Asgari, Andrew Gunter, Mehdi Saeidi, Mieszko Lis, Prashant Nair
[Second place in the 2021 ML-Based Data Prefetching Competition]

W.7. "Accelerated Learning by Exploiting Popular Choices", **PeRSonAl @ MLSys 2021**,
Muhammad Adnan, Yassaman Ebrahimzadeh Maboud, Divya Mahajan, Prashant Nair

W.8. "FaultSim: A Fast, Configurable Memory-Resilience Simulator", **Memory Forum**, *held in conjunction with ISCA'14*
David Roberts and Prashant Nair

W.9. "Citadel: Efficiently Protecting Stacked Memory from Large Granularity Failures", **Memory Forum**, *held in conjunction with ISCA'14*
Prashant Nair, David Roberts, Moinuddin Qureshi

Grants

Note: It is relatively inexpensive to support a graduate student in Canada. Thus, the funding agencies also fund faculty members proportionately.

A faculty member needs **nearly 30K CAD** to support one graduate student at the University of British Columbia **for one year**. The grant amounts must be seen with this in mind.

1. **NSERC - Discovery Grant:** Architectural Techniques to Sustain Moore's Law to Enable Reliable, Secure, and Efficient Memory Systems – Sole PI, 28000 CAD/yr until 2024.
2. **NSERC - Discovery Grant Supplement:** Architectural Techniques to Sustain Moore's Law to Enable Reliable, Secure, and Efficient Memory Systems – Sole PI, 12500 CAD.
3. **DARPA RTML Grant:** An Optimized TensorFlow to RTML Compilation Flow Systems – Co-PI, 240,000 USD (overall) for 1.5 years.
4. **Intel Transformative Datacentre Grant:** Rethinking Architectures and Systems for Recommendation Systems – Co-PI, 540,000 CAD (overall) for 3 years.
5. **Mitigating SDCs in Datacentres:** A Gift from Meta – PI, 50,000 USD.
6. **Efficient Quantum Chemistry Simulators:** NRC Canada – PI, 143000 CAD.

COURSES TAUGHT

1. CPEN 211 (Introduction to Microcomputers)
   Fall 2022
2. CPEN 311 (Digital Design)
   Spring 2022, Fall 2023
3. CPEN 411 (Undergraduate-Level Computer Architecture)
   Fall 2019, Fall 2020, Fall 2021, Fall 2022, Fall 2023
4. CPEN 511 (Graduate-Level Computer Architecture)
   Spring 2024, Spring 2019, Spring 2020
5. EECE 571 (Graduate-Level Advanced Memory Systems)
   Spring 2021

CURRENT STUDENTS

Jeonghyun Woo – Ph.D. student

Meng Wang – Ph.D. student

Muhammad Adnan – Ph.D. student

Yassaman Ebrahimzadeh Maboud – Ph.D. student

Mushahid Khan – Ph.D. student (primary advisor Prof. Olivia Di Matteo)

GRADUATED STUDENTS

Dr. Amin Ghasemazar (primary advisor Prof. Mieszko Lis)

Bolin Wang – M.A.Sc.

Muhammad Adnan: M.A.Sc. continued to Ph.D.

Yassaman Ebrahimzadeh Maboud: M.A.Sc. continued to Ph.D.

Ali Asgari – M.A.Sc. (primary advisor Prof. Karthik Pattabiraman)

Muchen He – M.A.Sc. (primary advisor Prof. Mieszko Lis)

Irene Wang – B.A.Sc.

Impact and Achievements

- HBM3 memory currently employs ideas from the XED paper – ISCA-2016.
- HPCA 2023 Best Paper Award.
- MICRO Top-Picks 2019 (honorable mention).
- ECE Graduate Research Assistant Excellence Award: An Electrical and Computer Engineering award for a student for his/her outstanding accomplishments as a researcher during their Ph.D. at Georgia Institute of Technology.
- MICRO Top-Picks 2016 (honorable mention).
- Organized the first Memory Reliability Forum at HPCA-2016 (20+ participants).
- Finalist at the Qualcomm Innovation Fellowship-2014.
- Thank a Teacher Award: For being an exemplary TA during Fall 2012.

Tools and Resources

- FaultSim: Open-Sourced Fast and Accurate Memory-Reliability Simulator, with AMD Inc.
  Available at: https://github.com/Prashant-GTech/FaultSim-A-Memory-Reliability-Simulator
- The first Memory Reliability Forum: A tutorial delivered by leading experts in reliability to educate the community and highlight key research areas in memory-reliability
  Available at: http://www.prism.gatech.edu/~pnair6/tutorial

Talks

- "From Bits to Beyond: Crafting Secure and Scalable Memory Architectures for Next-Generation Systems", at the University of Pennsylvania in November 2023
- "From Bits to Beyond: Crafting Secure and Scalable Memory Architectures for Next-Generation Systems", at UT Austin in November 2023
- "From Bits to Beyond: Crafting Secure and Scalable Memory Architectures for Next-Generation Systems", at NYU in November 2023
- "From Bits to Beyond: Crafting Secure and Scalable Memory Architectures for Next-Generation Systems", at EPFL in October 2023
- "From Bits to Beyond: Crafting Secure and Scalable Memory Architectures for Next-Generation Systems", at d-matrix in October 2023
- "Scaling the Memory Wall: Towards Next Generation Architecture and Systems", at AMD in May 2023
- "Research in Academia and Industry!", *Keynote Speaker* at the uArch Workshop (co-held with ISCA 2022) in June 2022
- "Attaché: Towards Ideal Memory Compression by Mitigating Metadata Bandwidth Overheads", at the MICRO-51 in October 2018
- "DVoLT: Dynamic Voltage and Timing for Memory DIMMs", at IBM in Aug. 2016
- "XED: Exposing On-Die Error Detection Information for Strong Memory Reliability", during ISCA'16
- "XED: Exposing On-Die Error Detection Information for Strong Memory Reliability", at IBM in Aug. 2016

- ◇ "On Fault Simulators", Memory Reliability Forum (Organizer & Speaker) in HPCA'16
- ◇ "DMAT: Decoupling DRAM Mats for low-latency", at ArchiTech co-located with ASPLOS'16
- ◇ "Reducing Read Latency of Phase Change Memory via Early Read & Turbo Read", during HPCA'15
- ◇ "Citadel: Efficiently Protecting Stacked Memory from Large Granularity Failures", during MICRO'14
- ◇ "Citadel: Efficiently Protecting Stacked Memory from Large Granularity Failures", during Memory Forum in ISCA'14
- ◇ "FAULTSIM: A Fast, Configurable Memory-Resilience Simulator", during Memory Forum in ISCA'14
- ◇ "ArchShield: Architectural Framework for Assisting DRAM Scaling by Tolerating High Error-Rates", at AMD in Jun. 2013
- ◇ "A Case for Refresh Pausing in DRAM Memory Systems", during HPCA'13

ACADEMIC SERVICE

- ◇ **Program Committee Member**
  - International Symposium on Microarchitecture (MICRO) 2024
  - International Symposium on Computer Architecture (ISCA) 2024
  - International Symposium on Microarchitecture (MICRO) 2023
  - International Symposium on Computer Architecture (ISCA) 2023
  - International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2023
  - International Symposium on Microarchitecture (MICRO) 2022
  - International Conference for High Performance Computing, Networking, Storage, and Analysis (SC) 2022
  - IEEE Micro Special Issue on Top Picks from the 2021 Computer Architecture Conferences
  - International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2022
  - International Parallel and Distributed Processing Symposium (IPDPS) 2022
  - International Symposium on High-Performance Computer Architecture (HPCA) 2022
  - International Symposium on Microarchitecture (MICRO) 2021
  - International Symposium on Computer Architecture (ISCA) 2021
  - Annual Non-Volatile Memories Workshop 2021
  - IEEE Micro Special Issue on Top Picks from the 2020 Computer Architecture Conferences
  - International Symposium on Microarchitecture (MICRO) 2019
  - IEEE Transactions on Parallel and Distributed Systems
  - IEEE Computer Architecture Letters

- ACM Transactions on Architecture and Code Optimization
- ACM Transactions on Computers

◇ **External Review Committee Member:**

- International Symposium on High-Performance Computer Architecture (HPCA) 2024,
- International Symposium on High-Performance Computer Architecture (HPCA) 2023,
- International Symposium on Computer Architecture (ISCA) 2022,
- International Symposium on Computer Architecture (ISCA) 2020,
- International Symposium on High-Performance Computer Architecture (HPCA) 2018,
- International Symposium on Computer Architecture (ISCA) 2016

◇ **Invited Reviewer:** International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2016

◇ **Submission Chair:**

- International Symposium on Microarchitecture (MICRO) 2015
- IEEE Micro Special Issue on Top Picks from the 2016 Computer Architecture Conferences

◇ **Local-Area Co-Chair:** International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2023

◇ **Finance Chair:** 2024 IEEE International Symposium on Workload Characterization (IISWC)

◇ **Publication Chair:** 32nd IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems

◇ **Organizer:**

- Tutorial on training Big Tutorial Sparse Recommendation Models on Commodity Servers (Co-held with HPCA 2022)
- The Memory Reliability Forum Workshop (Co-held with HPCA 2016)

University Service

◇ Faculty Recruiting Committee Member: 2020-2021, 2023-2024

◇ Graduate Awards Committee Member: 2020-present.

◇ Ph.D. Committee Member (Chair)– For Dr. Ayub Gubran (graduated 2019).

◇ Ph.D. Qualifying Exam Committee Member – Deval Shah.

◇ Ph.D. Qualifying Exam Committee Member – Dingqing Yang.

◇ Ph.D. Qualifying Exam Committee Member – Mohammad Olyaiy.

◇ Ph.D. Qualifying Exam Committee Member – Joel Nider.

◇ Ph.D. Qualifying Exam Committee Member – Nihkil Ghanathe.

PATENTS

1. "Dynamic clustering-based data compression"
   UPSTO#: US11245415, Issued on 02/08/2022
   Inventors: Amin Ghasemazar, Prashant Nair, Mieszko Lis

2. "Employing single error correction and triple error detection to optimize bandwidth and resilience under multiple bit failures"
   UPSTO#: US11095313B2, Issued on 08/17/2021
   Inventors: Prashant Nair, Robert Montoye, Jeffrey Derby, Bruce Fleischer

3. "Systems, methods and computer program products using multi-tag storage for efficient data compression in caches"
   UPSTO#: US10831669B2, Issued on 11/10/2020
   Inventors: Prashant Nair, Seokin Hong, Alper Buyuktosunoglu, Michael B Healy, Bulent Abali

4. "Dynamic adjustments within memory systems"
   UPSTO#: 2019/0146864A, Issued on 5/16/2019
   Inventors: Prashant Nair, Alper Buyuktosunoglu, Pradip Bose

5. "Bandwidth efficient techniques for enabling tagged memories"
   UPSTO#: 10,423,538B2, Issued on 9/24/2019
   Inventors: Prashant Nair, Alper Buyuktosunoglu, Seokin Hong

6. "Enabling compression based on queue occupancy"
   UPSTO#: US20200183620A1, Issued on 11/06/2020
   Inventors: Prashant Nair, Seokin Hong, Michael Healy, Bulent Abali, Alper Buyuktosunoglu

7. "System and method for an error-aware runtime configurable memory hierarchy for improved energy efficiency"
   UPSTO#: US20200342284A1, Issued on 10/29/2020
   Inventors: Alper Buyuktosunoglu, Nandini Chandramoorthy, Prashant Nair, Karthik Swaminathan

8. "Error Detection and Correction Utilizing Locally Stored Parity Information"
   UPSTO#: 20160117221, Issued on 4/28/2016
   Inventors: Prashant Nair and David A. Roberts

9. "Completely Utilizing the Hamming Distance for SECDED based DIMMs"
   UPSTO#: 20160134307, Issued on 5/12/2016
   Inventors: Prashant Nair, Chaohong Hu and Hongzhong Zheng

10. "Memory Page Access Detection"
    UPSTO#: US20160231933, Issued on 8/14/2016
    Inventors: Gabriel H. Loh, David A. Roberts, Mitesh R. Meswani, Mark R. Nutter, John R. Slice, Prashant Nair and Michael Ignatowski

PROFESSIONAL MEMBERSHIPS

Senior Member IEEE, ACM