

Low-Cost Inter-Linked Subarrays (LISA)

Enabling Fast Inter-Subarray Data Movement in DRAM

Kevin Chang

Prashant Nair, Donghyuk Lee, Saugata Ghose,
Moinuddin Qureshi, and Onur Mutlu

SAFARI
CARET

Carnegie Mellon

**Georgia
Tech** 

Problem: Inefficient Bulk Data Movement

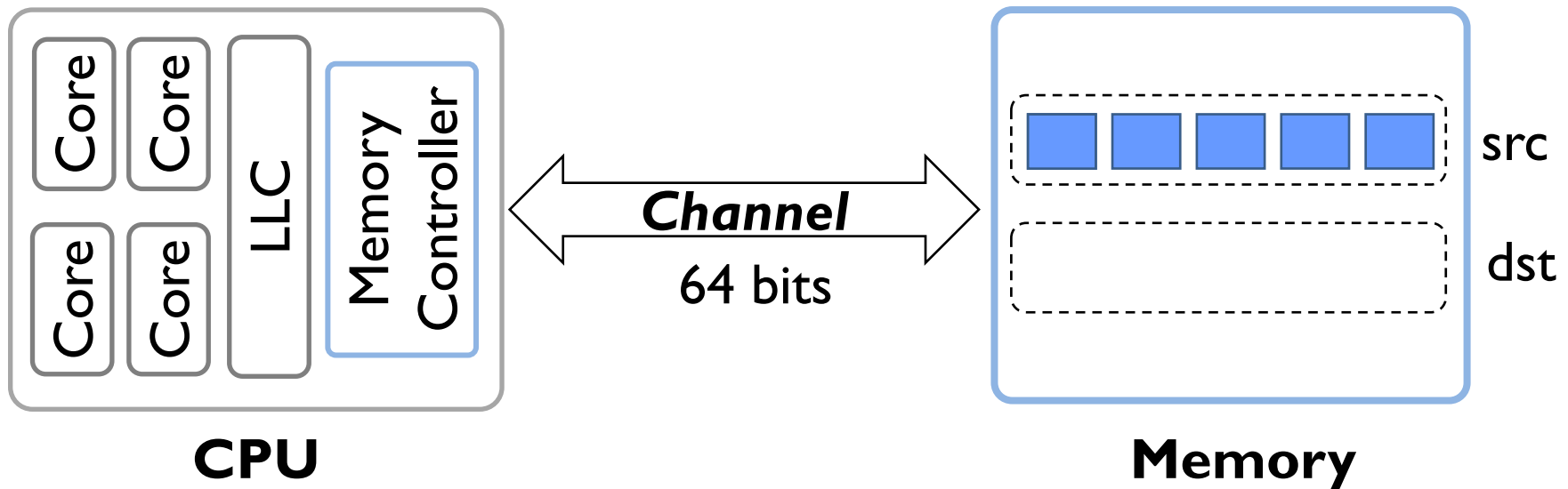
Bulk data movement is a key operation in many applications

– *memmove & memcpy: 5% cycles in Google's datacenter [Kanev+ ISCA'15]*

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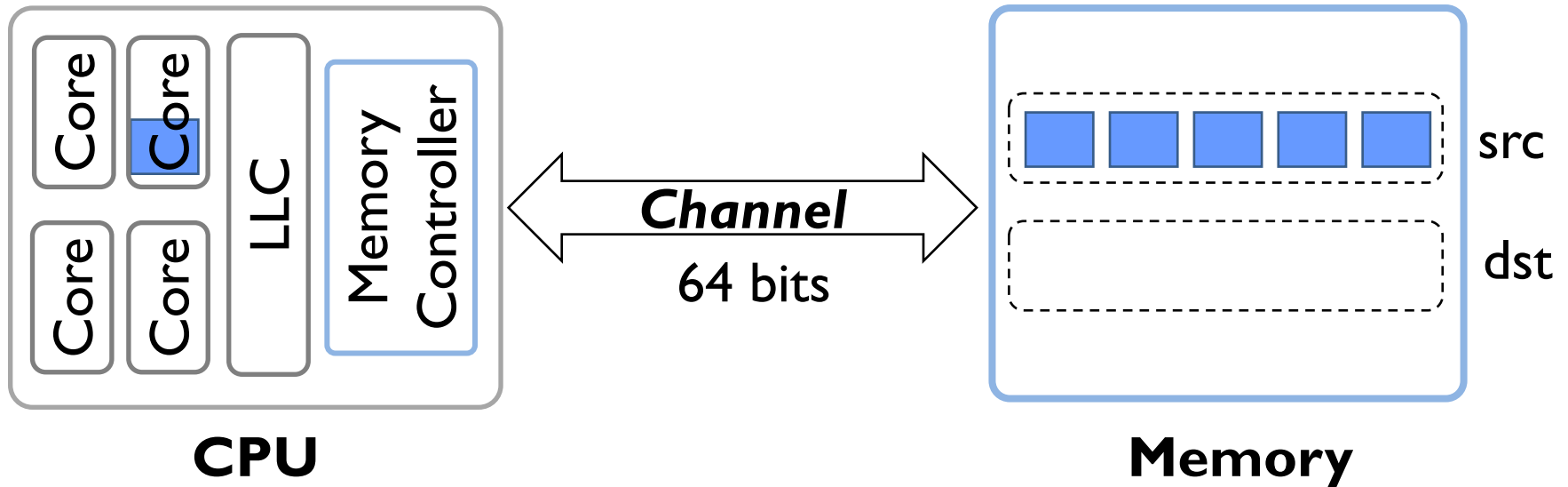
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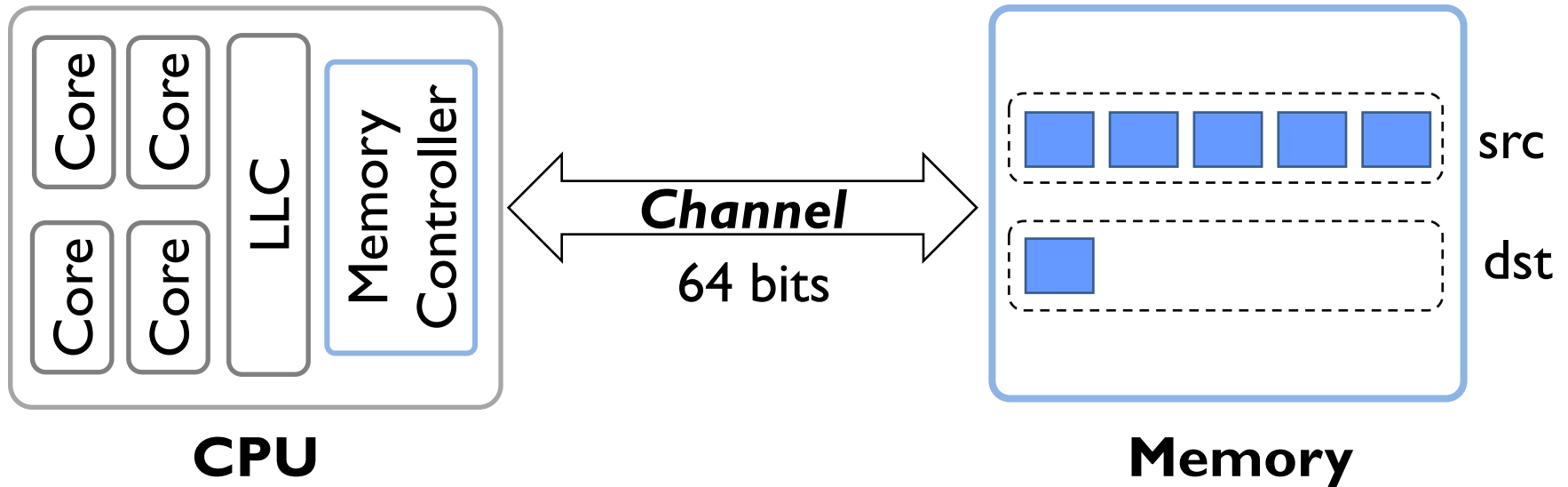
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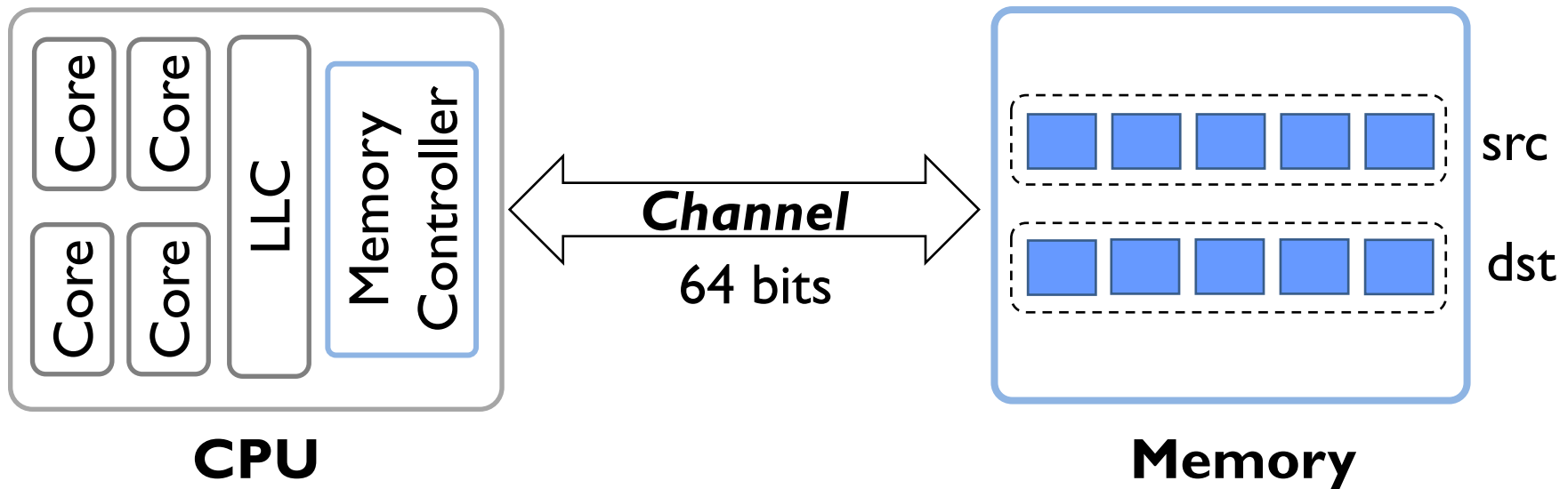
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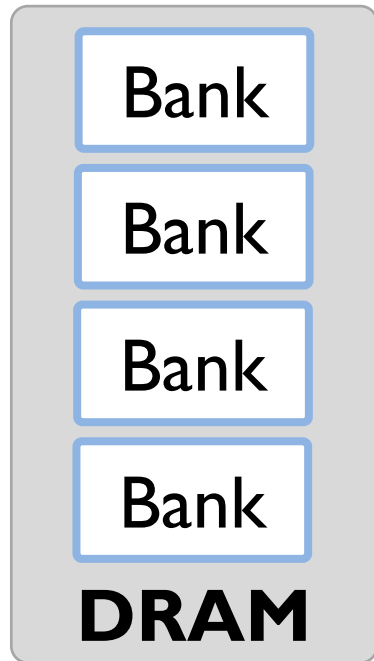
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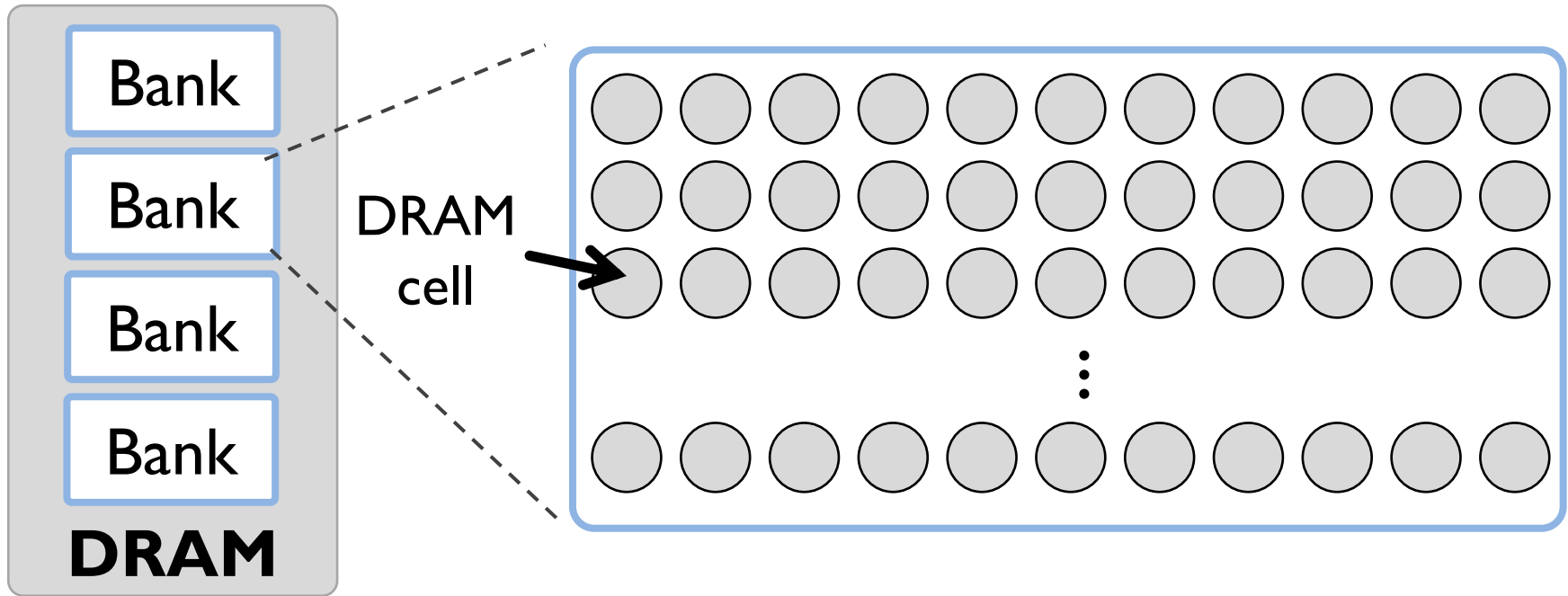
Long latency and high energy

Moving Data Inside DRAM?

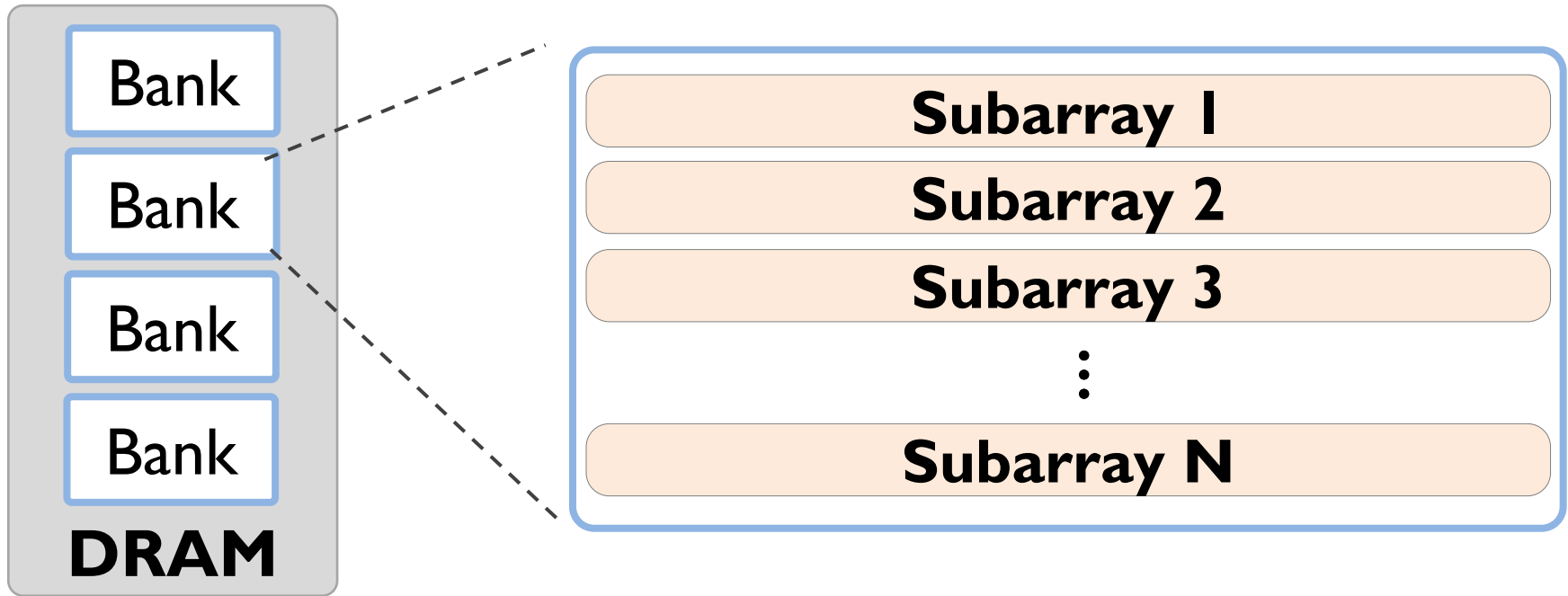
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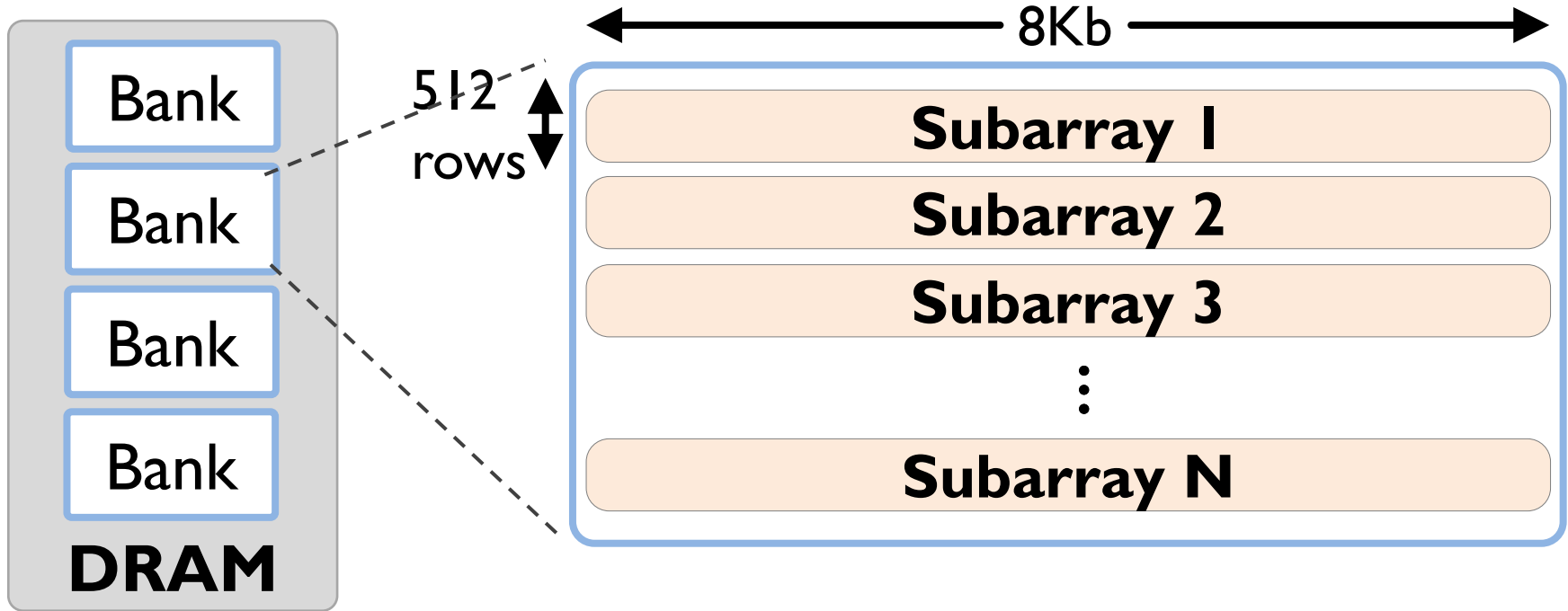
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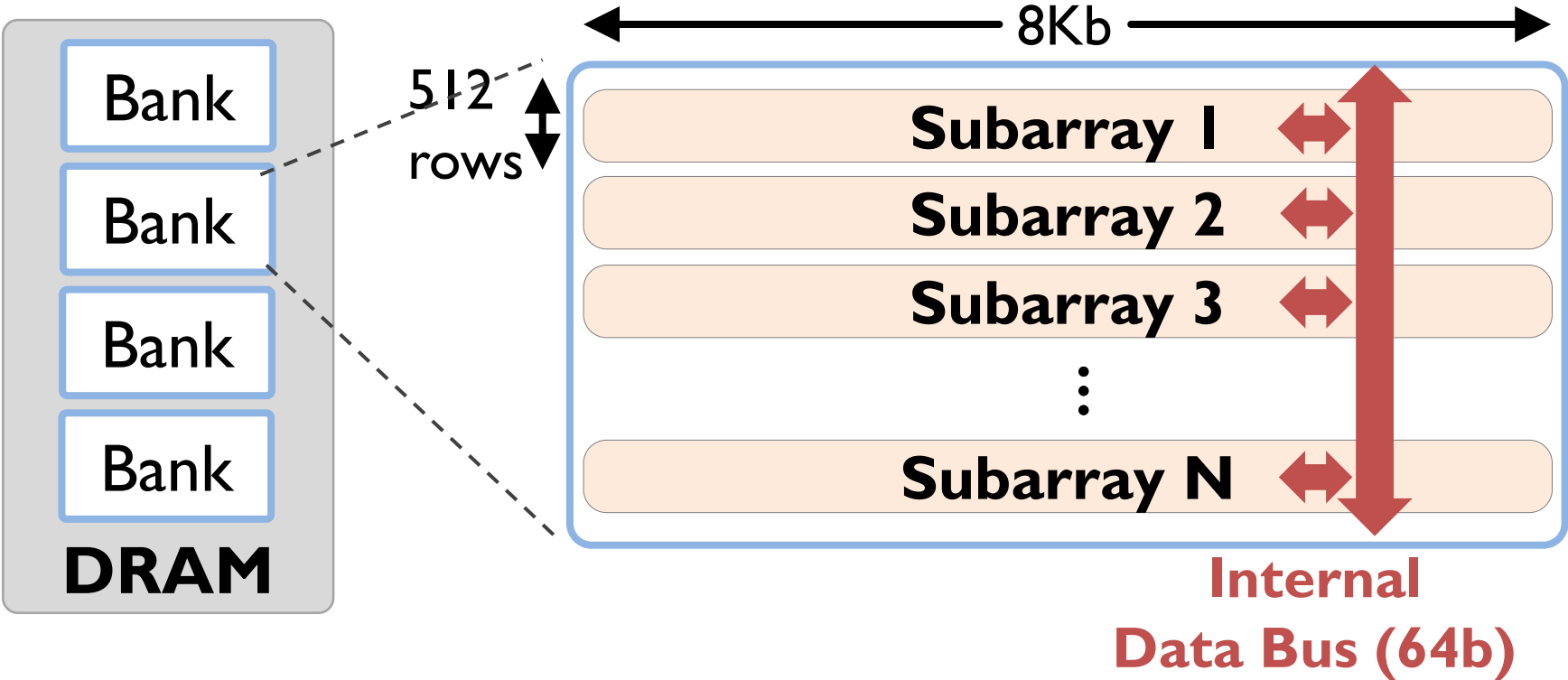
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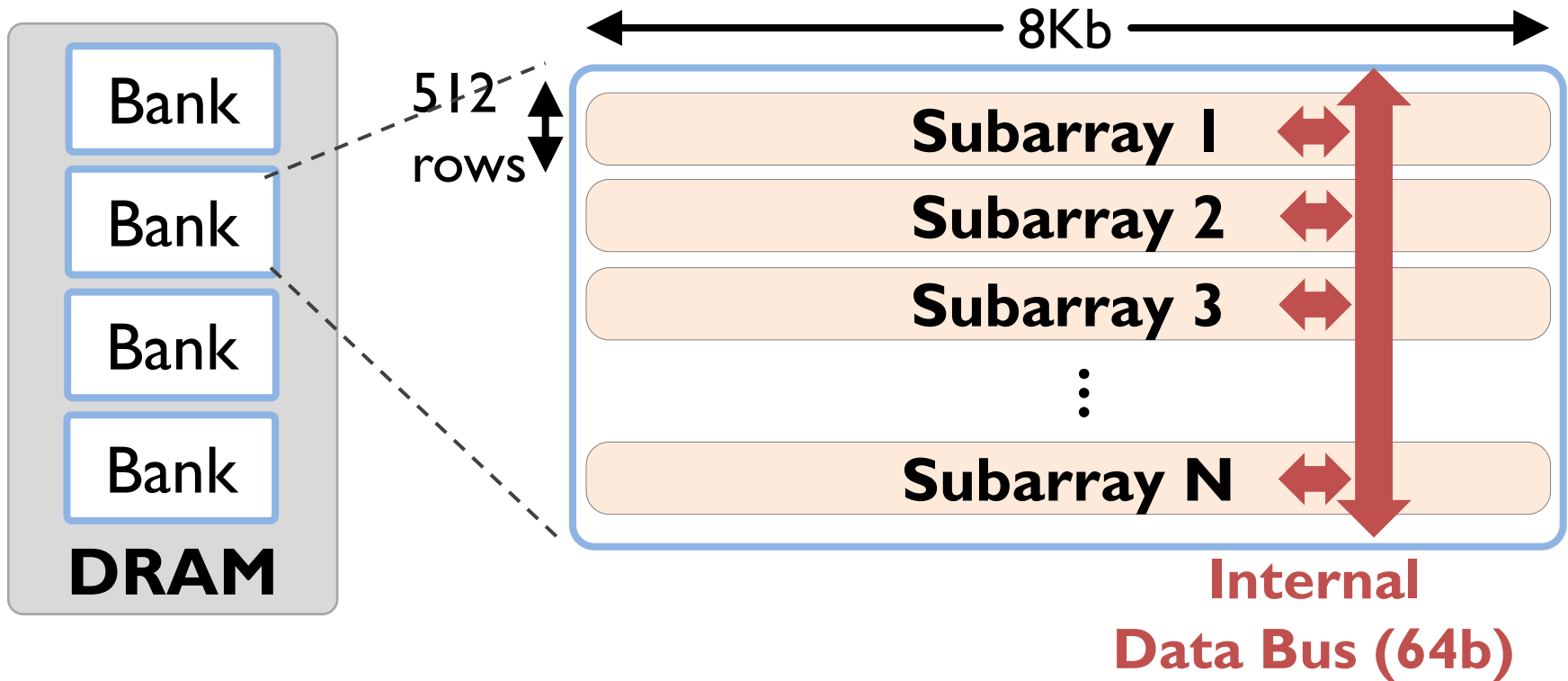
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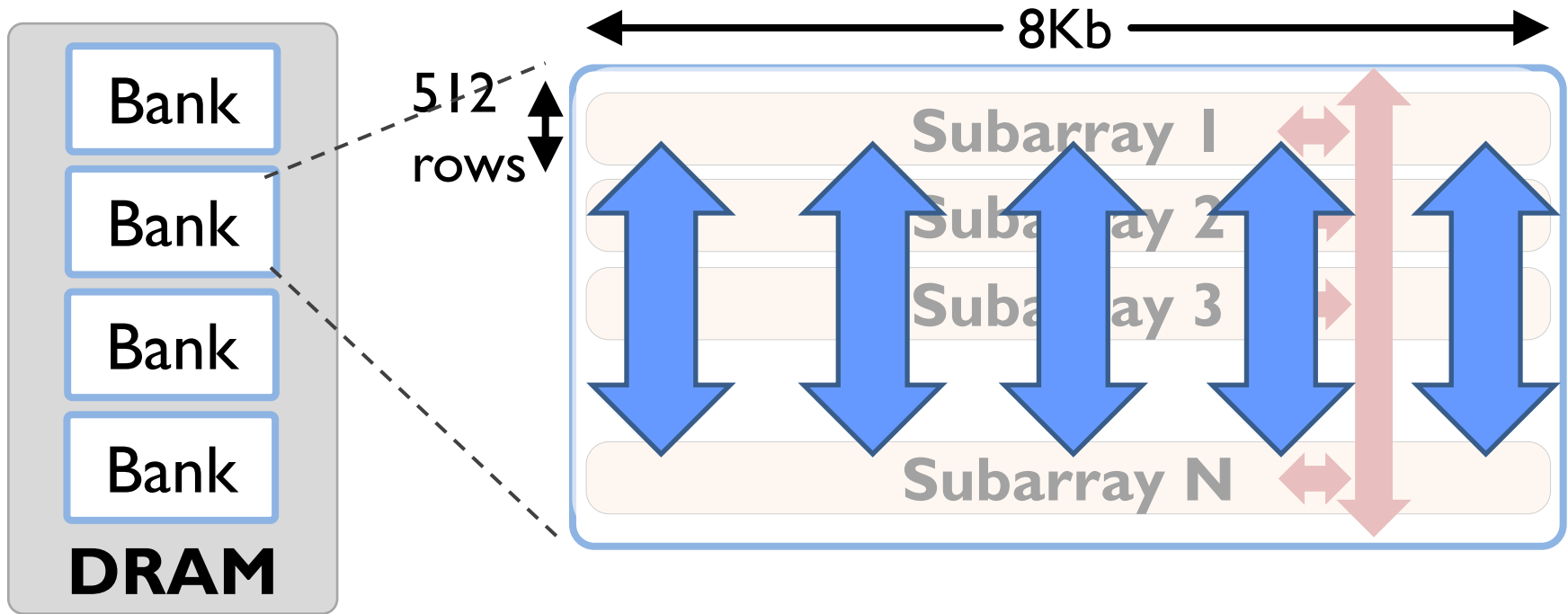


Moving Data Inside DRAM?



Low connectivity in DRAM is the fundamental bottleneck for bulk data movement

Moving Data Inside DRAM?



Goal: Provide a new substrate to enable wide connectivity between subarrays

Key Idea and Applications

- **Low-cost Inter-linked subarrays (LISA)**
 - Fast bulk data movement between subarrays
 - **Wide datapath via isolation transistors: 0.8% DRAM chip area**

Key Idea and Applications

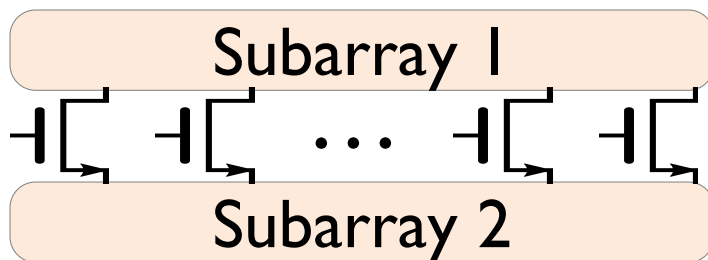
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Subarray 1

Subarray 2

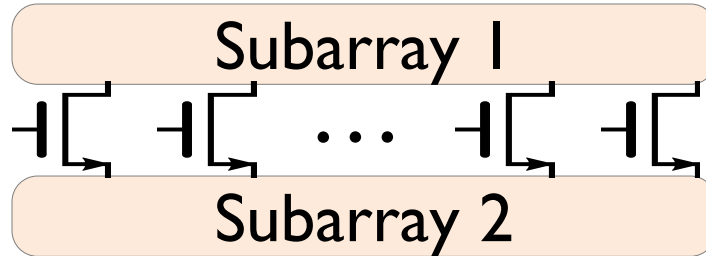
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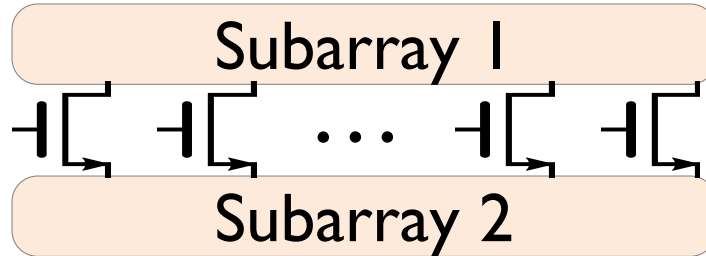
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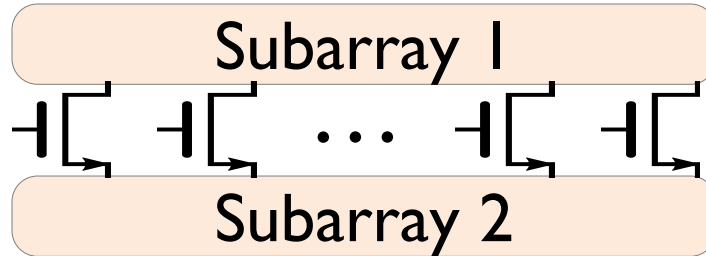
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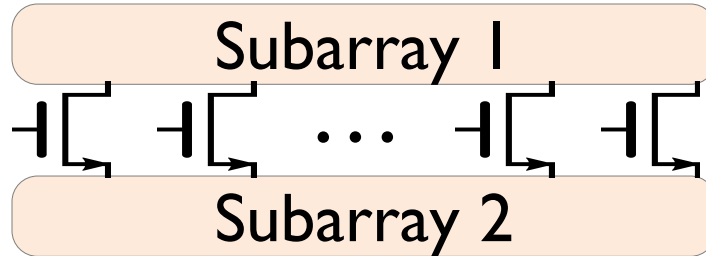


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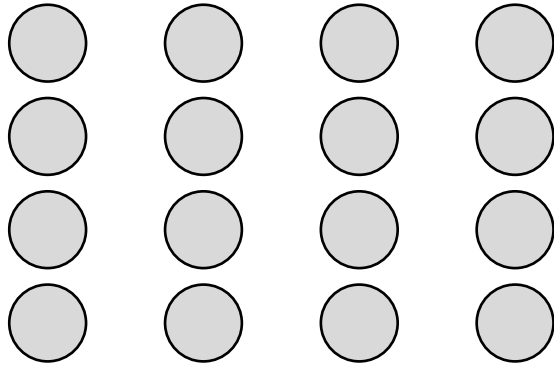
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→ 5% speedup
 - Fast precharge:** Precharge latency 13.1ns→5.0ns (**2.6x**)
→ 8% speedup

Outline

- Motivation and Key Idea
- **DRAM Background**
- LISA Substrate
 - New DRAM Command to Use LISA
- Applications of LISA

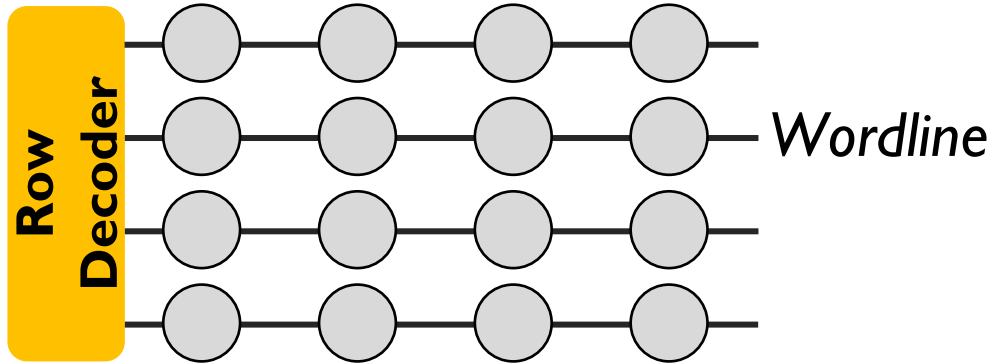
DRAM Internals

Subarray



DRAM Internals

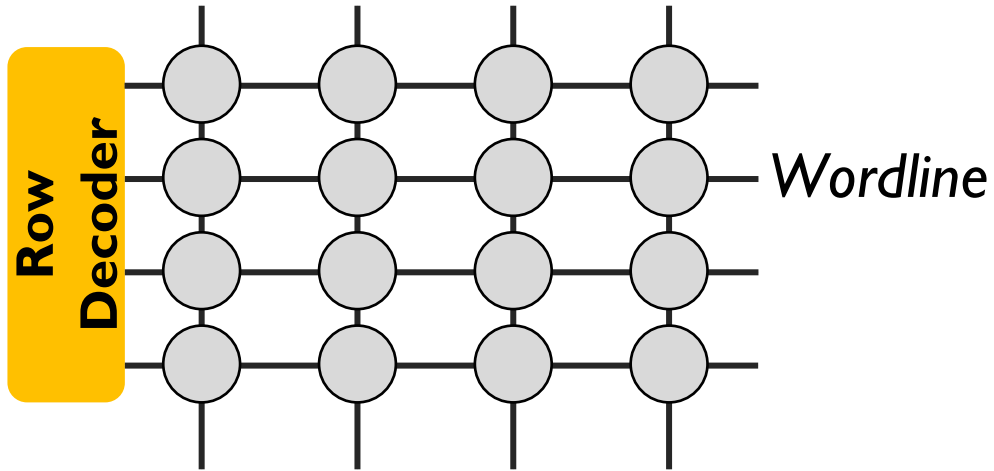
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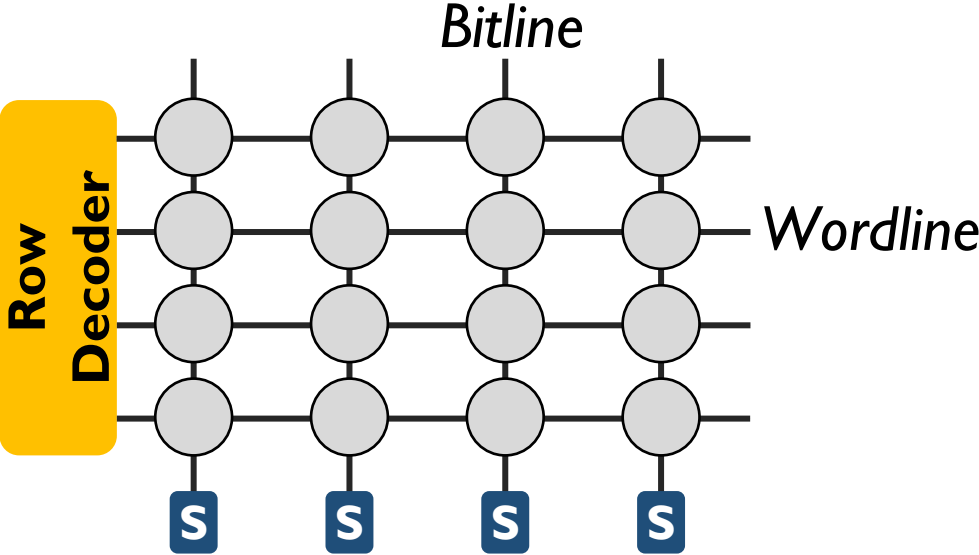
Subarray

Bitline



DRAM Internals

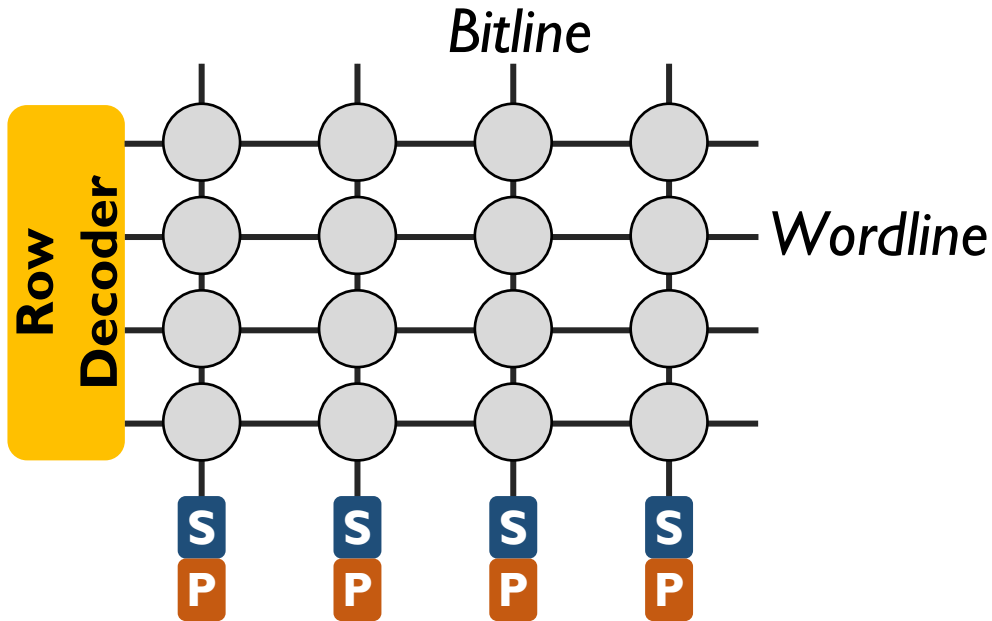
Subarray



S Sense amplifier

DRAM Internals

Subarray



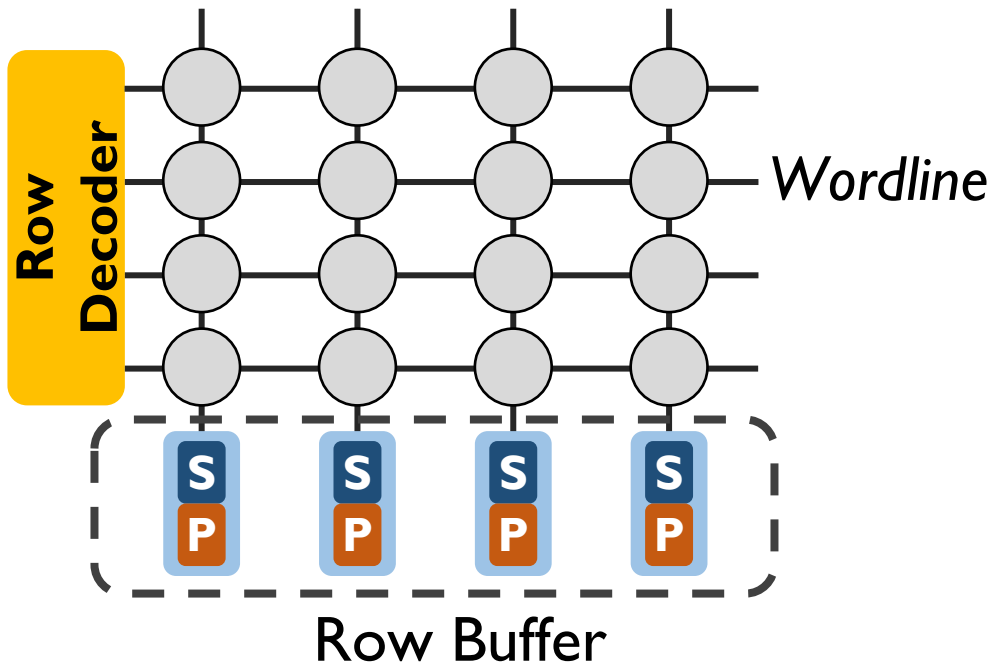
S Sense amplifier

P Precharge unit

DRAM Internals

Subarray

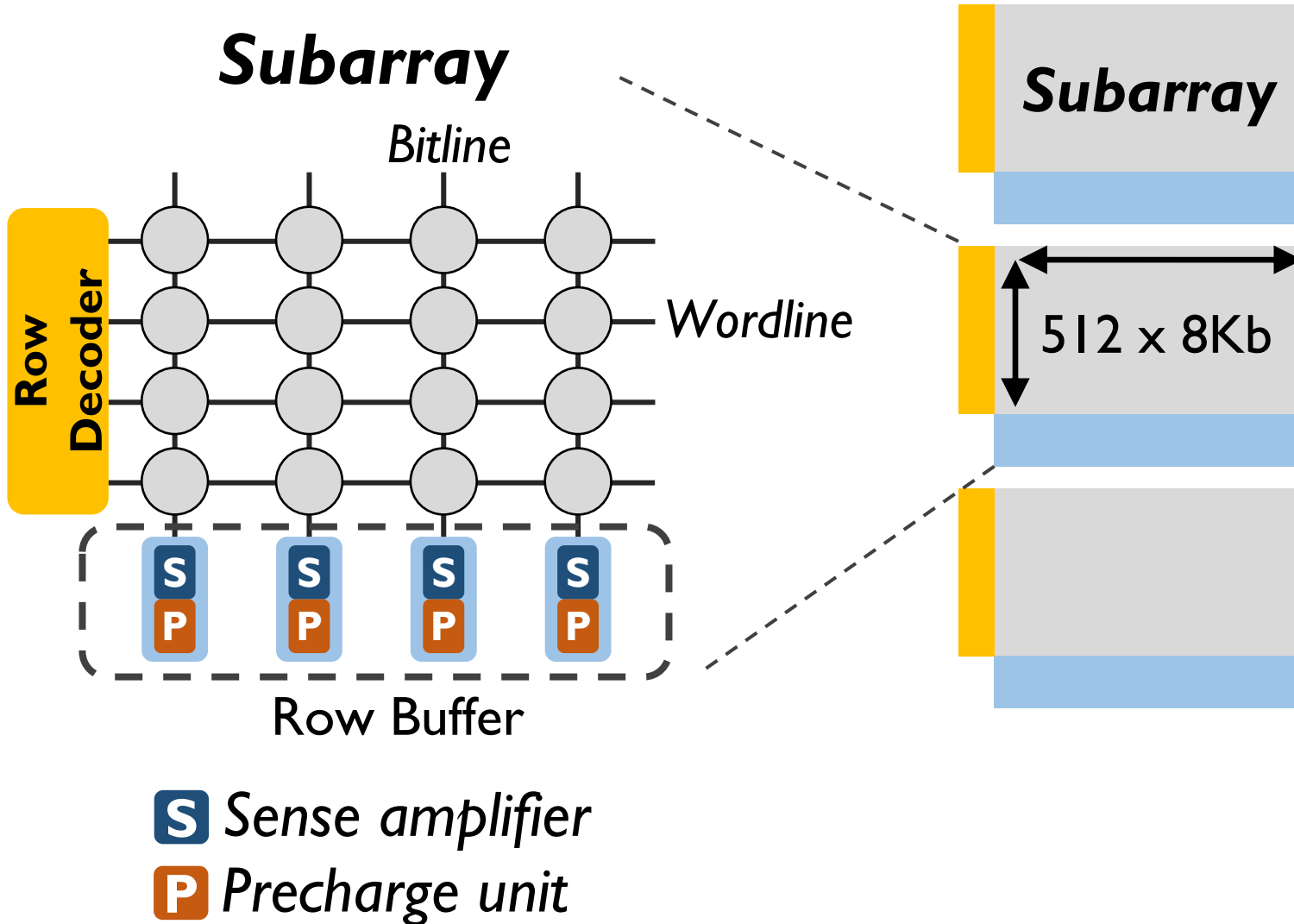
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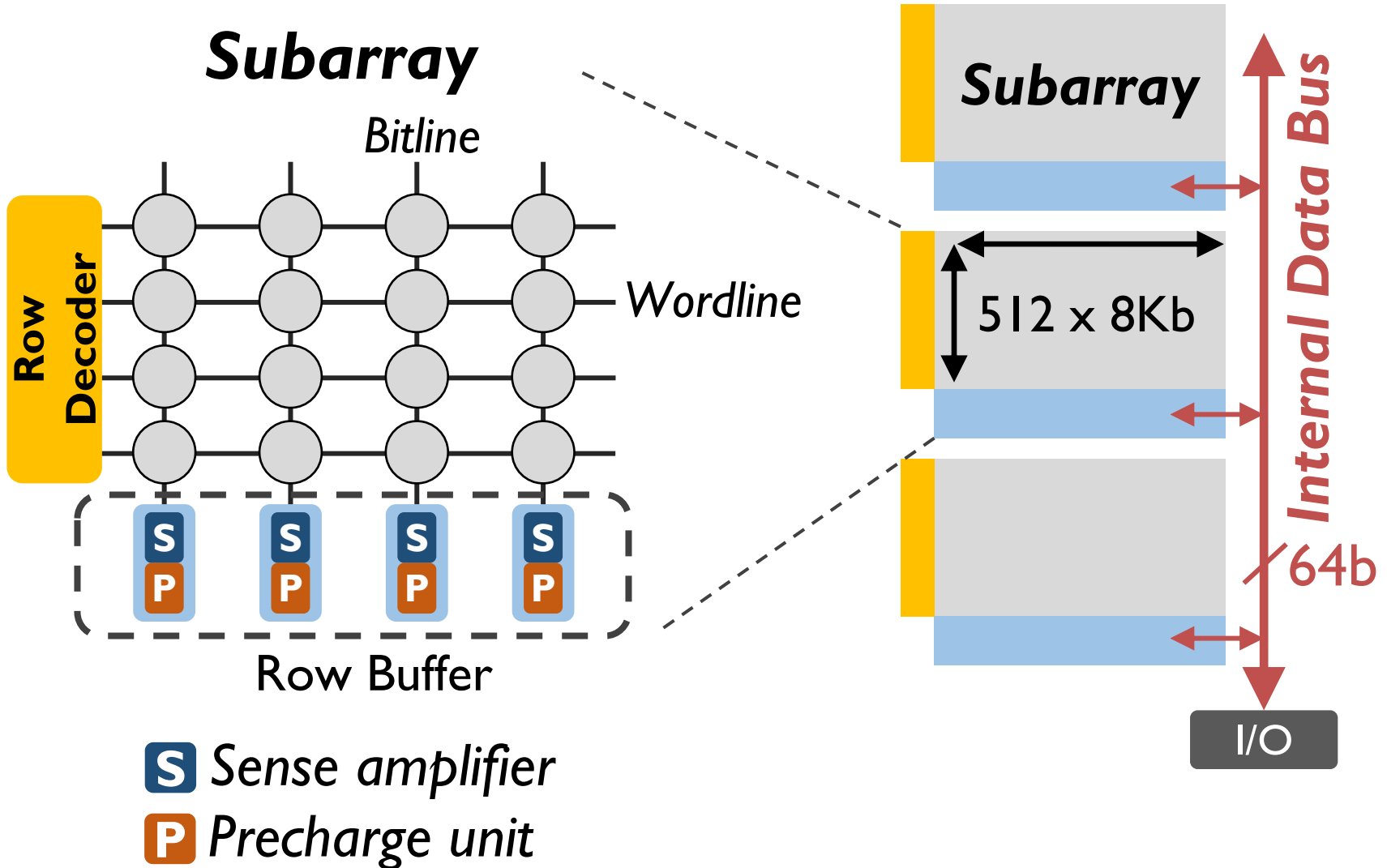
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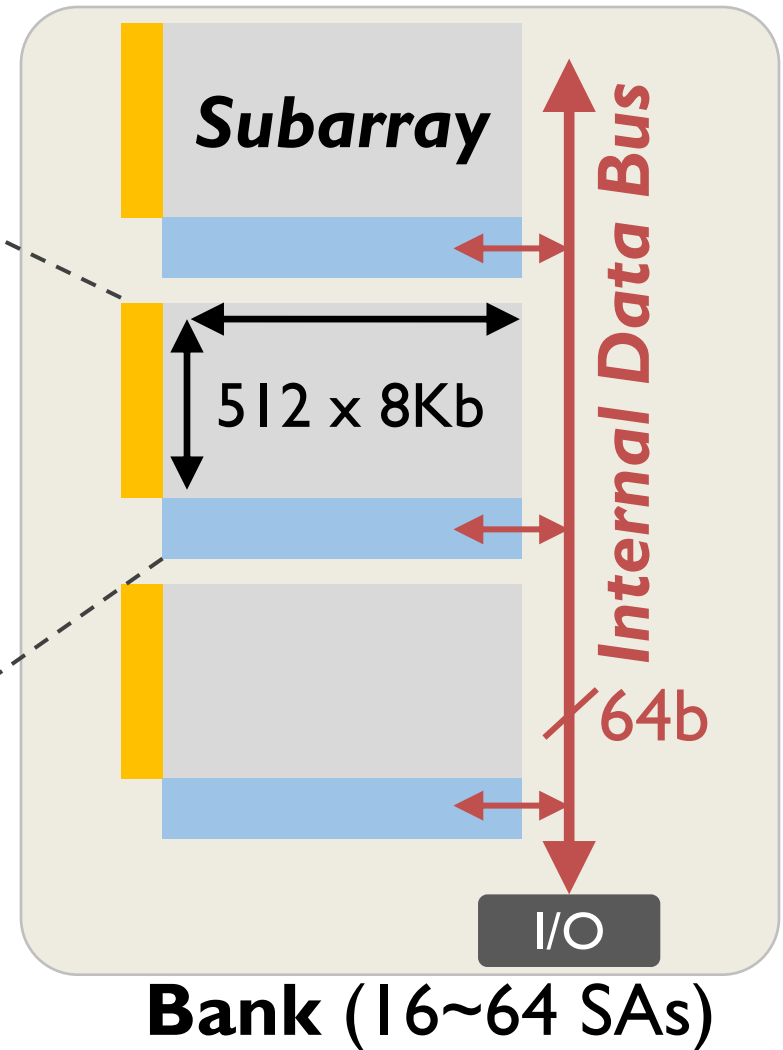
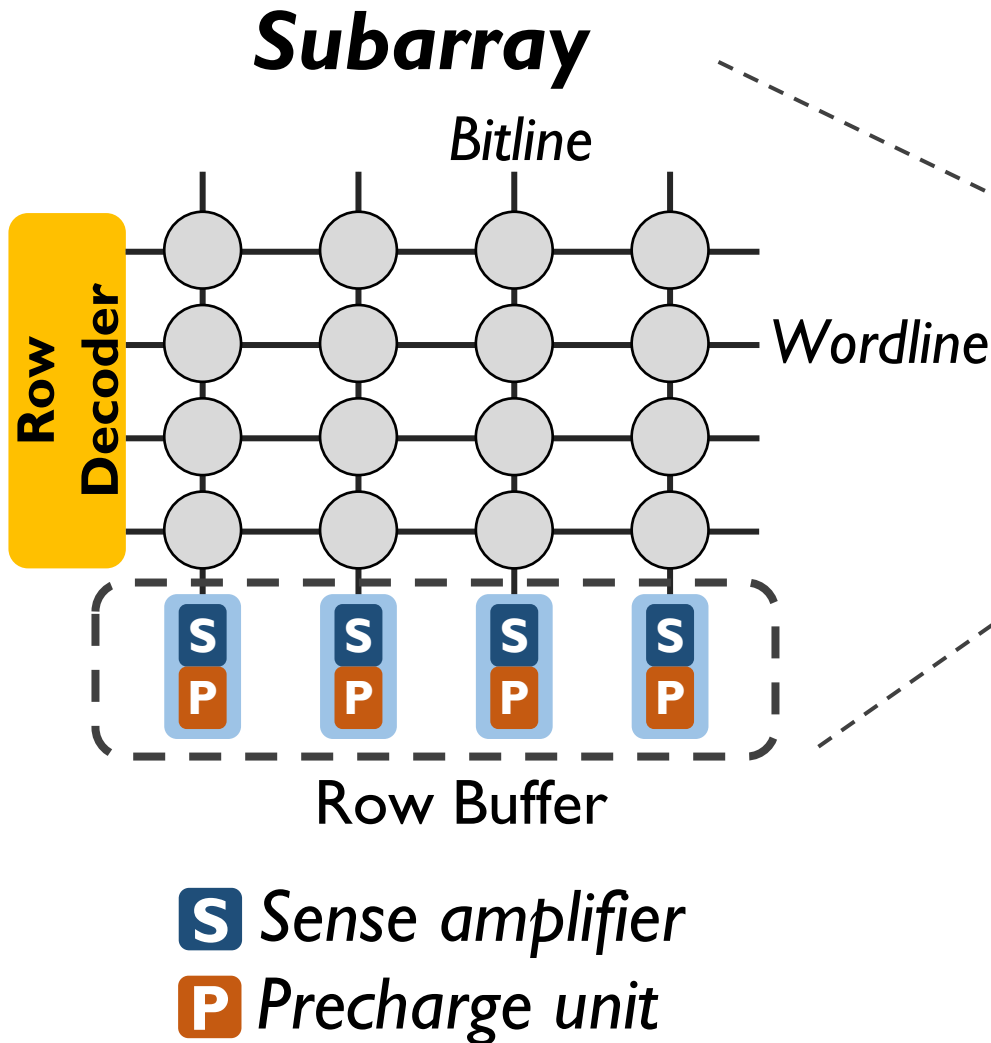
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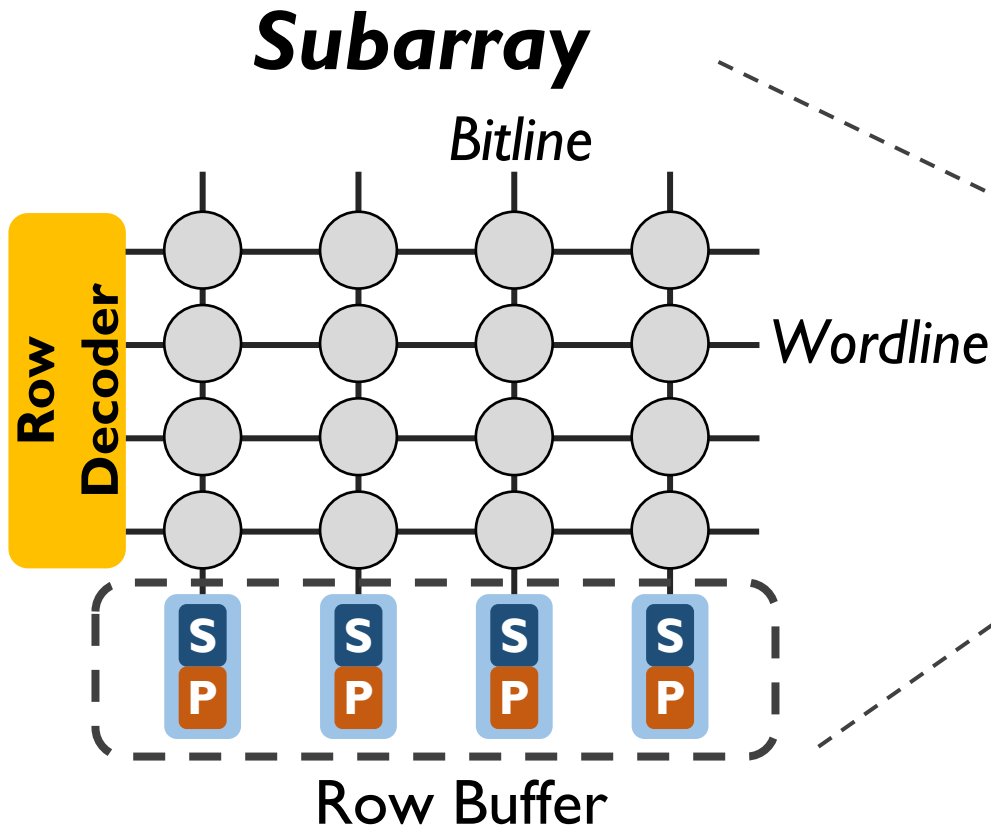
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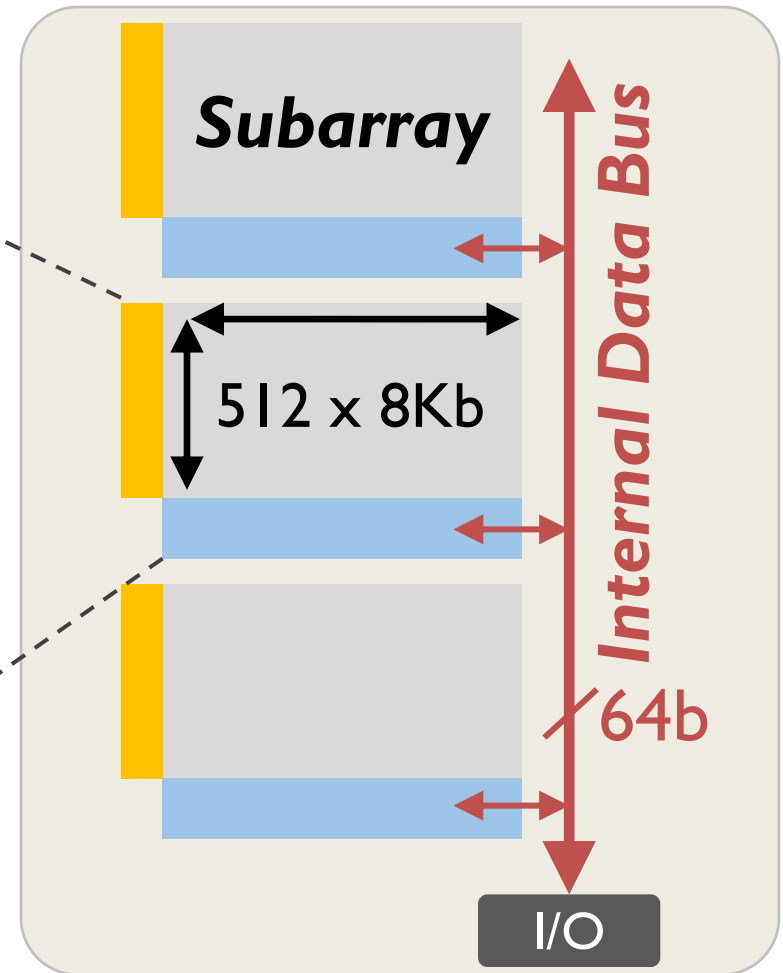
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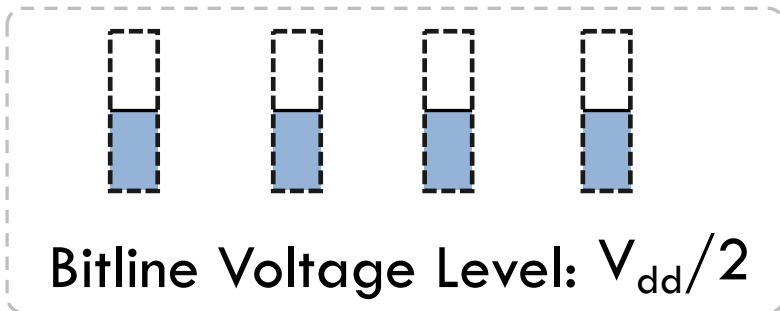
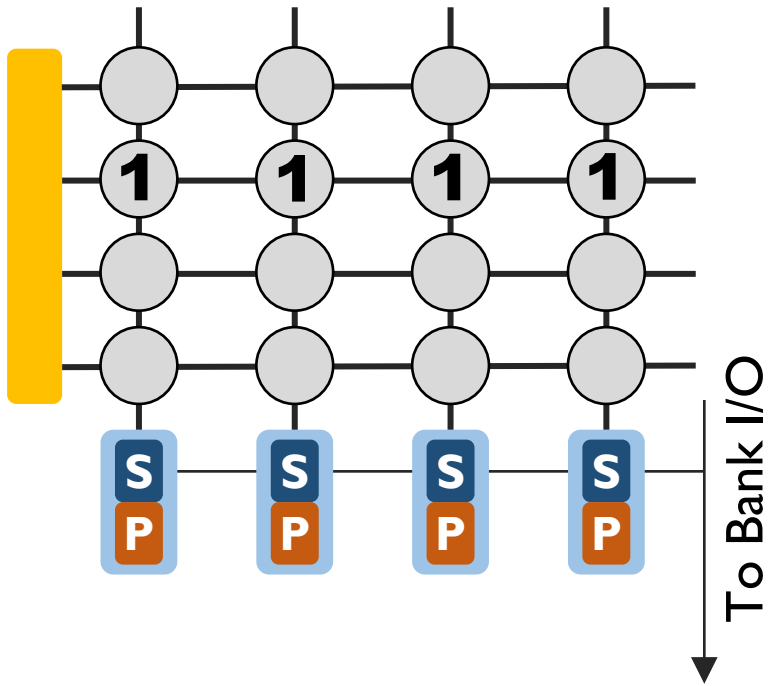


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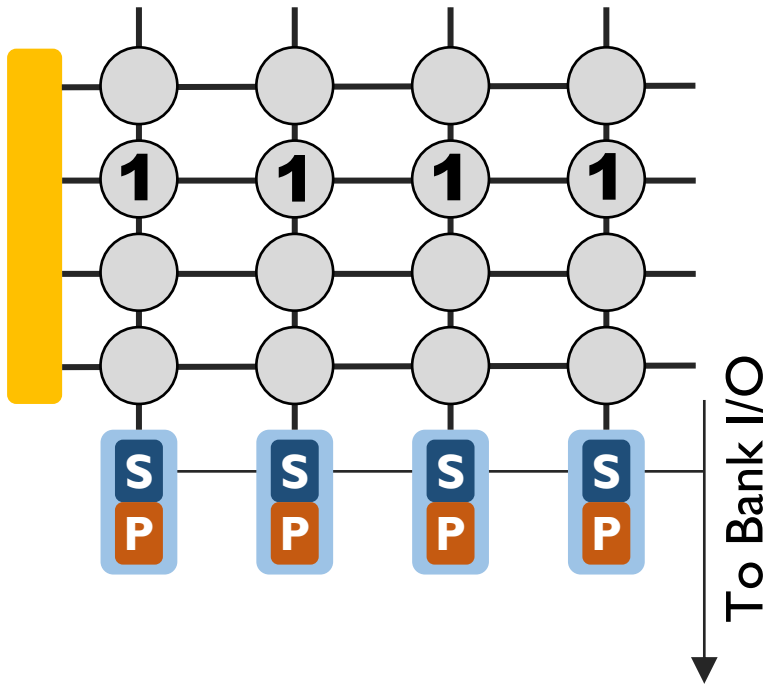


Bank (16~64 SAs)
8~16 banks per chip

DRAM Operation

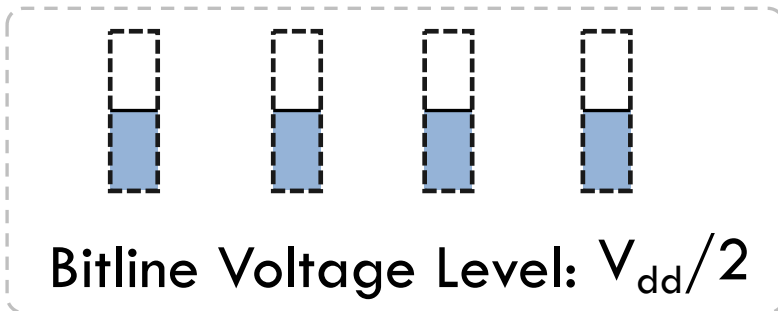


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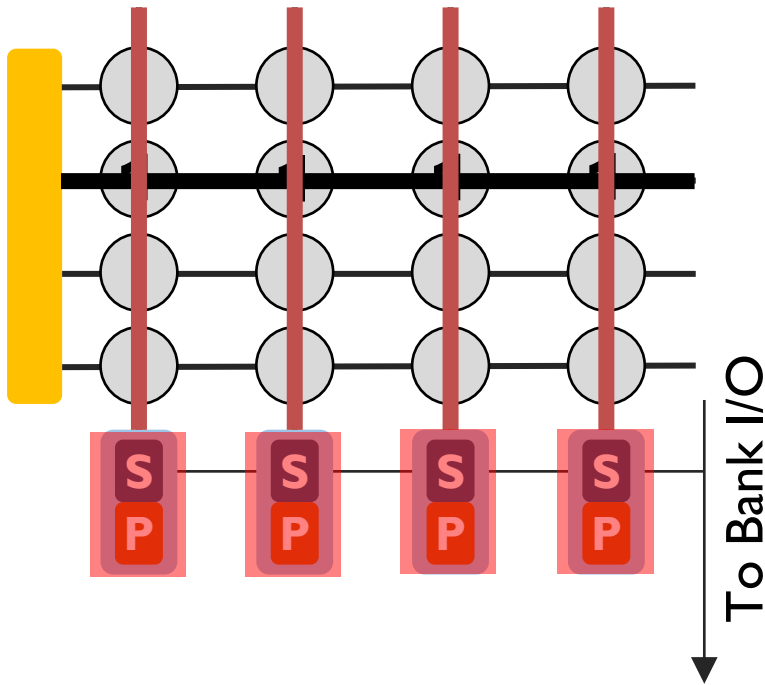


1

ACTIVATE: Store the row into the row buffer

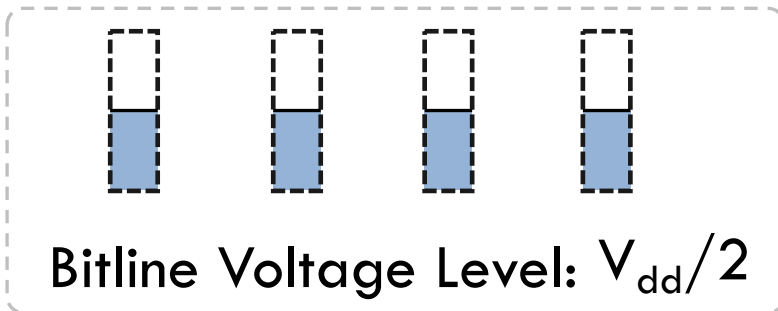


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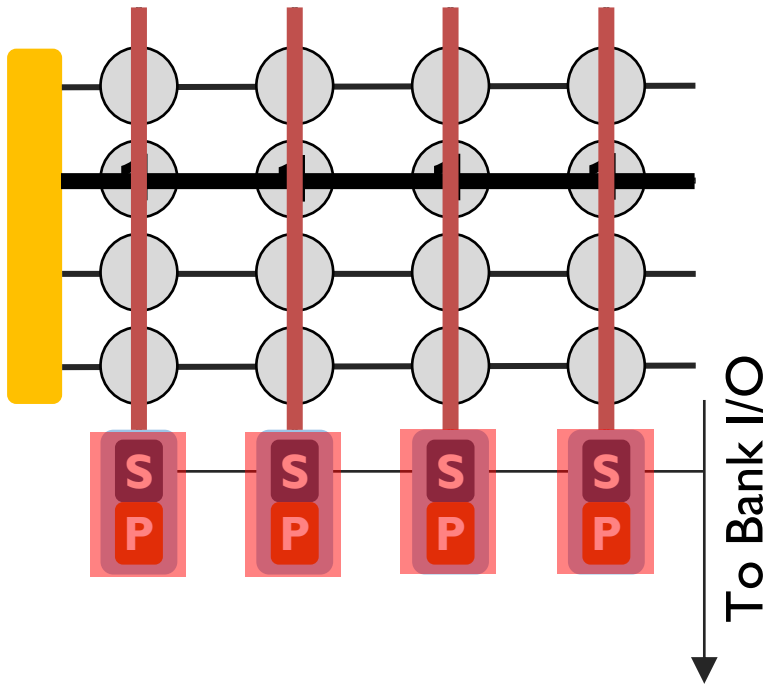


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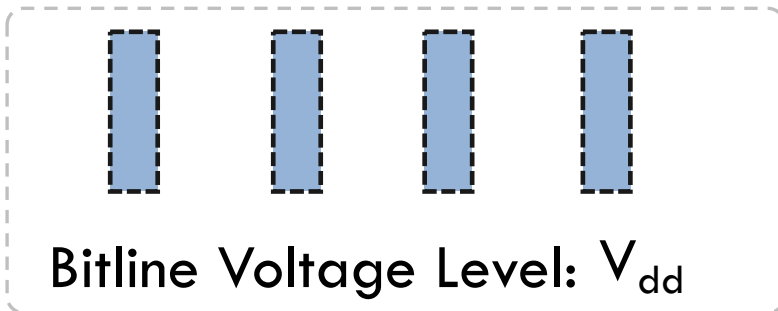


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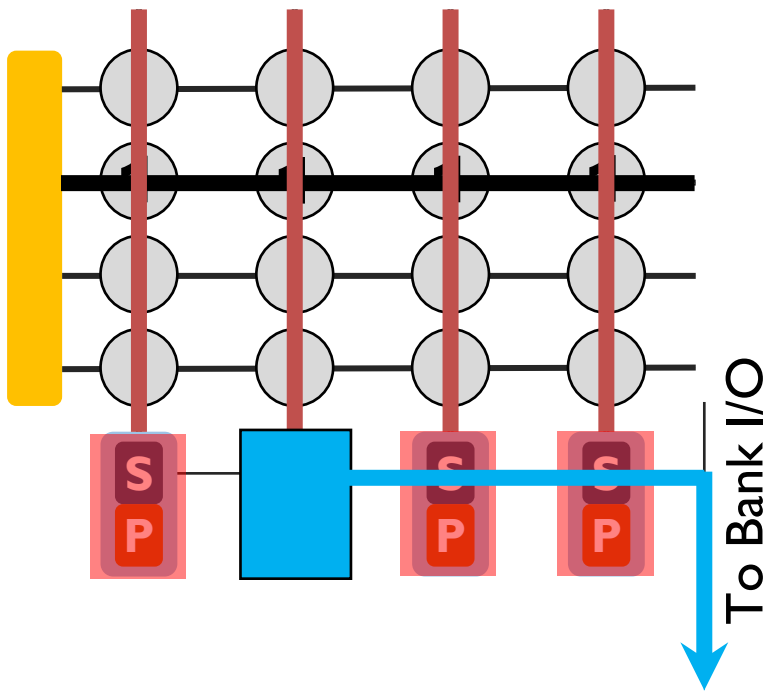


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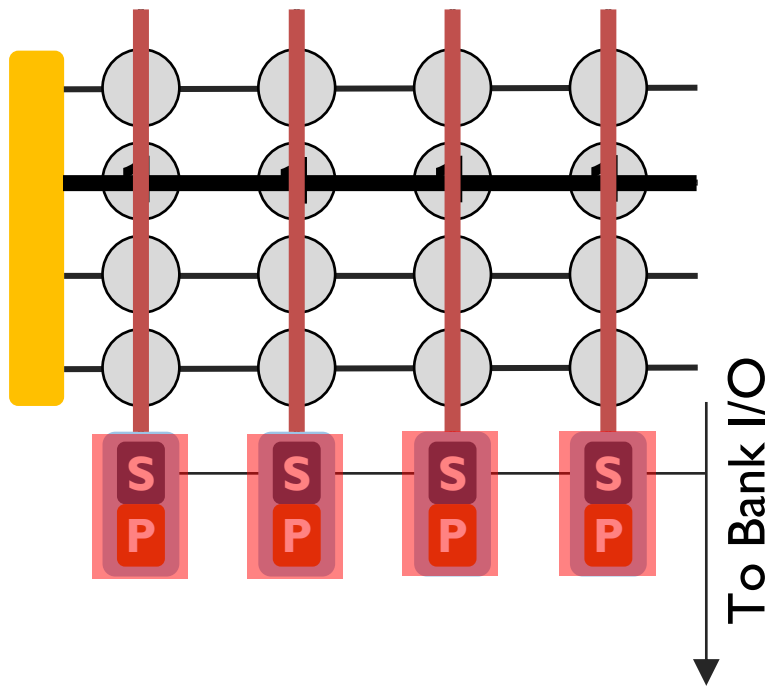


1 **ACTIVATE**: Store the row into the **row buffer**

2 **READ**: Select the target column and drive to I/O

Bitline Voltage Level: V_{dd}

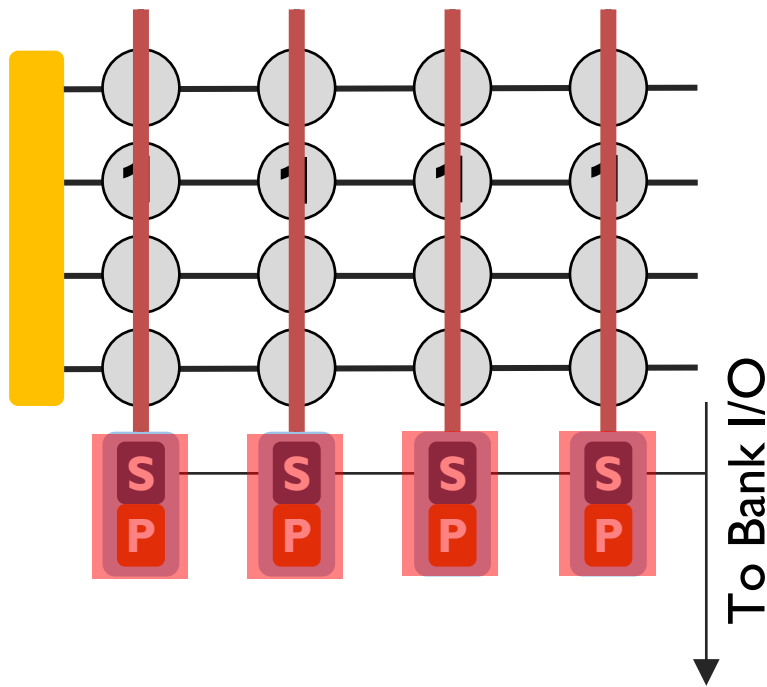
DRAM Operation



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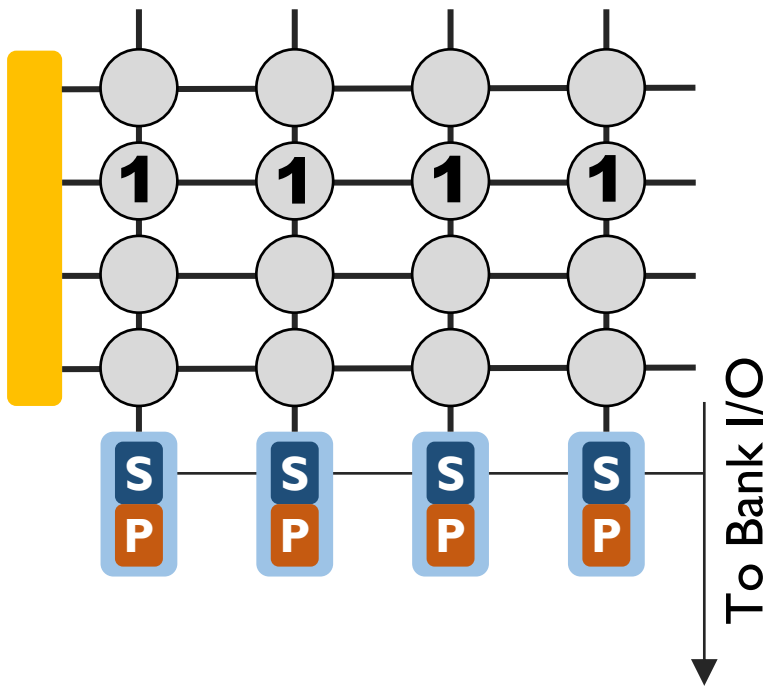
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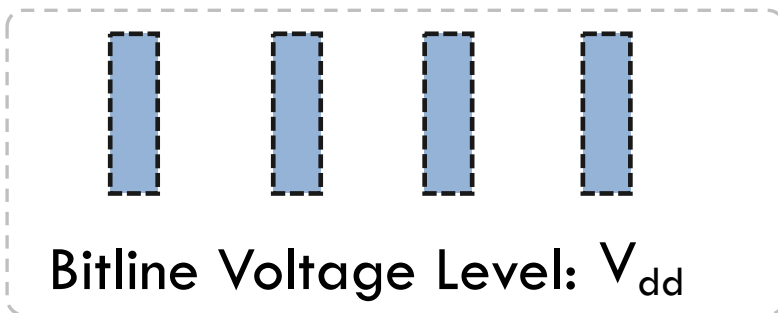
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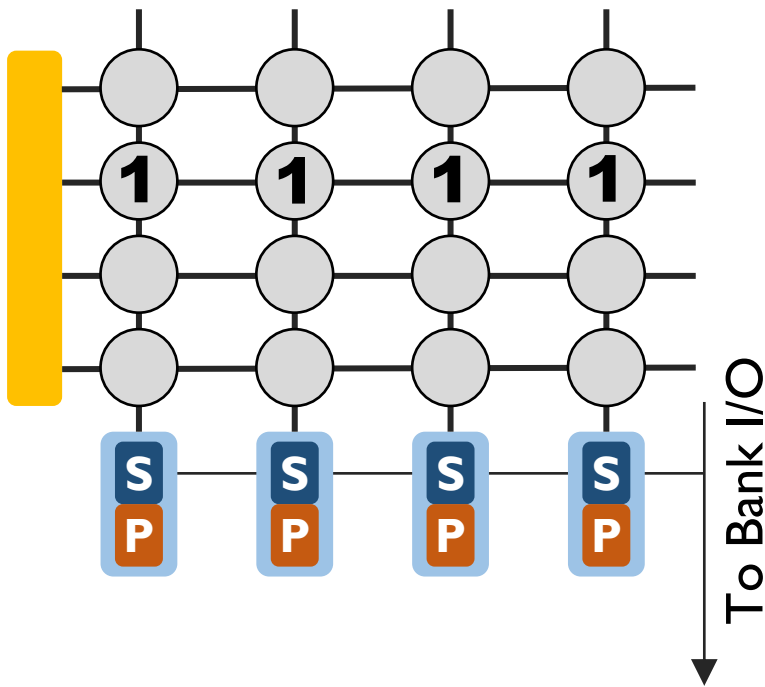
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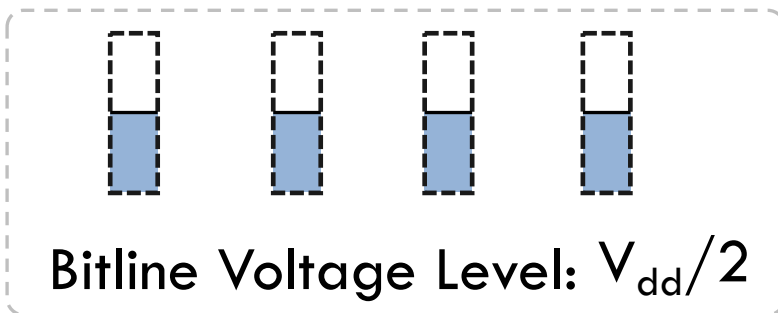
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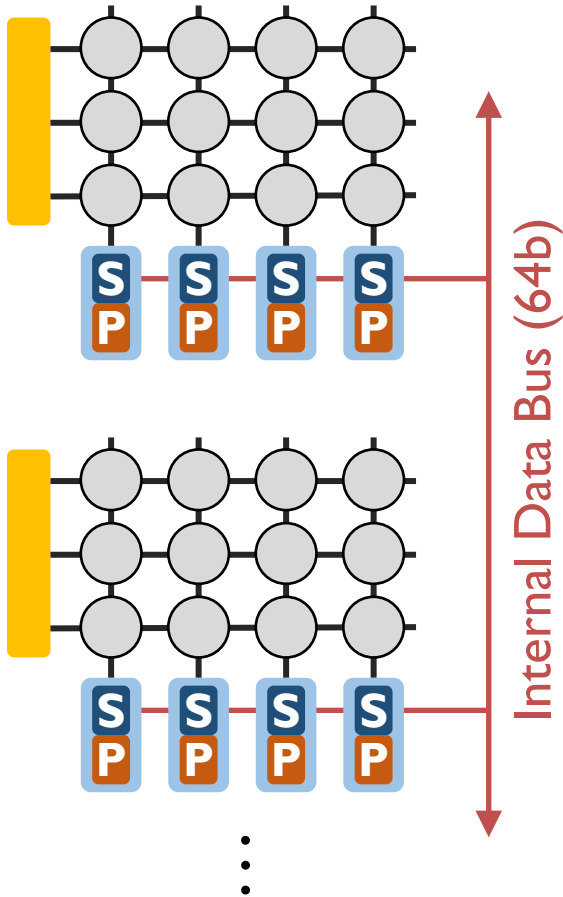
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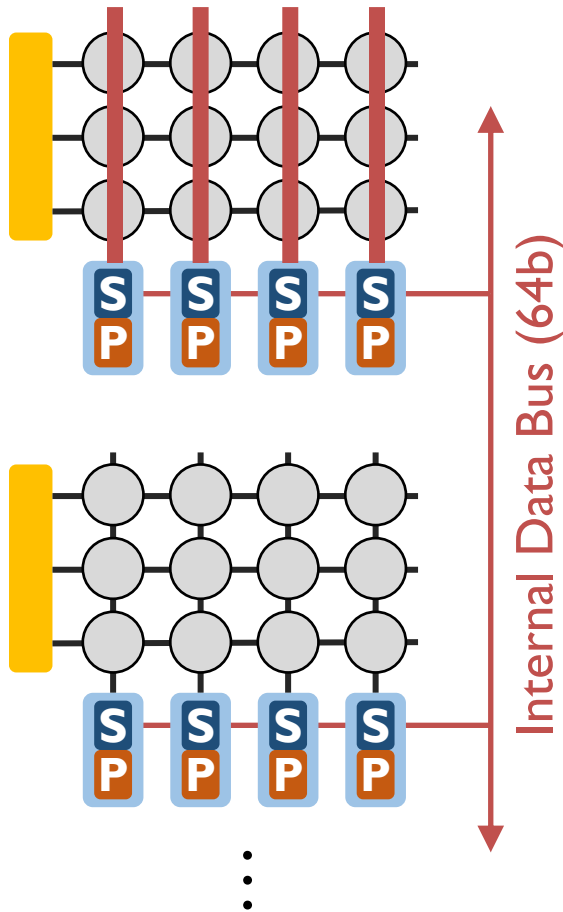
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- **LISA Substrate**
 - **New DRAM Command to Use LISA**
- Applications of LISA

Observations

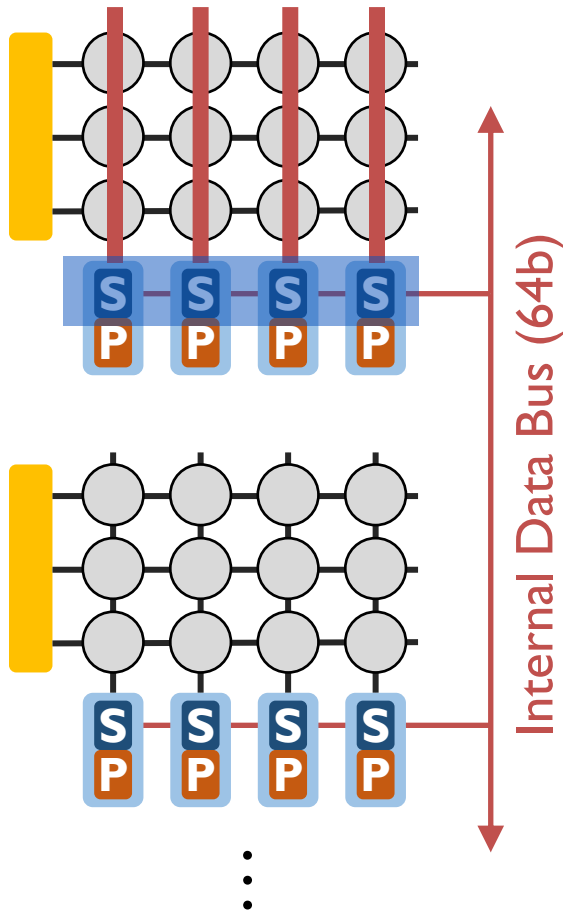


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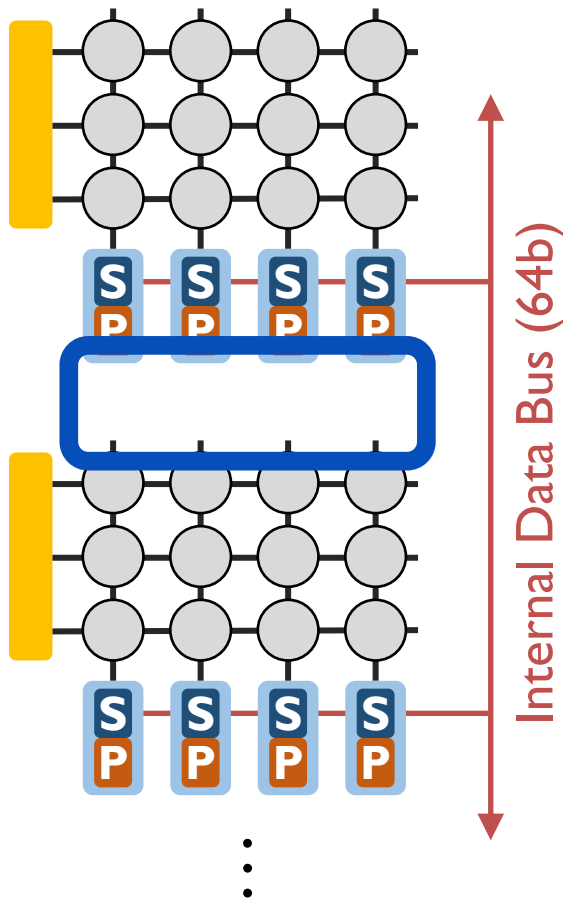
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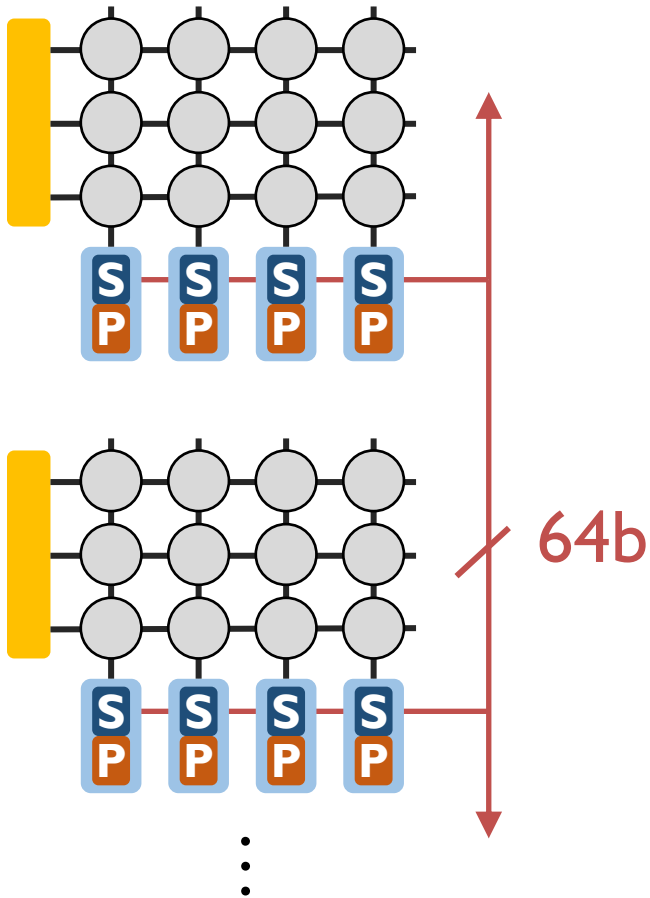
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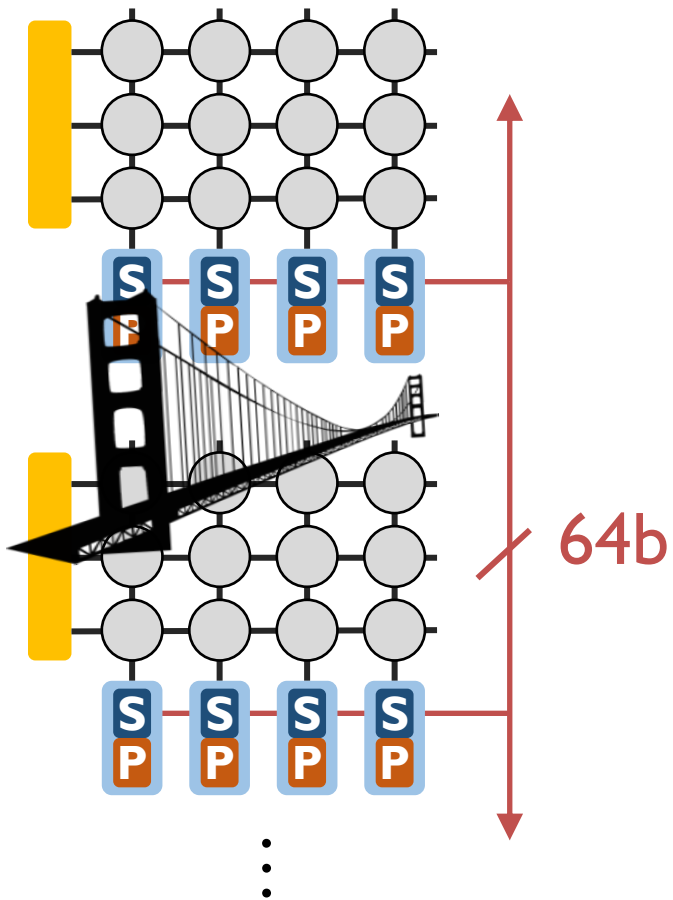


- 1 Bitlines serve as a bus that is as wide as a row
- 2 Bitlines between subarrays are close but disconnected

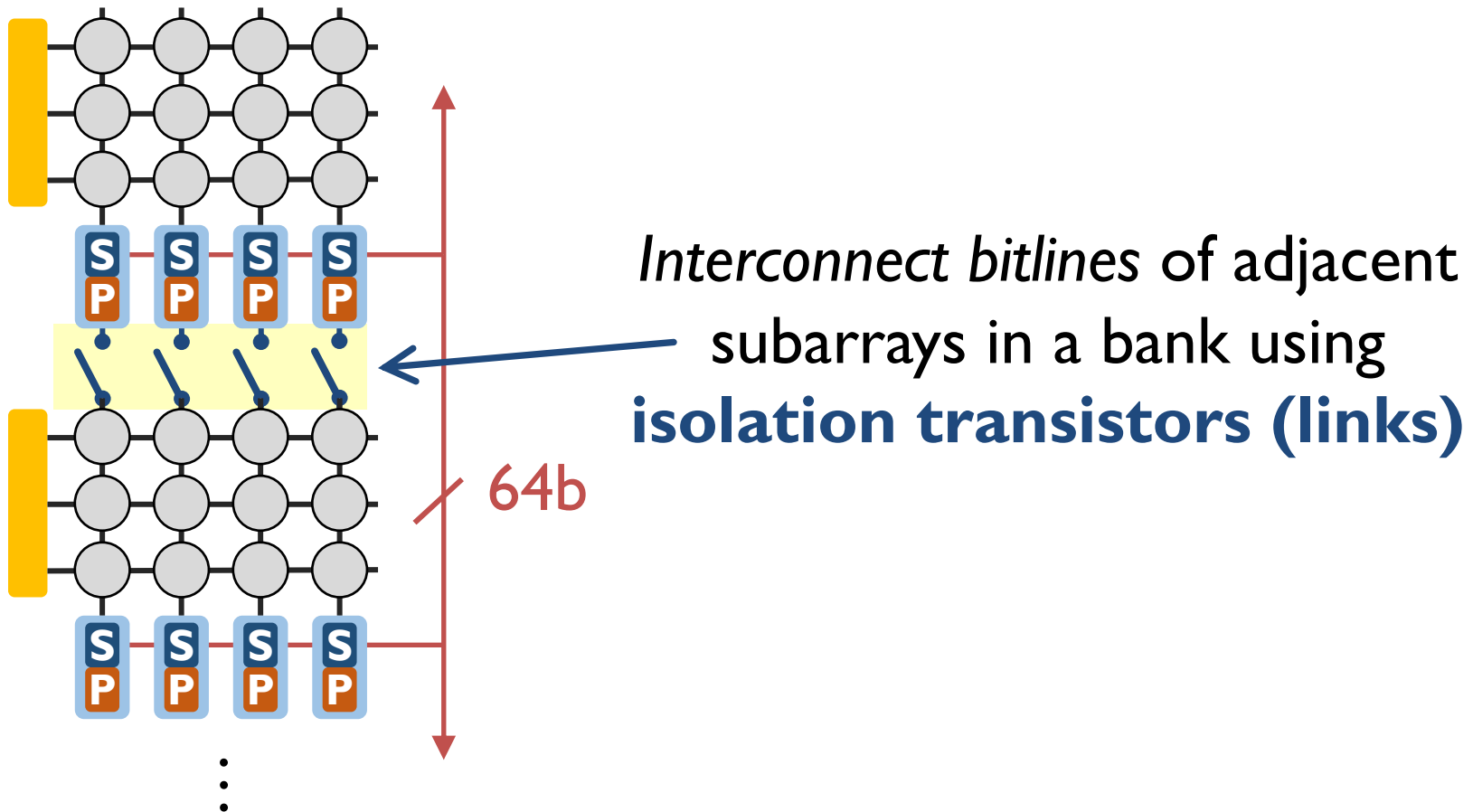
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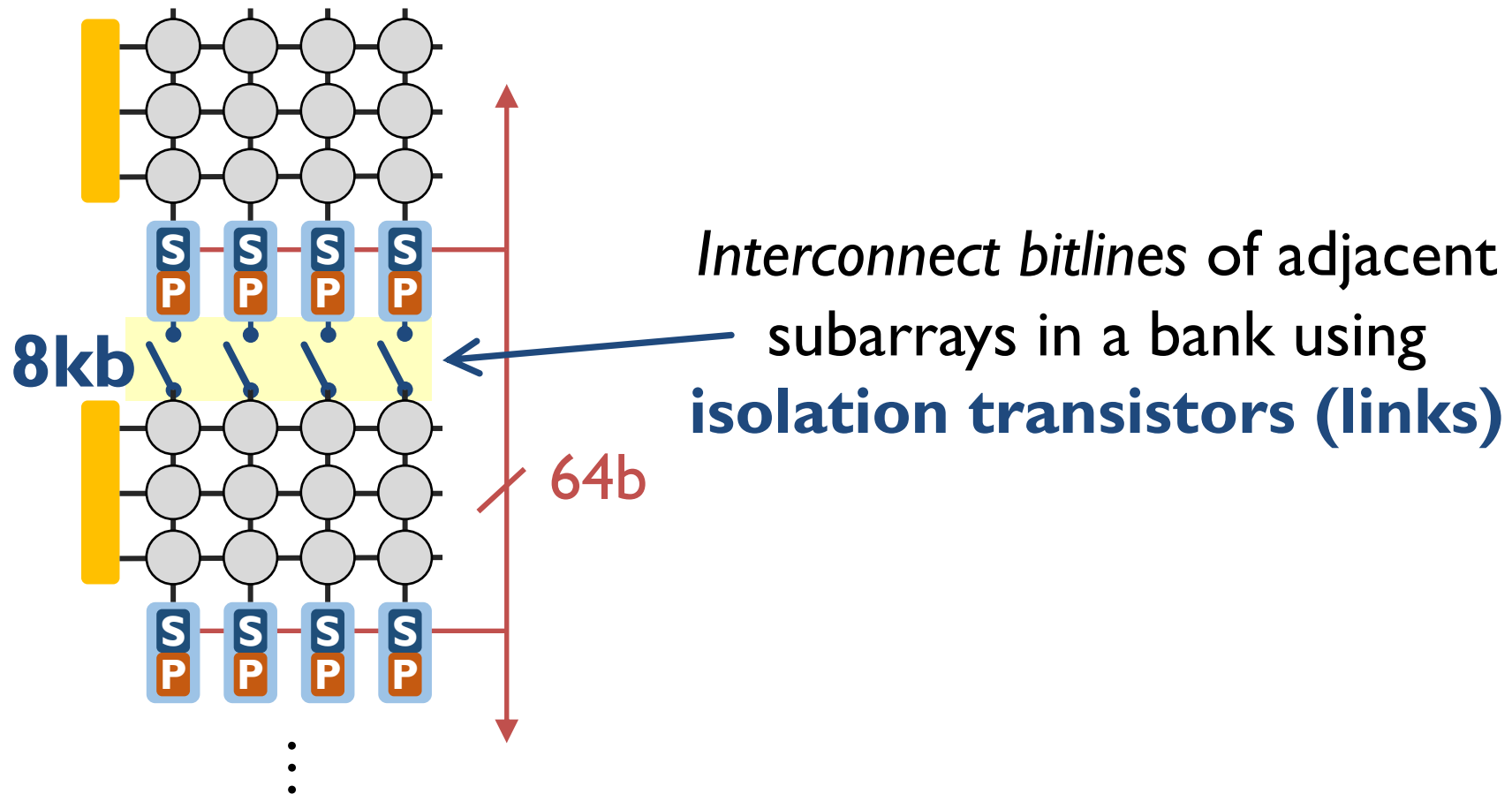
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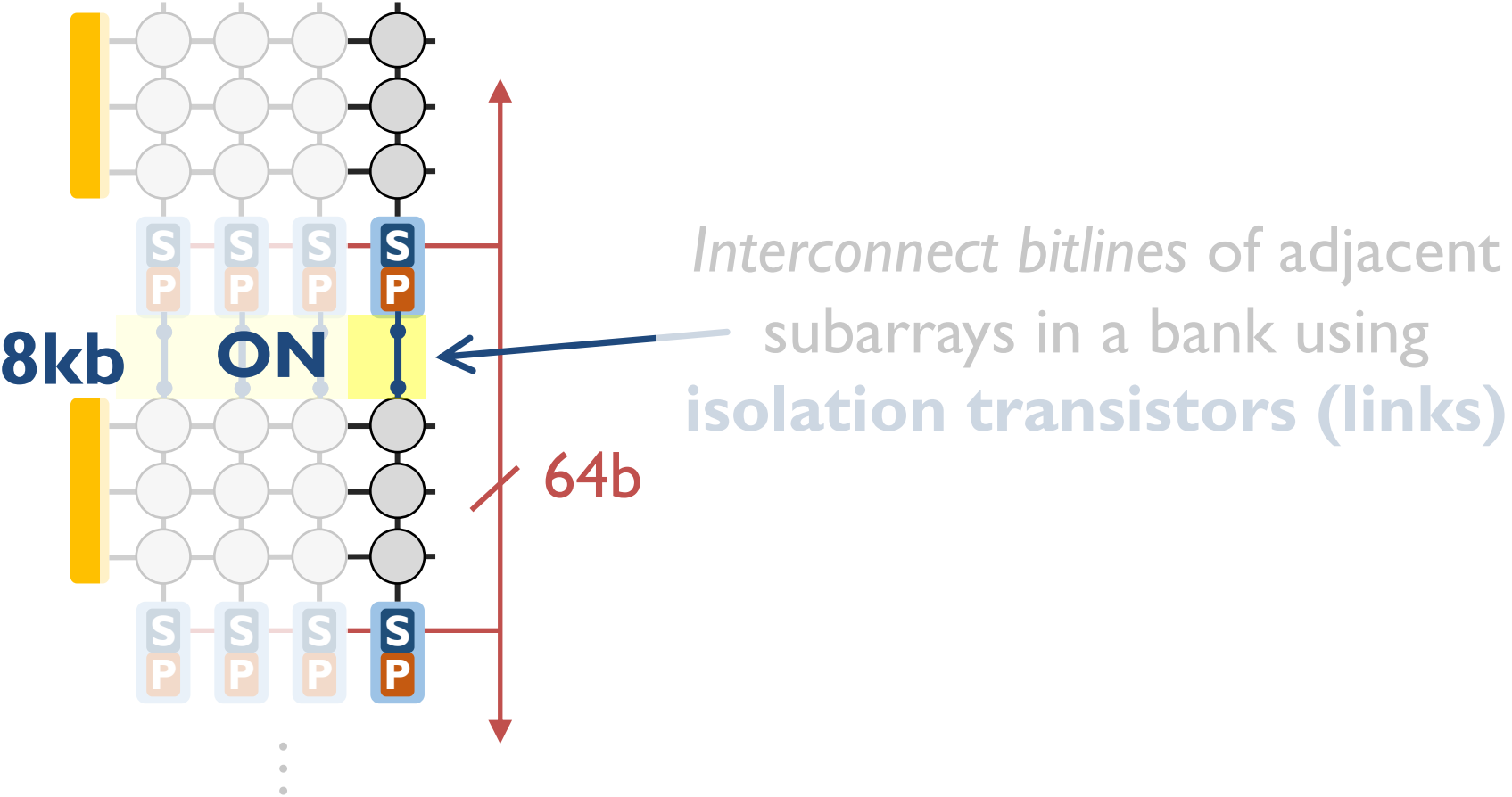
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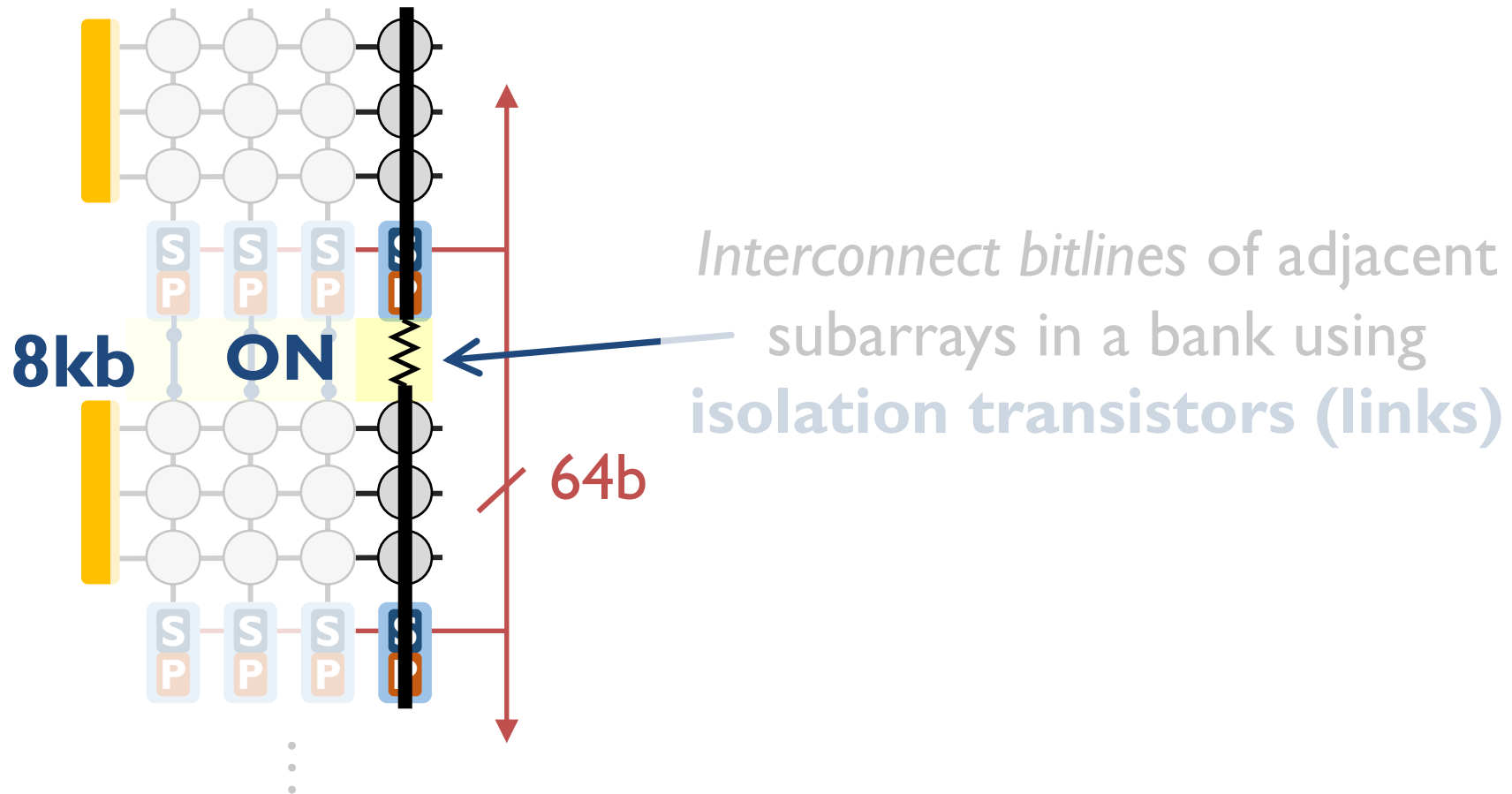
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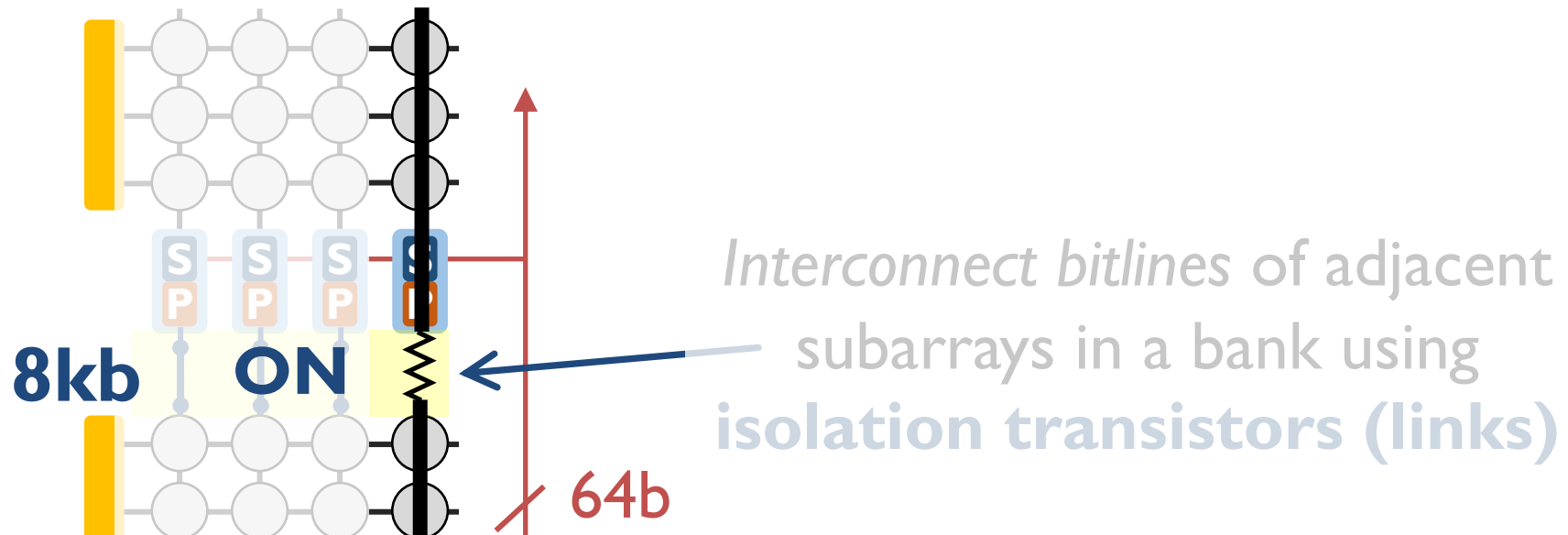
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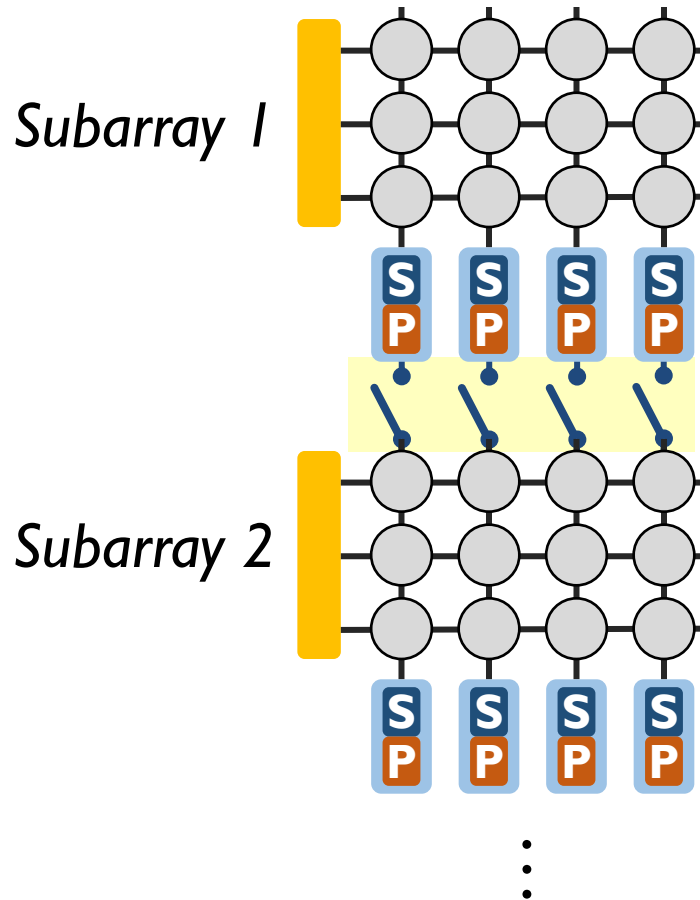
LISA forms a wide datapath b/w subarrays

New DRAM Command to Use LISA

Row Buffer Movement (RBM): Move a row of data in an activated row buffer to a precharged one

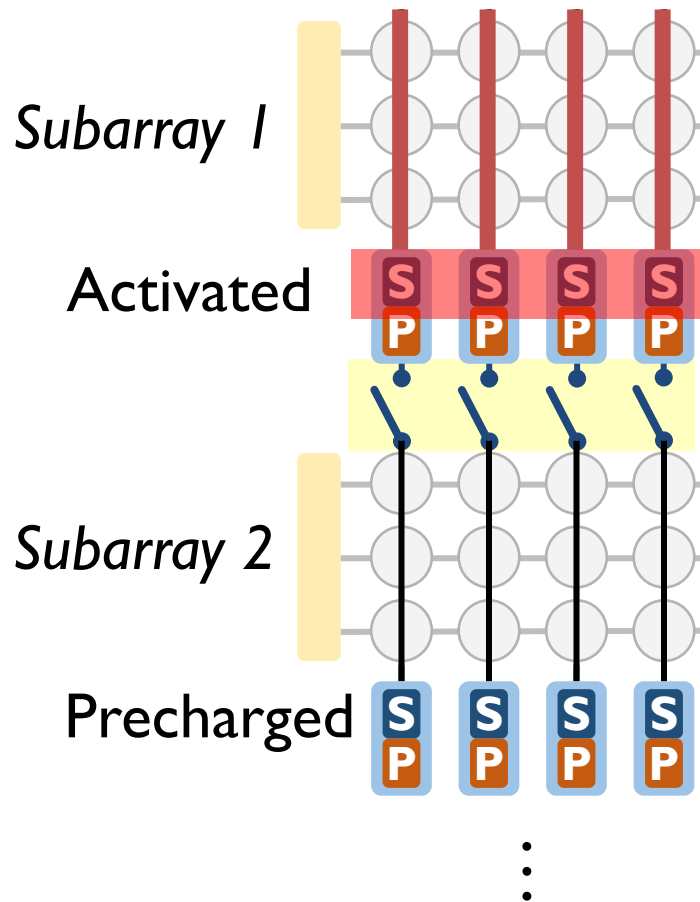
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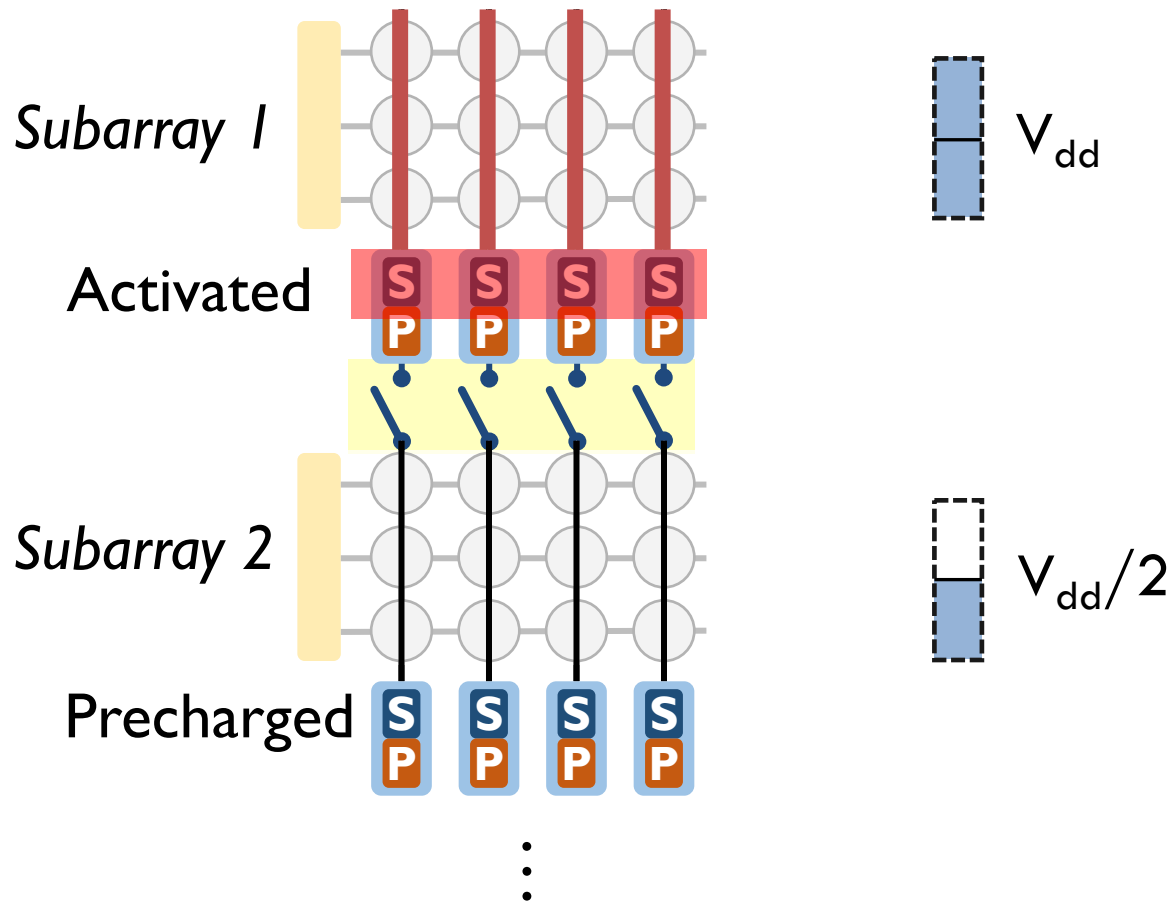
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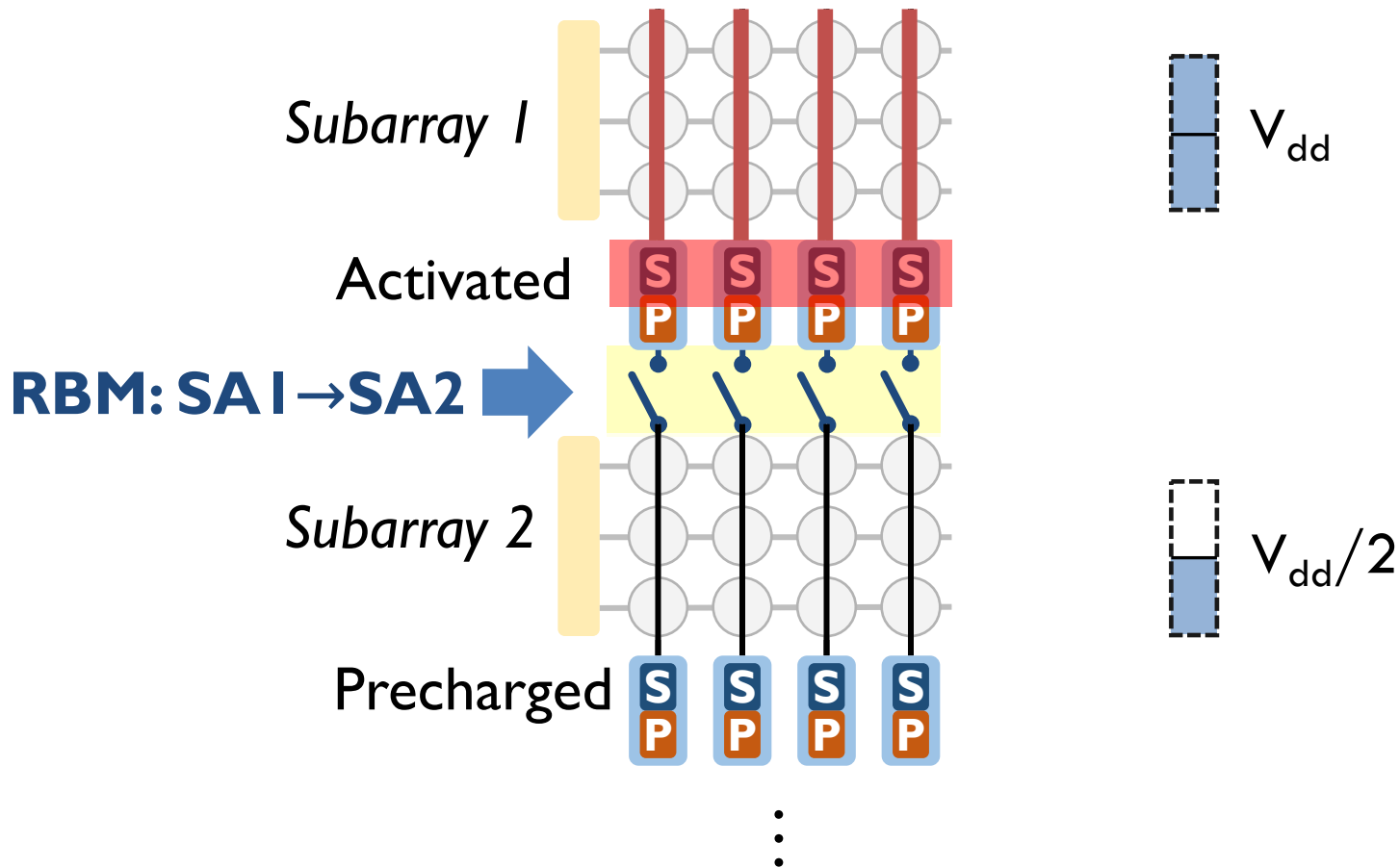
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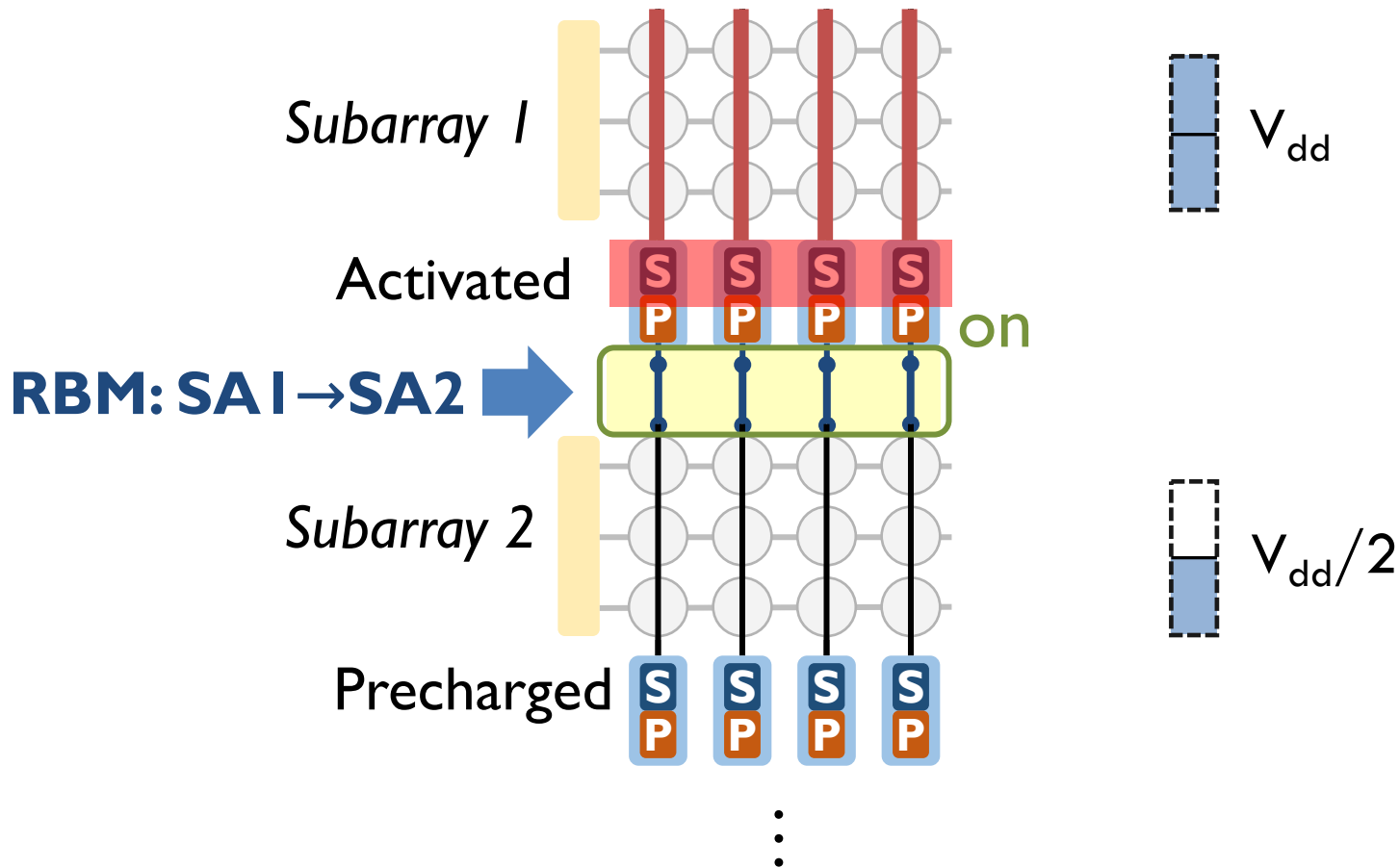
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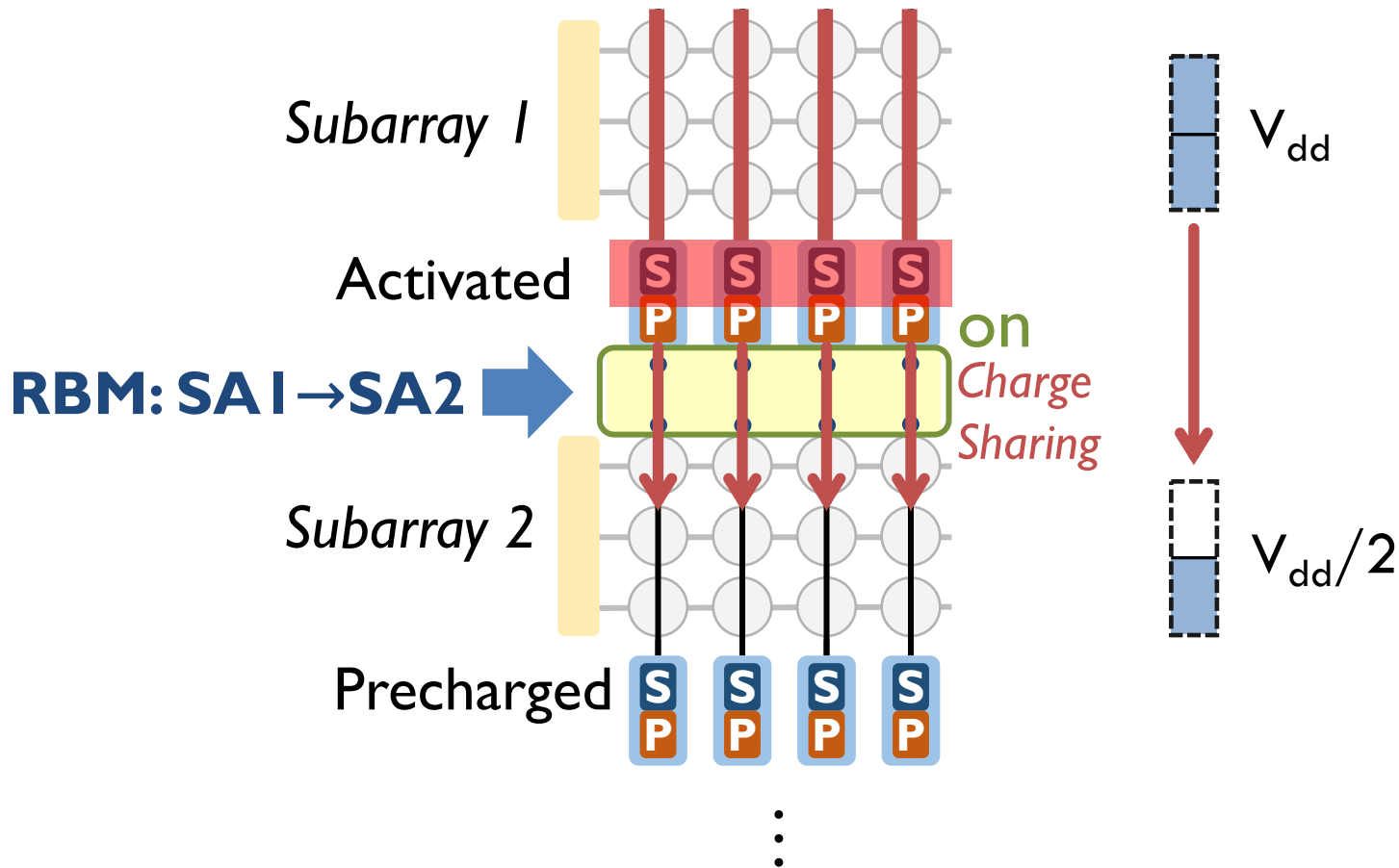
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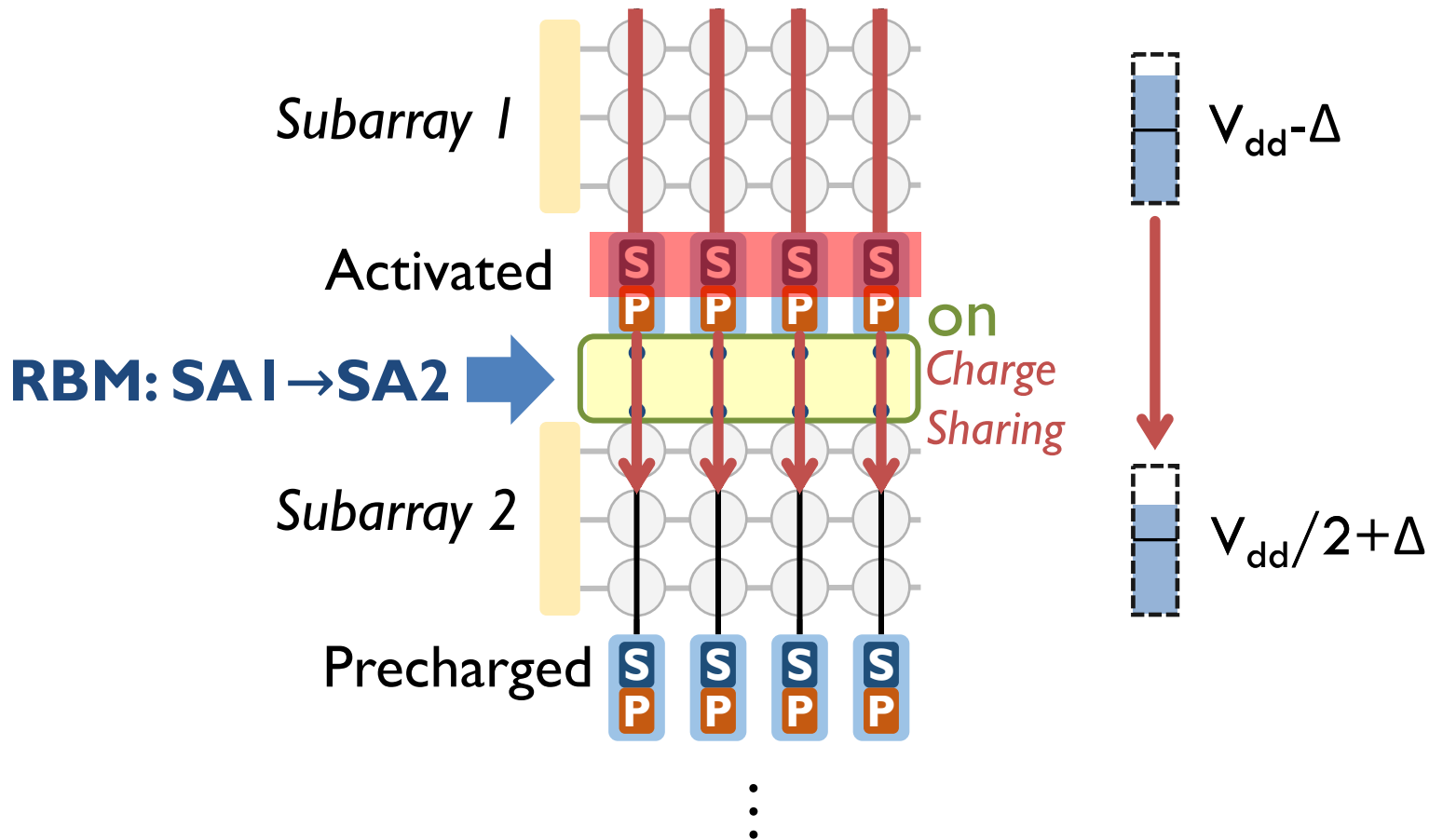
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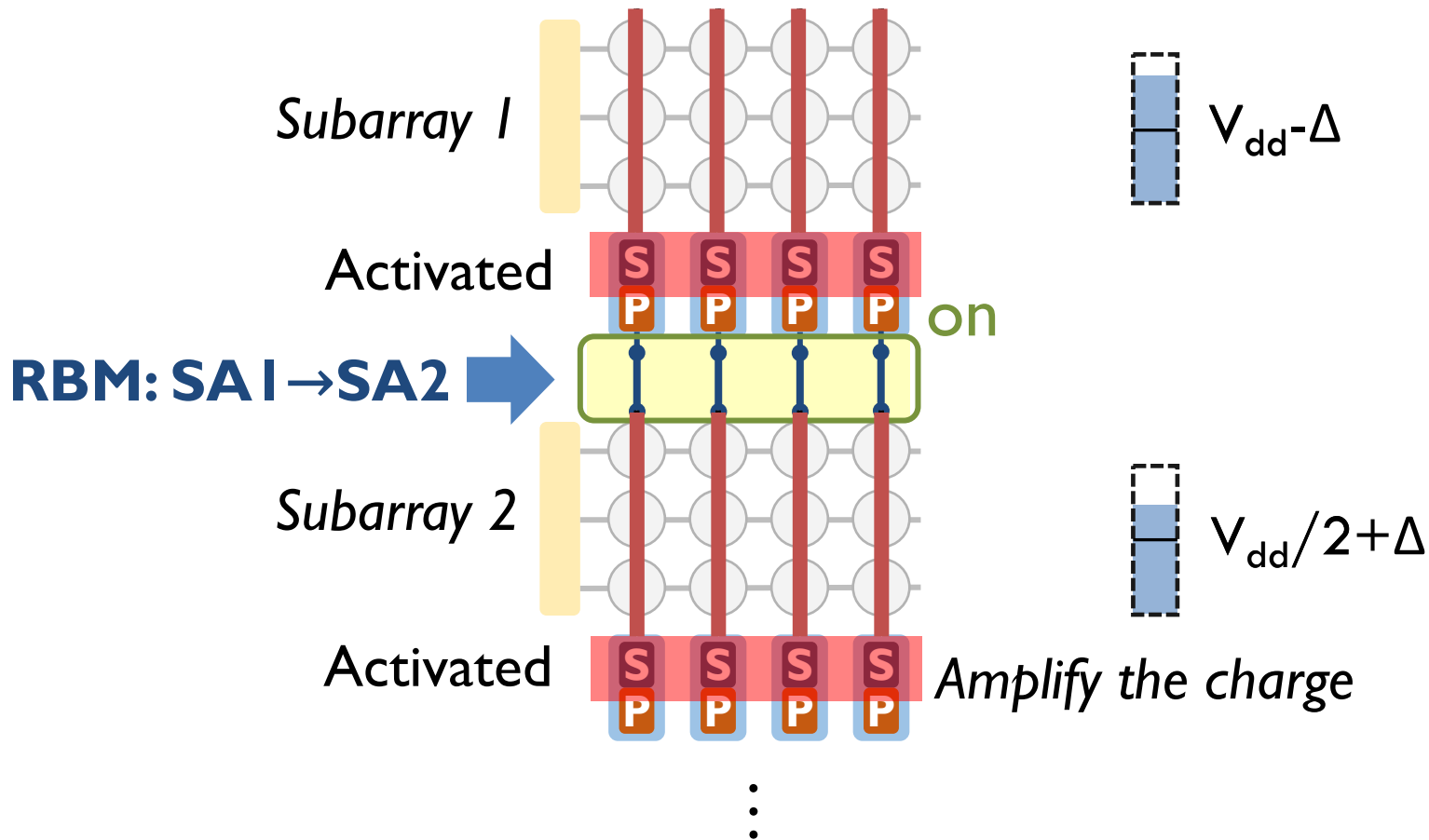
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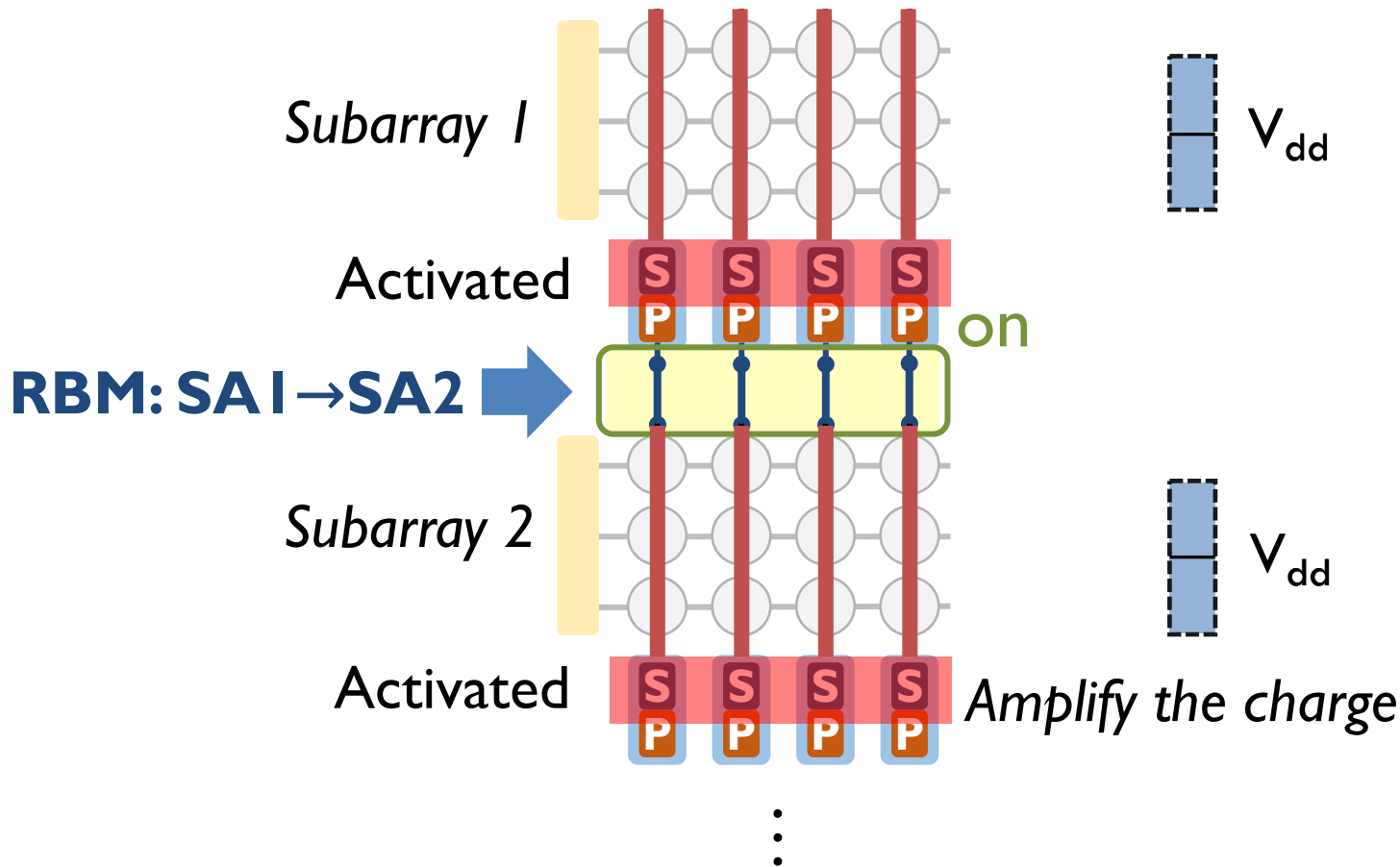
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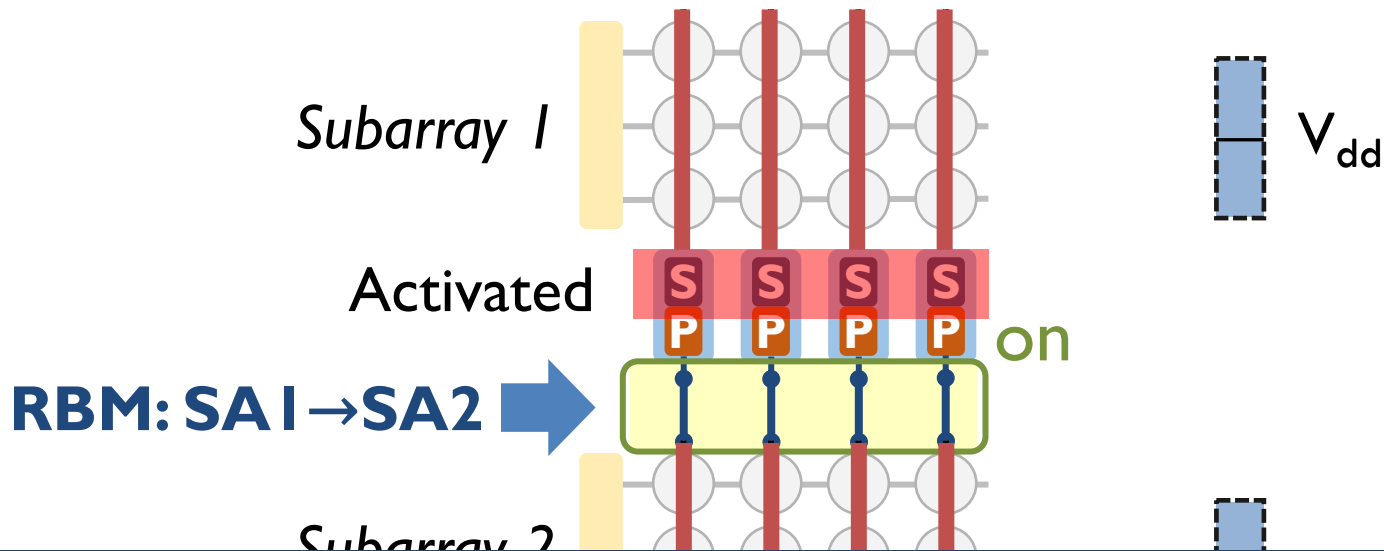
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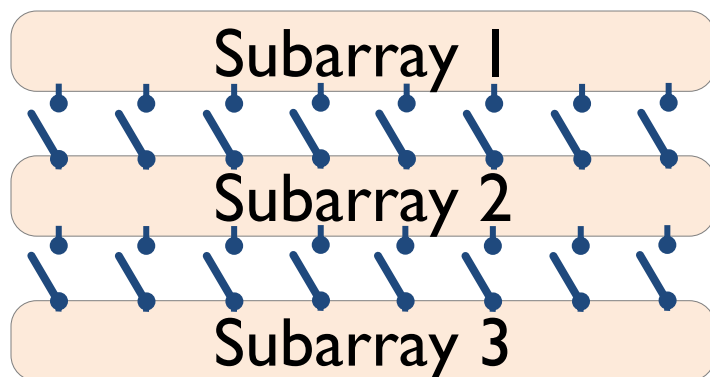
RBM transfers an entire row b/w subarrays

RBM Analysis

- The range of RBM depends on the DRAM design
 - Multiple RBMs to move data across > 3 subarrays

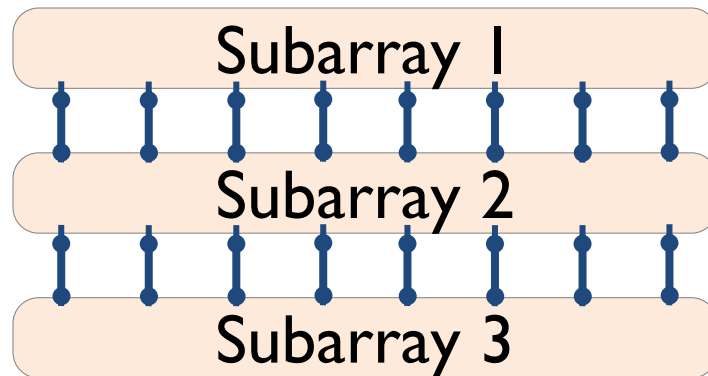
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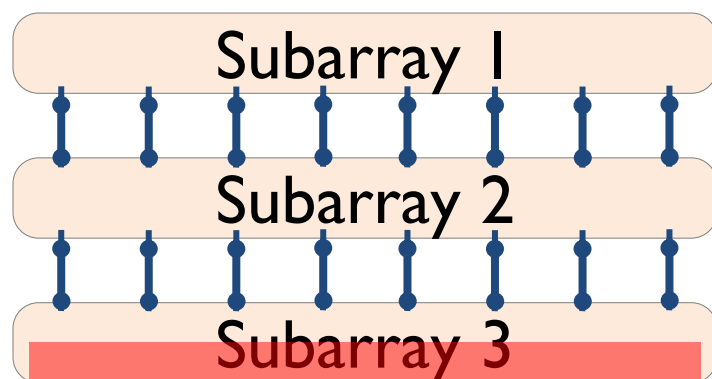
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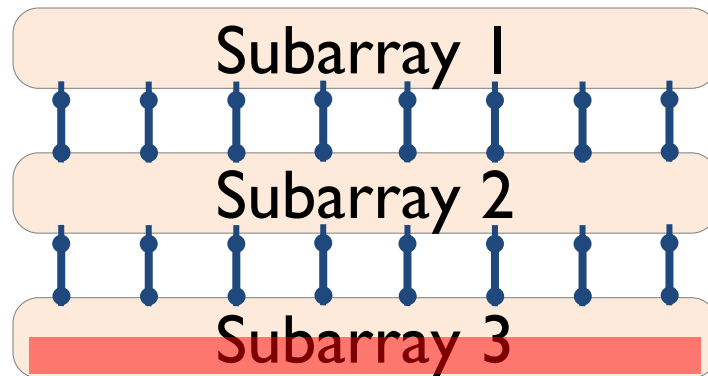
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 - Multiple RBMs to move data across > 3 subarrays



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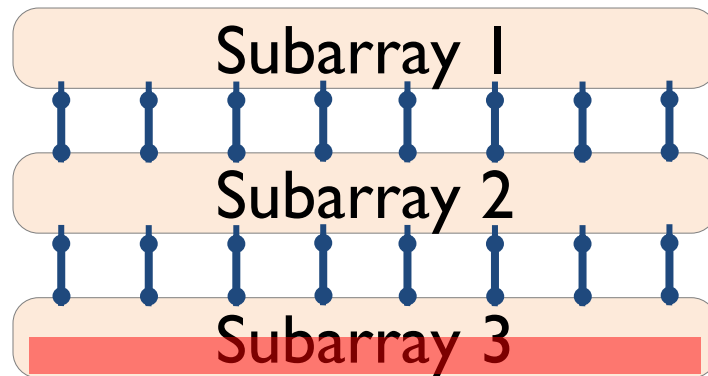
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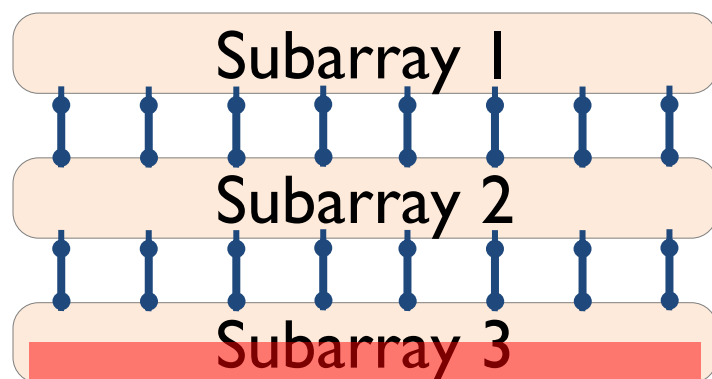
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Outline

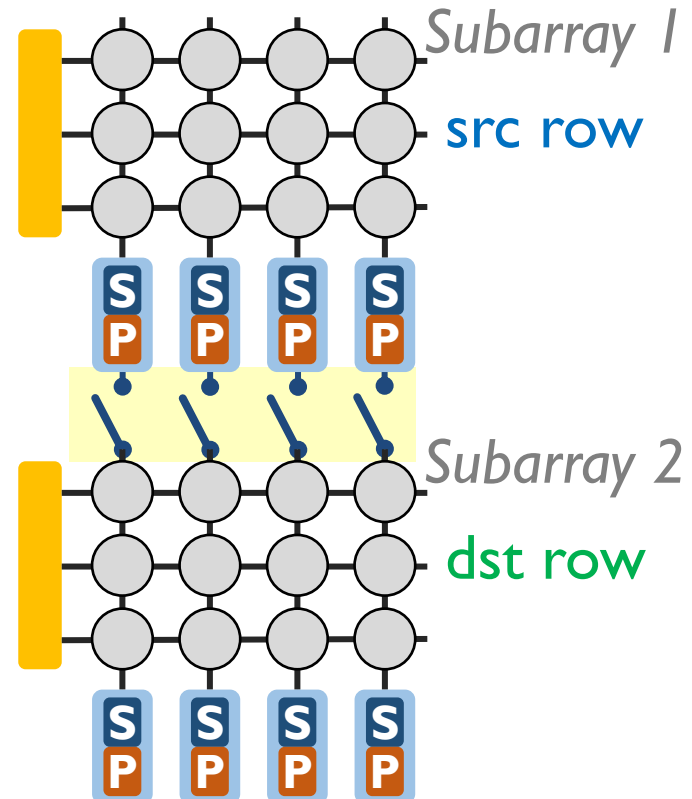
- Motivation and Key Idea
- DRAM Background
- LISA Substrate
 - New DRAM Command to Use LISA
- **Applications of LISA**
 - **1.** Rapid Inter-Subarray Copying (RISC)
 - **2.** Variable Latency DRAM (VILLA)
 - **3.** Linked Precharge (LIP)

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- **Goal:** Efficiently copy a row across subarrays
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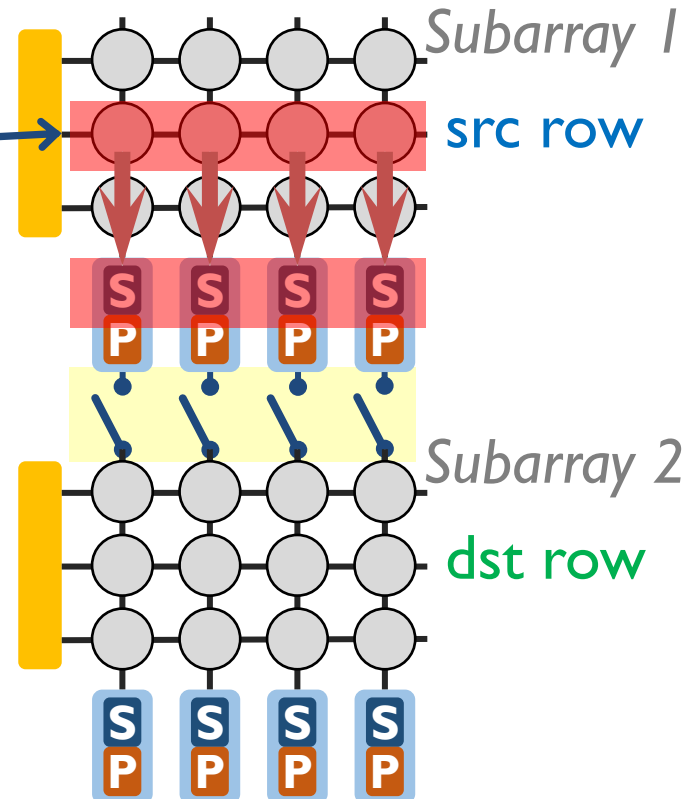
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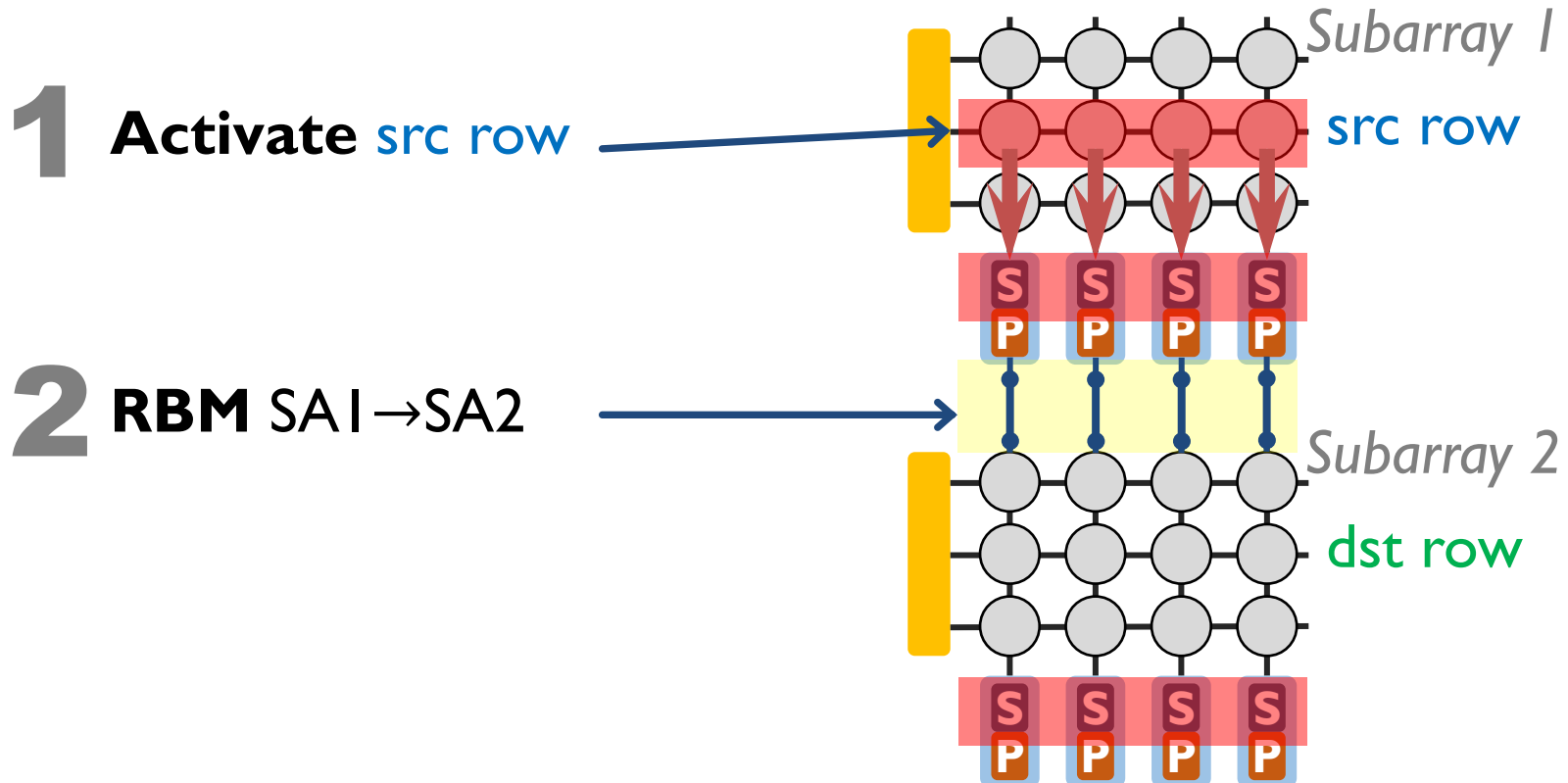
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1 **Activate src row**



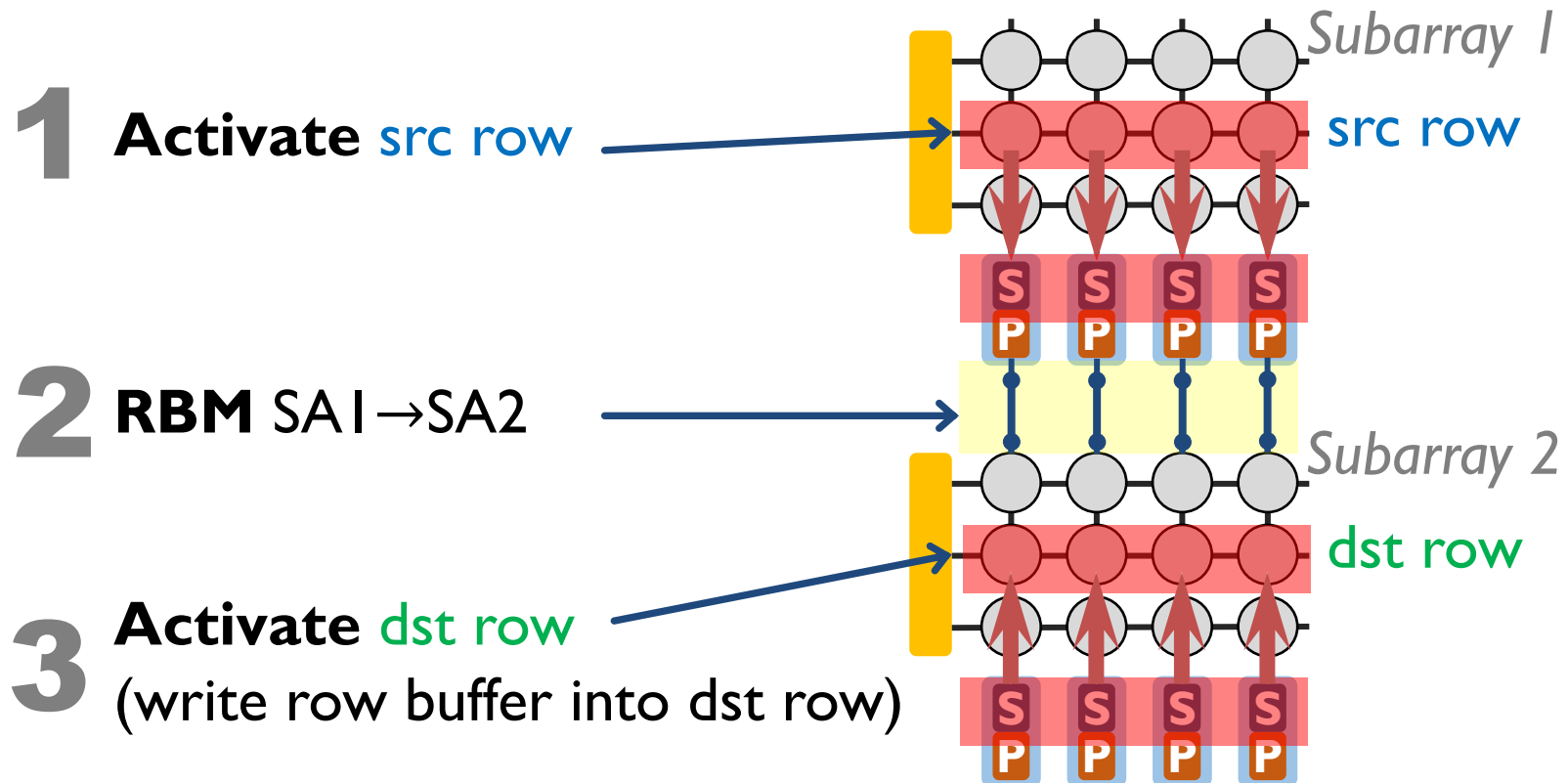
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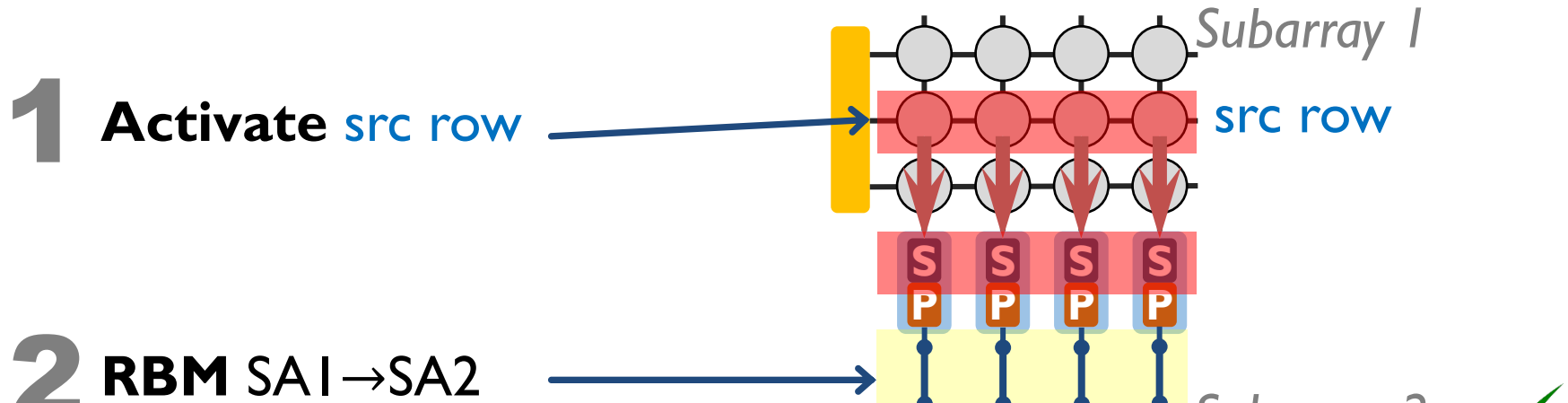
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Reduces row-copy latency by 9.2x,
DRAM energy by 48.1x

Methodology

- Cycle-level simulator: Ramulator [CAL'15]
<https://github.com/CMU-SAFARI/ramulator>
- CPU: **4 out-of-order cores, 4GHz**
- L1: 64KB/core, L2: 512KB/core, L3: shared 4MB
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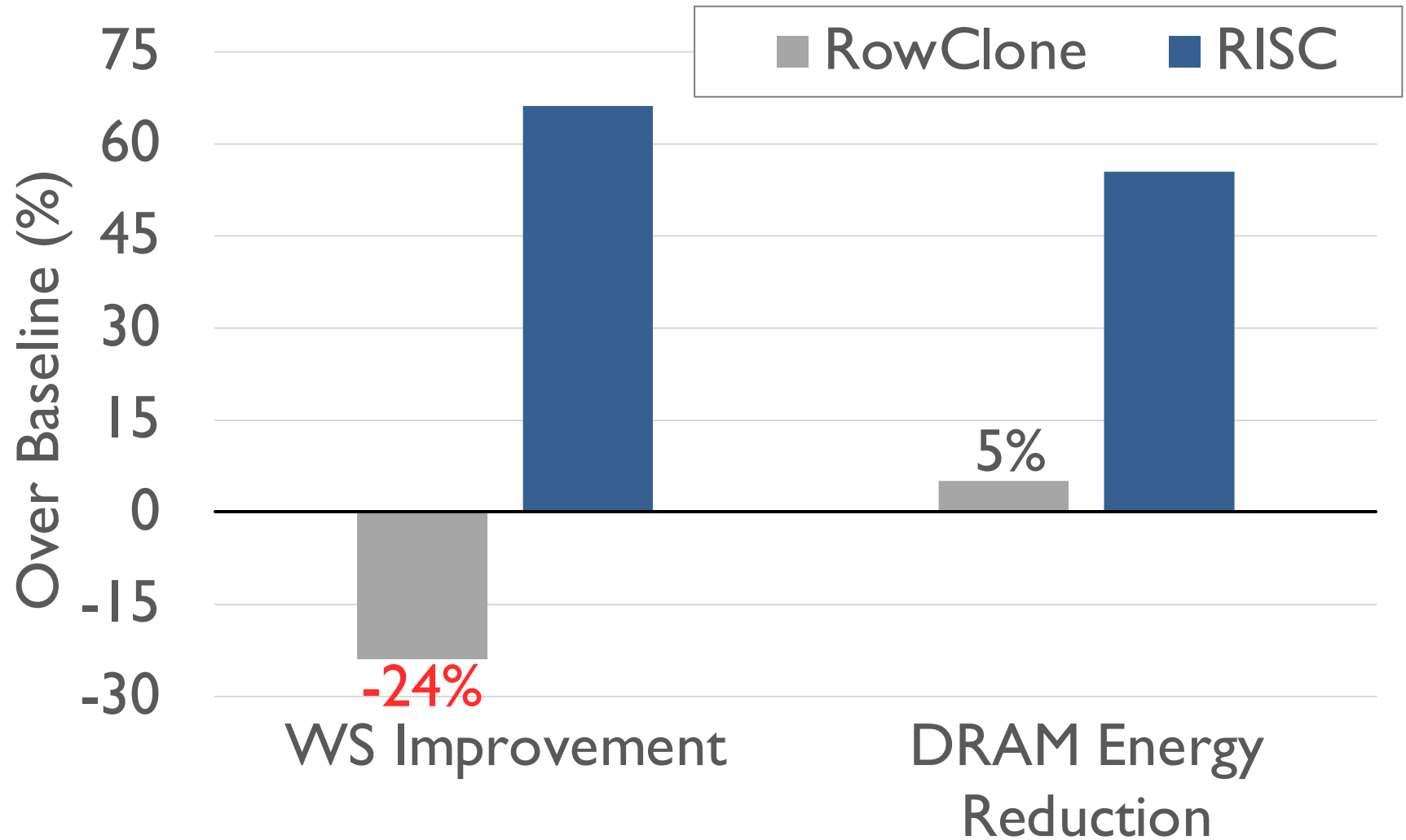
Comparison Points

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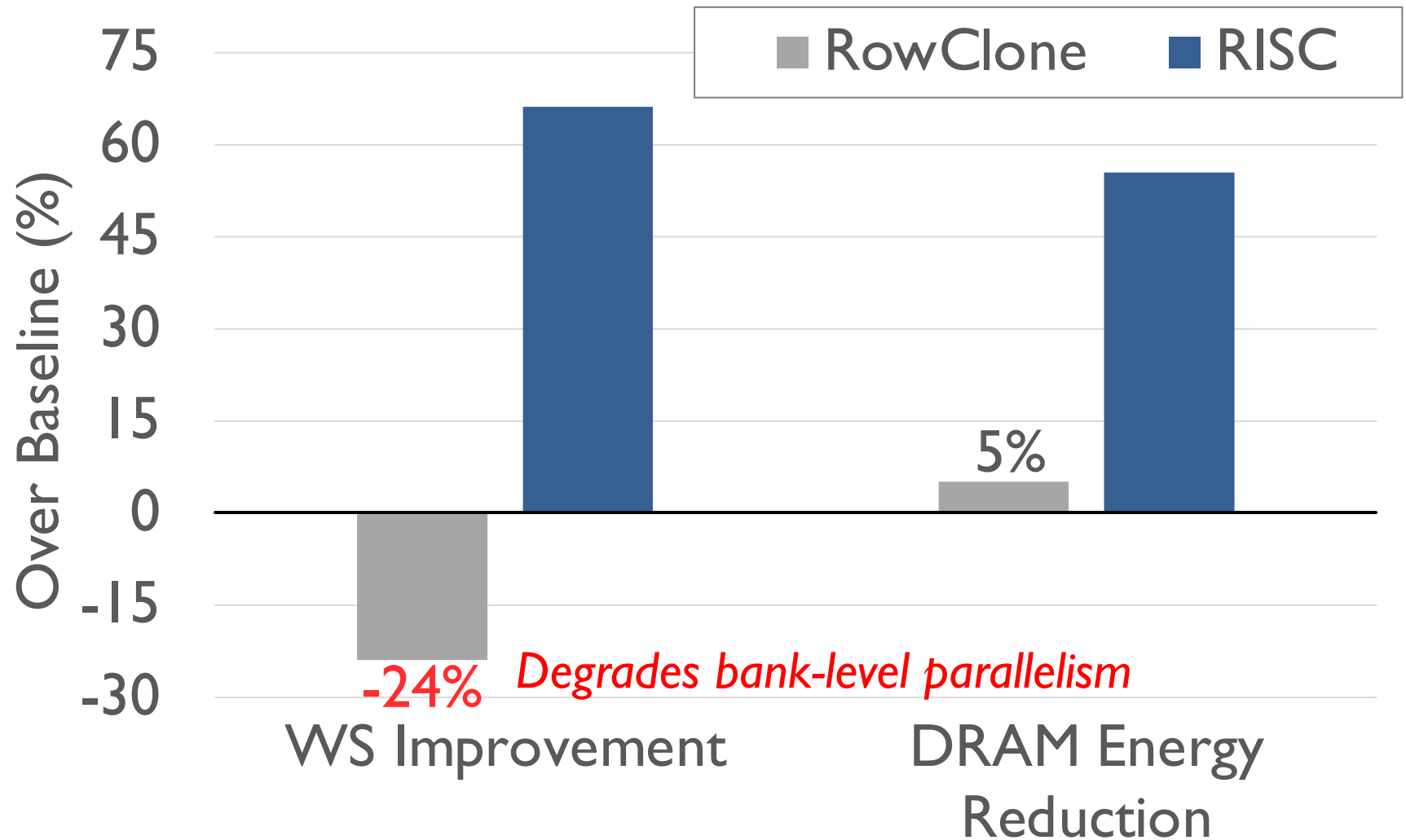
Comparison Points

- **Baseline:** Copy data through CPU (existing systems)
- **RowClone** [Seshadri+ MICRO'13]
 - In-DRAM bulk copy scheme
 - Fast **intra-subarray** copying via bitlines
 - Slow **inter-subarray** copying via internal data bus

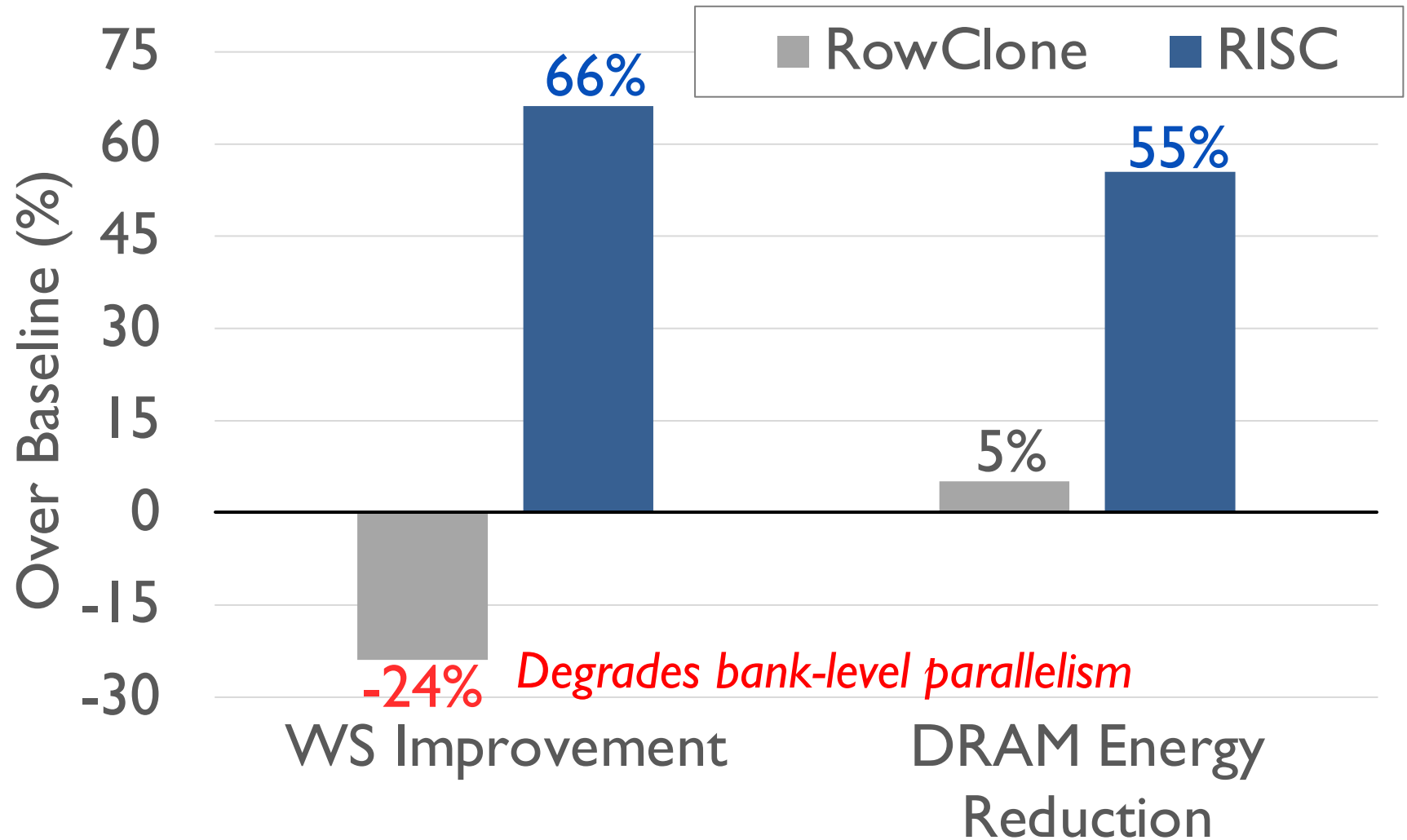
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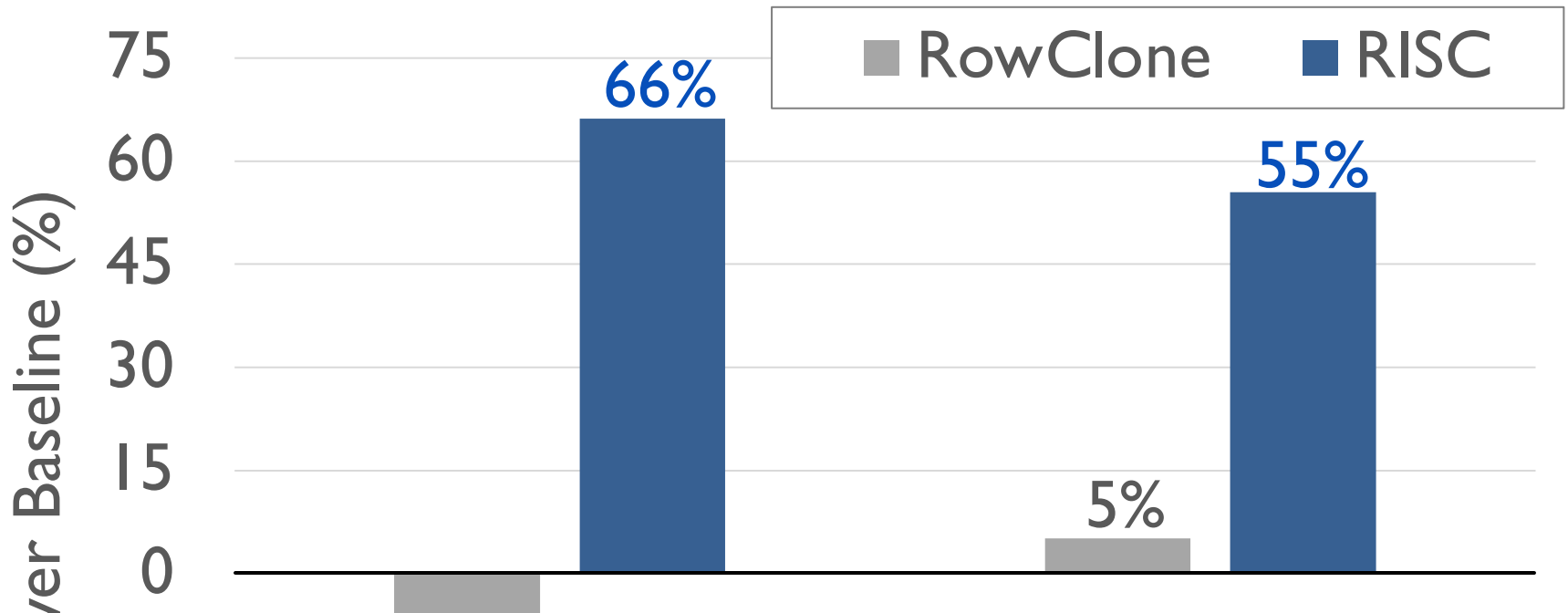
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Rapid Inter-Subarray Copying (RISC) using LISA improves system performance

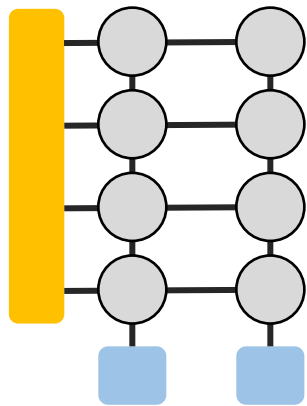
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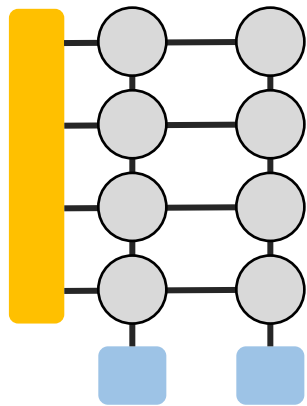
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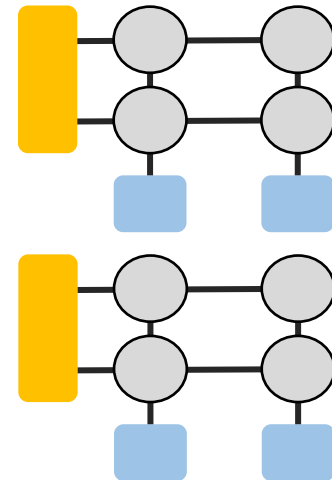
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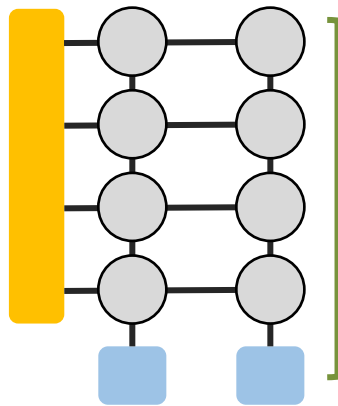
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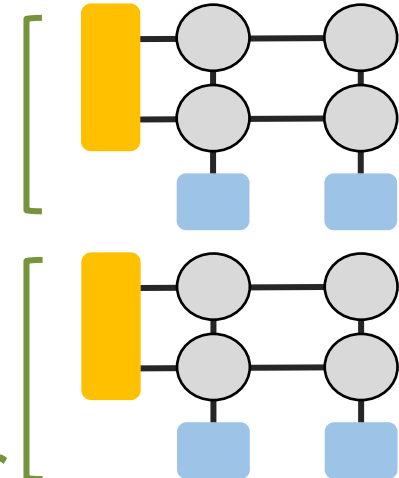
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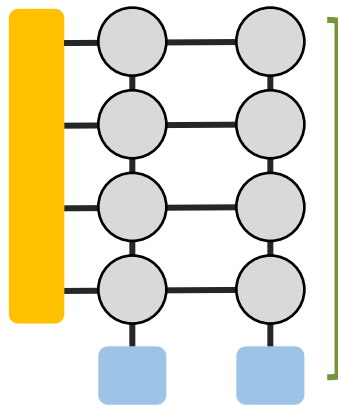


Shorter bitlines → faster
activate and **precharge** time

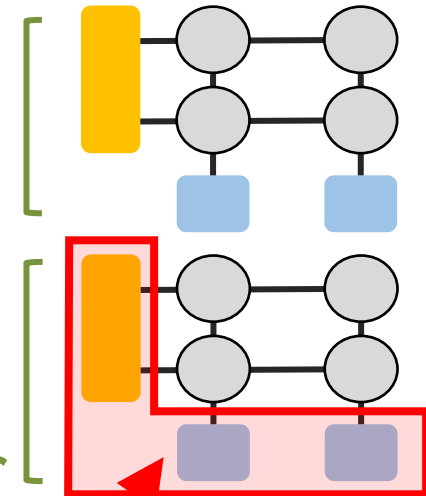
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High area overhead: >40%

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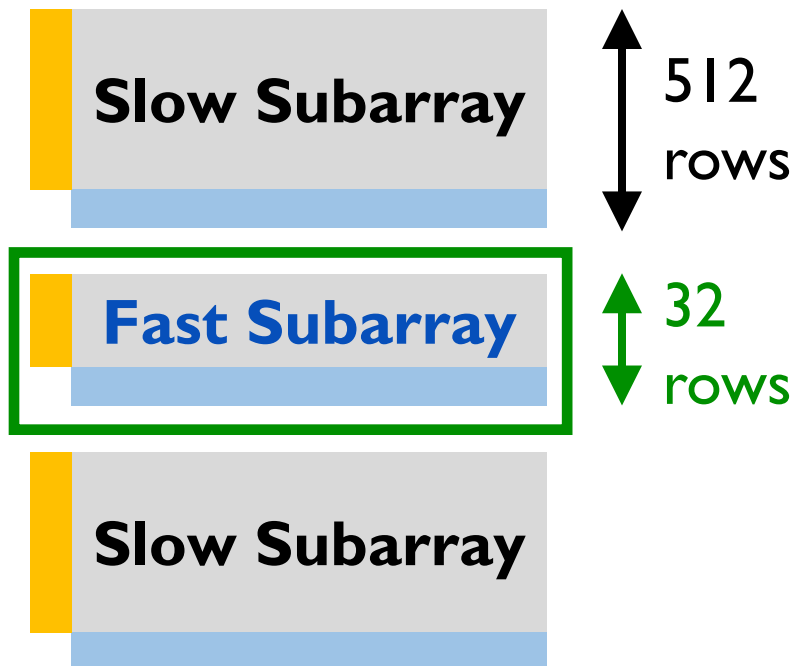
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Slow Subarray

The diagram shows a gray rectangular block representing a slow subarray. It has a yellow vertical bar on its left side and a light blue horizontal bar at its bottom.

Challenge: VILLA cache requires frequent movement of data rows



Fast Subarray

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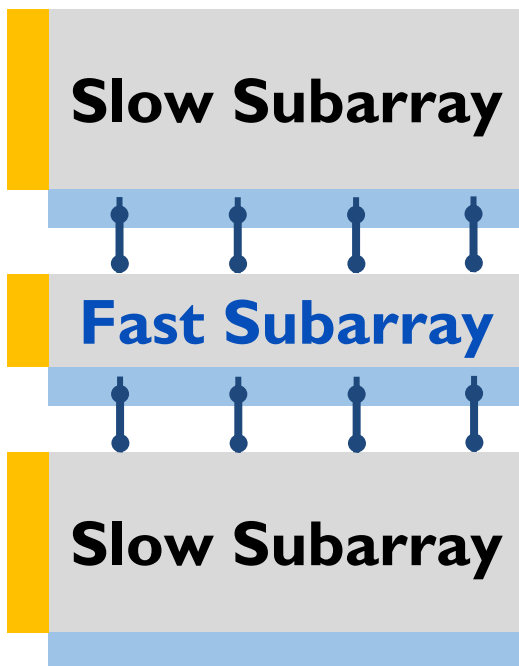


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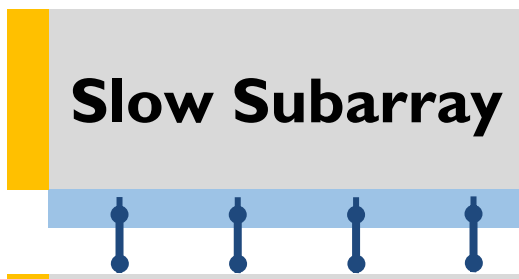


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LISA: Cache rows rapidly from slow to fast subarrays

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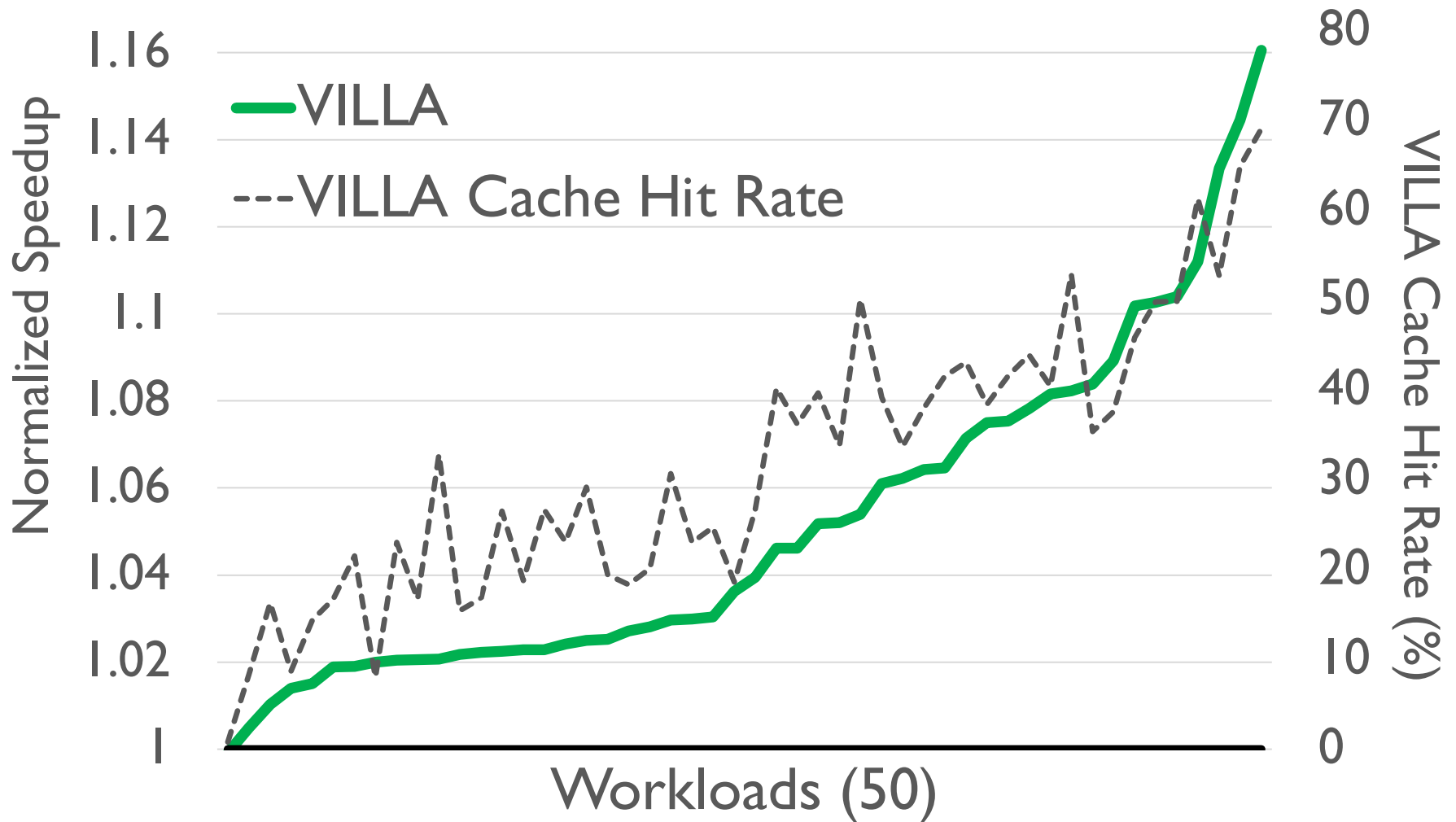


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Reduces hot data access latency by 2.2x
at only 1.6% area overhead

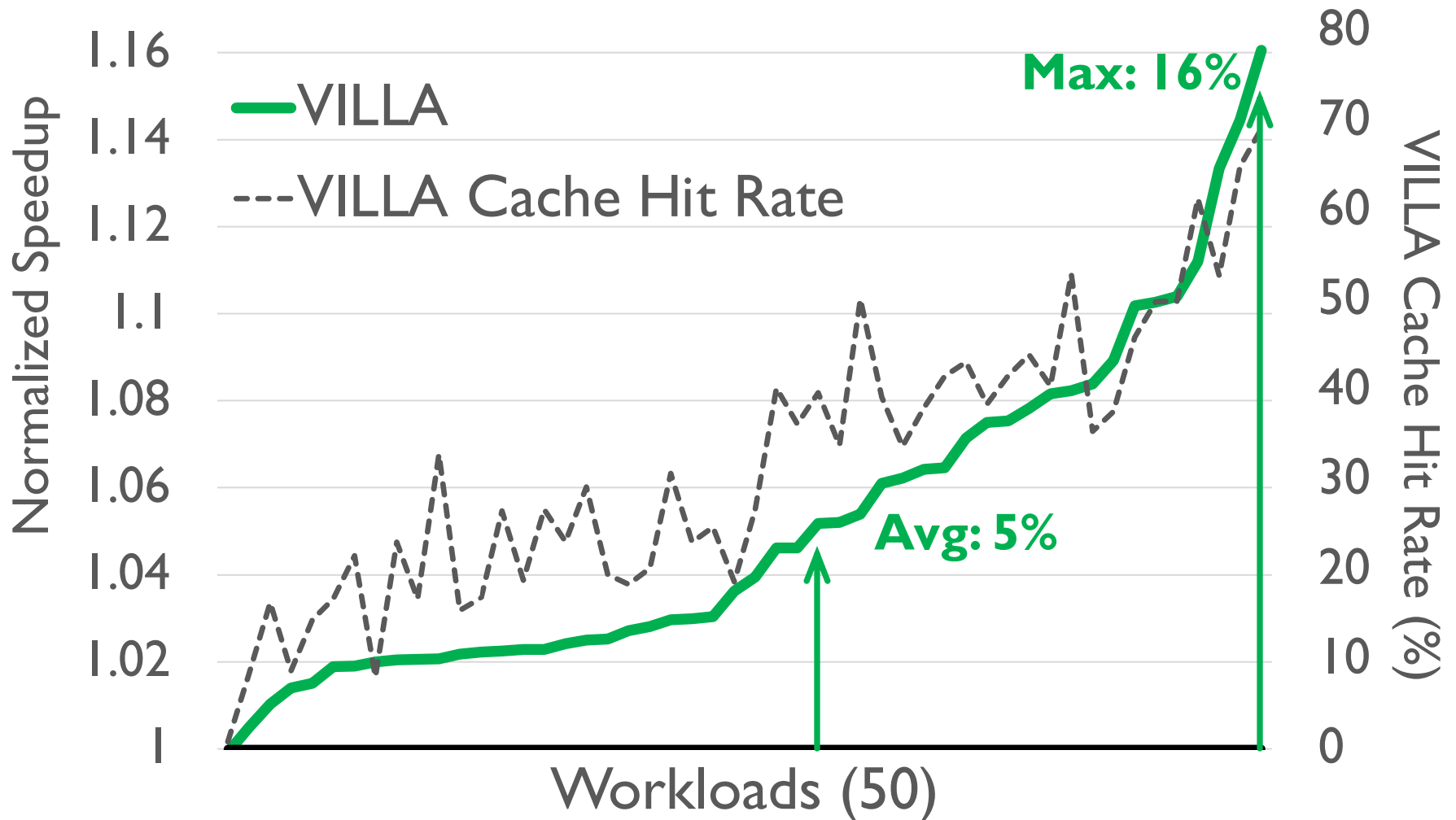
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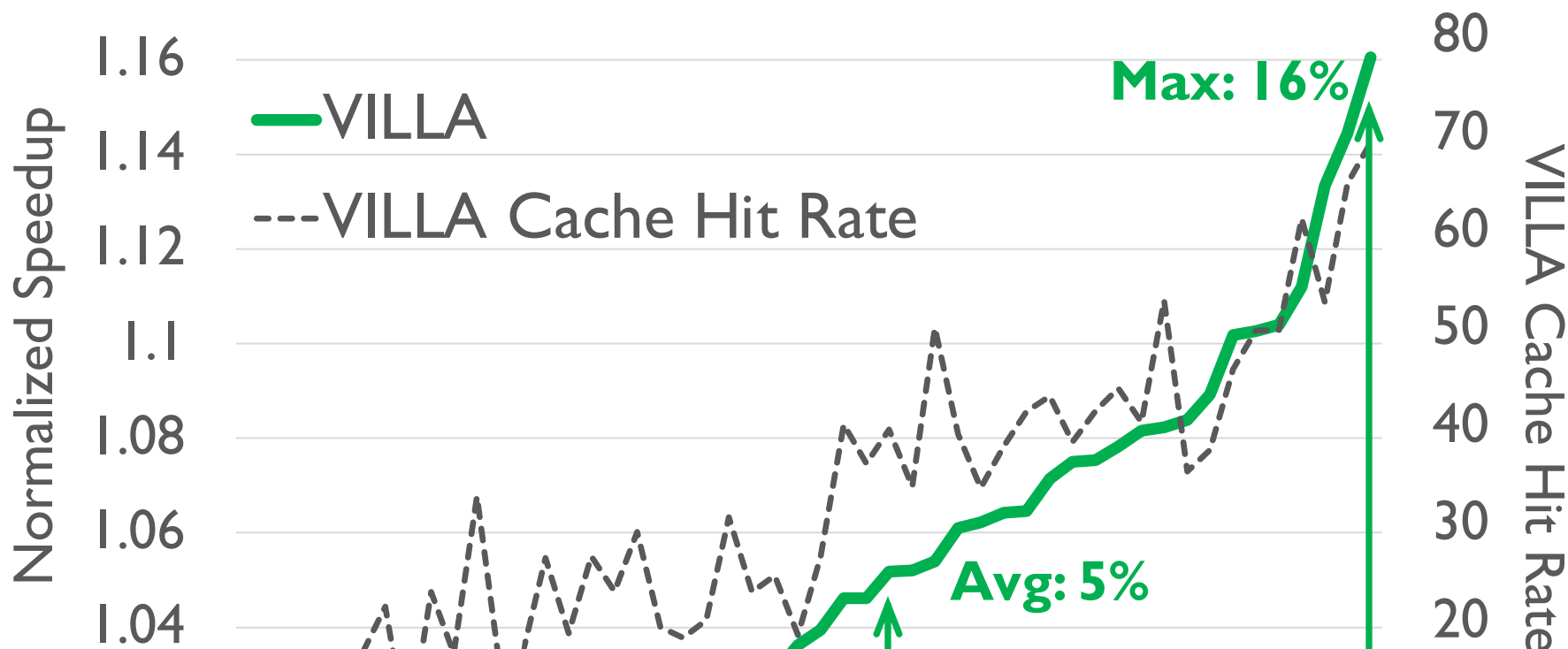
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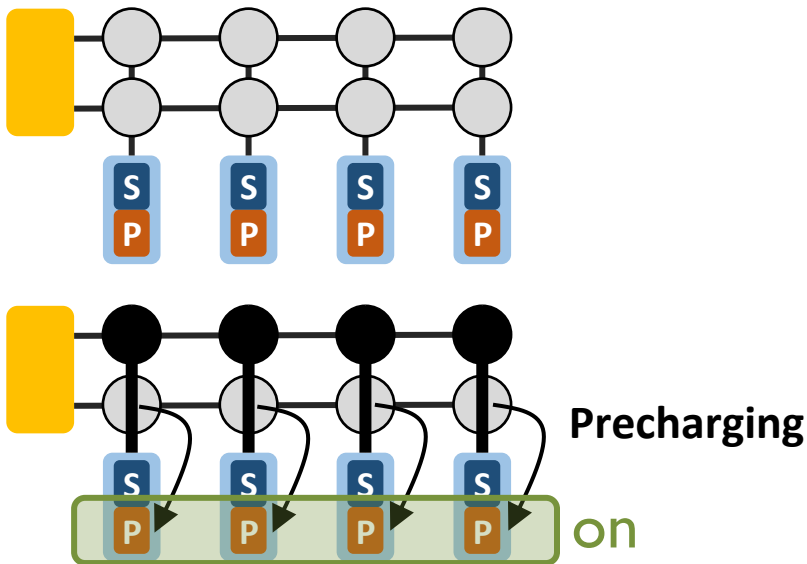
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Caching hot data in DRAM using LISA improves system performance

3. Linked Precharge (LIP)

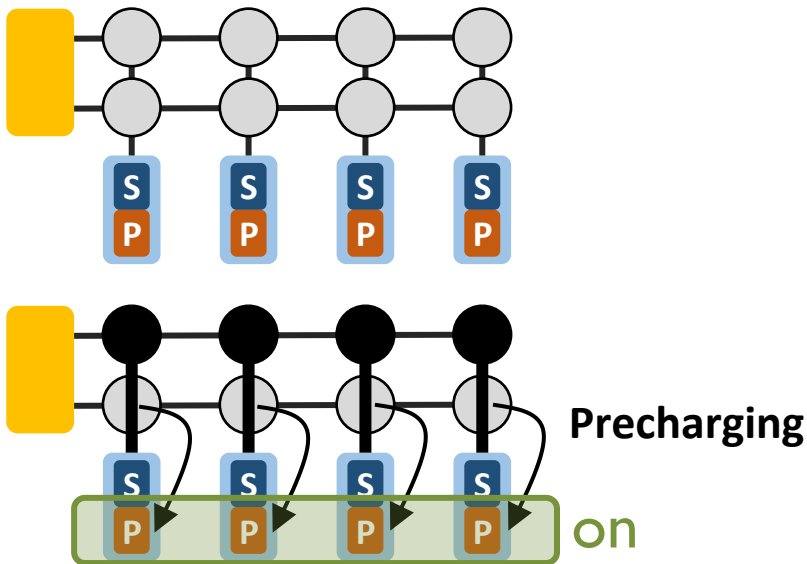
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Conventional DRAM

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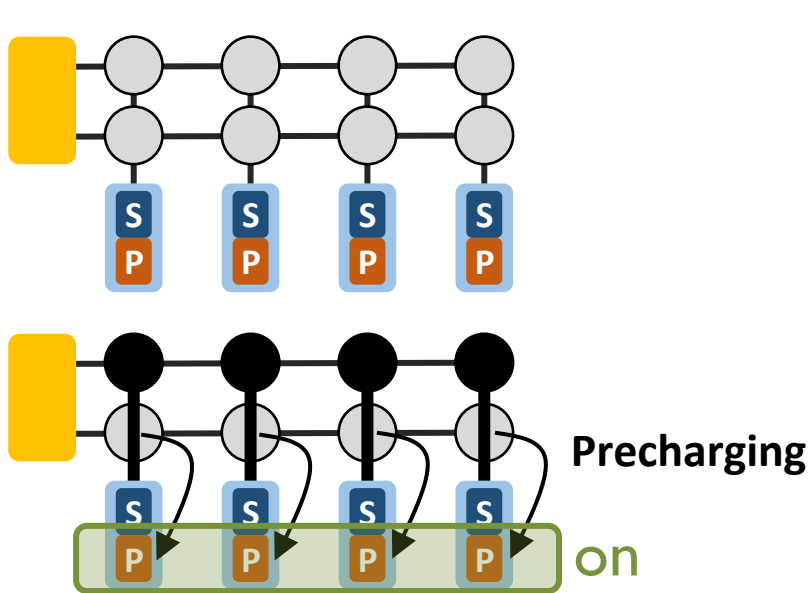
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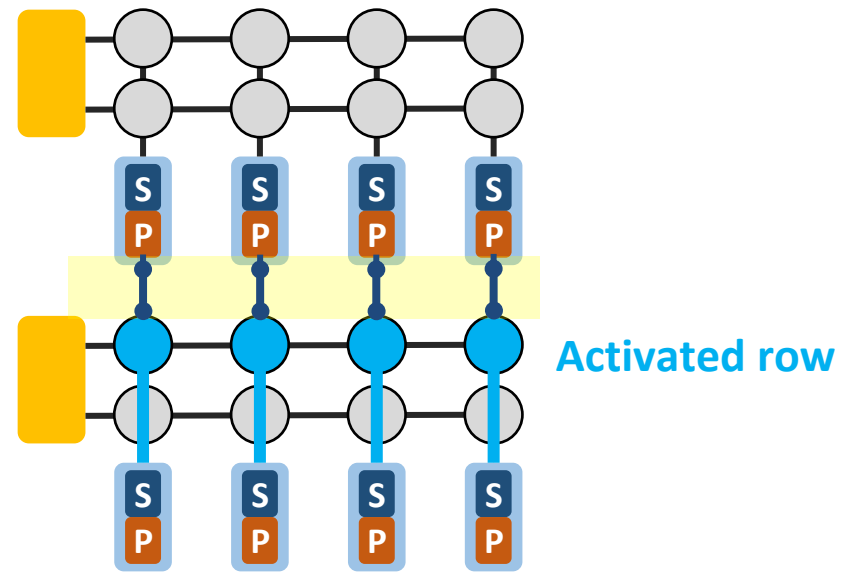
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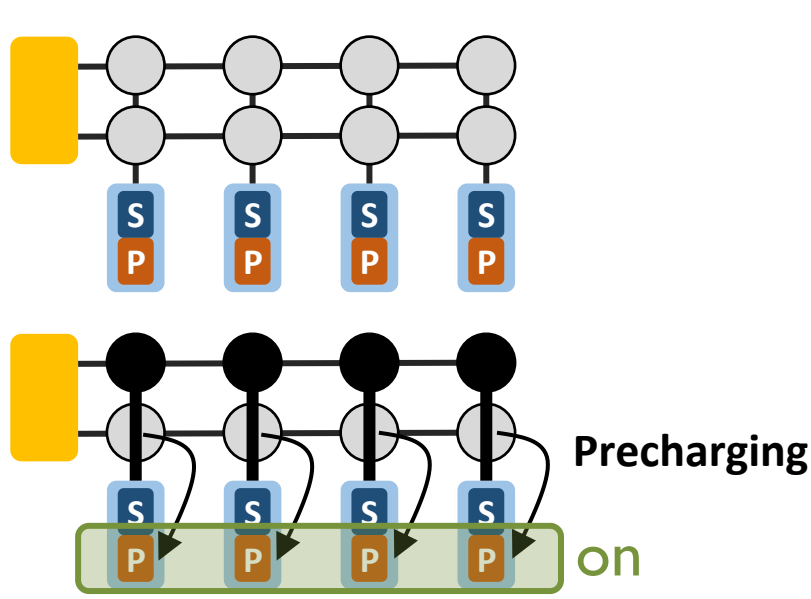
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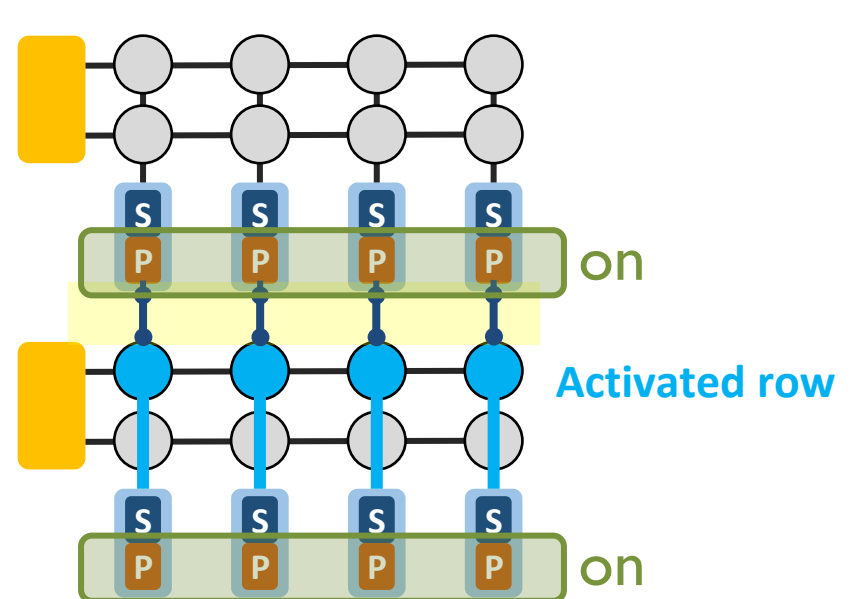
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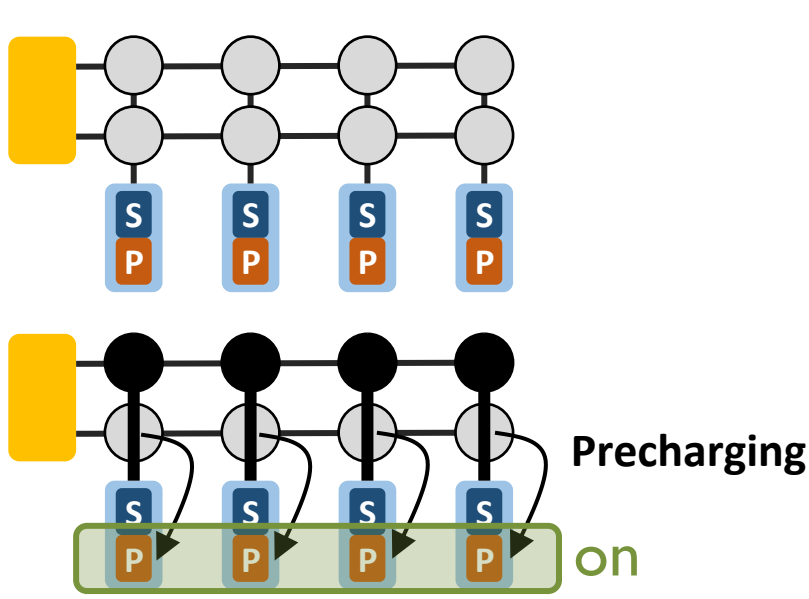
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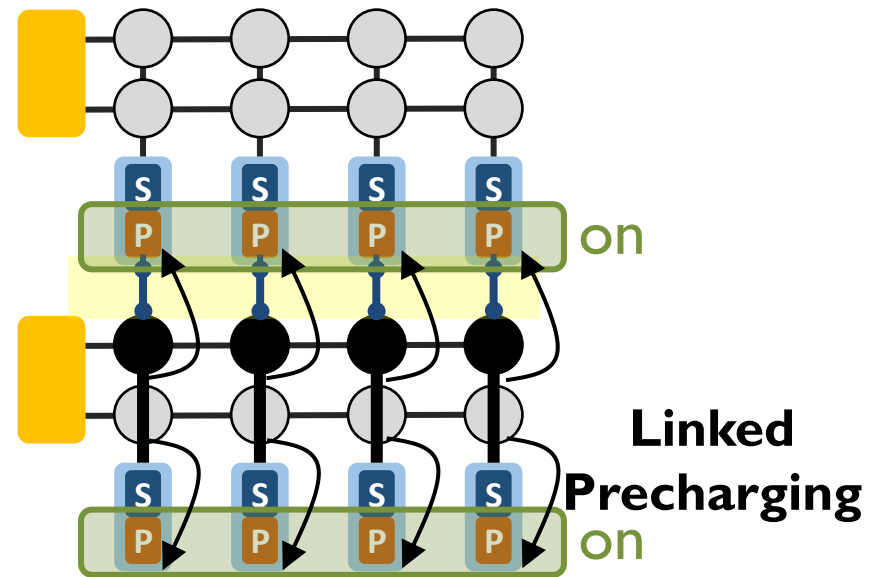
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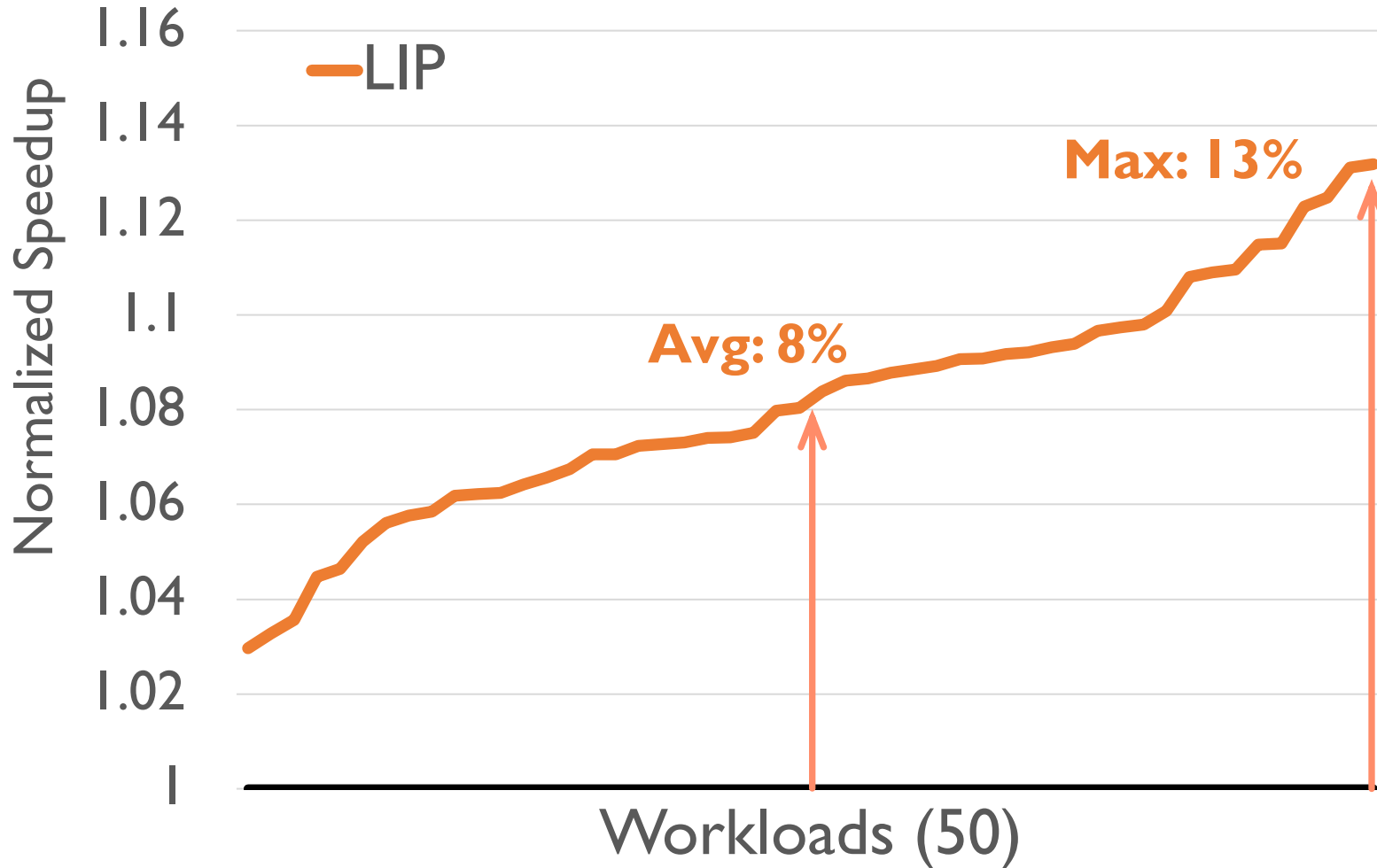
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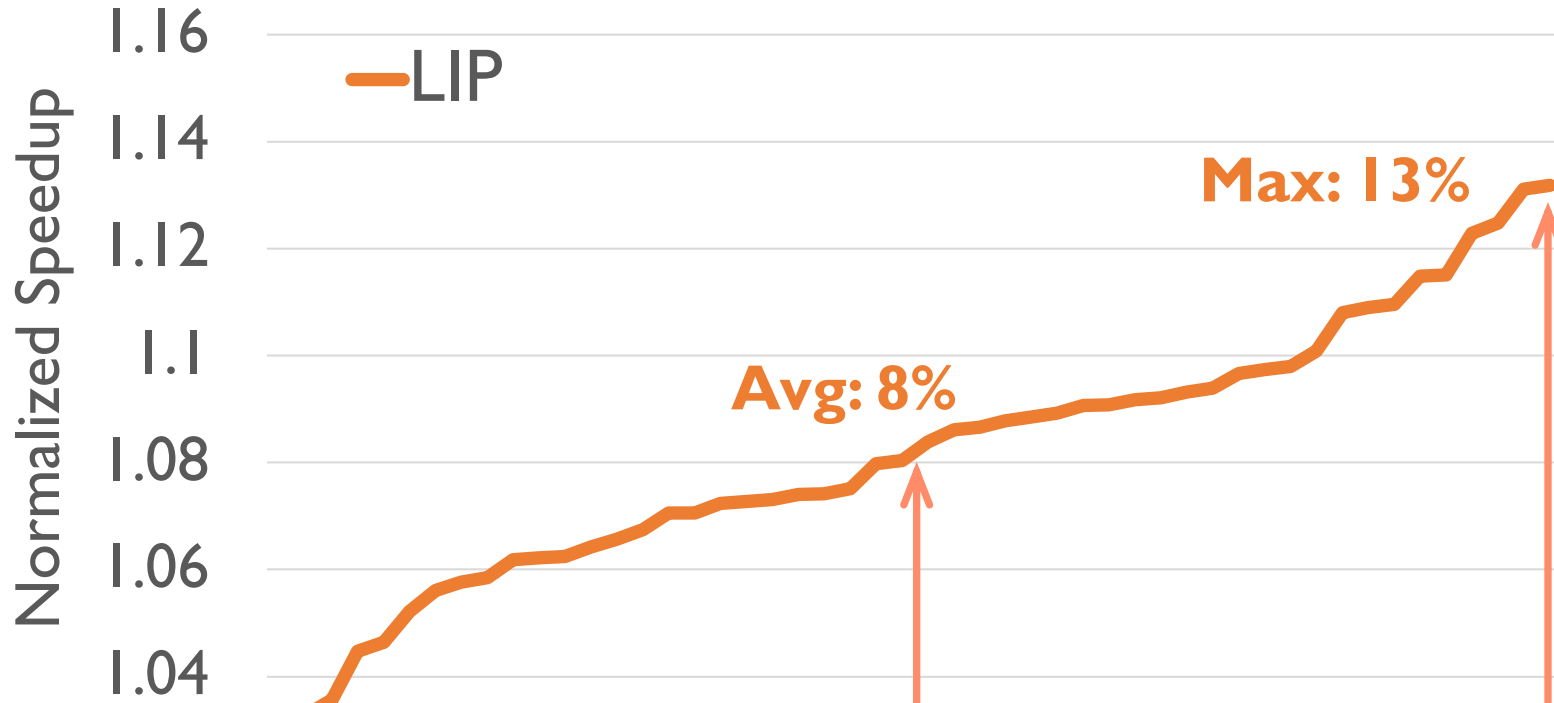
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Accelerating precharge using LISA improves system performance

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- Source code will be available in April
<https://github.com/CMU-SAFARI>

Low-Cost Inter-Linked Subarrays (LISA)

Enabling Fast Inter-Subarray Data Movement in DRAM

Kevin Chang

Prashant Nair, Donghyuk Lee, Saugata Ghose,
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SAFARI
CARET

Carnegie Mellon

**Georgia
Tech** 