REDUCING REFRESH POWER IN MOBILE DEVICES WITH MORPHABLE ECC

DSN-45
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GROWING DRAM SIZE IN SMARTPHONES

Smartphone usability: battery life

courtesy: Samsung

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Smartphone usability: battery life

30% energy goes to memory system in idle mode

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Samsung Galaxy S2 (2011)
1GB DRAM

Samsung Galaxy S6 (2015)
3GB DRAM

courtesy: Samsung

GROWING DRAM SIZE IN SMARTPHONES

Smartphone usability: battery life

30% energy goes to memory system in idle mode

Samsung Galaxy S2 (2011)
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Samsung Galaxy S6 (2015)
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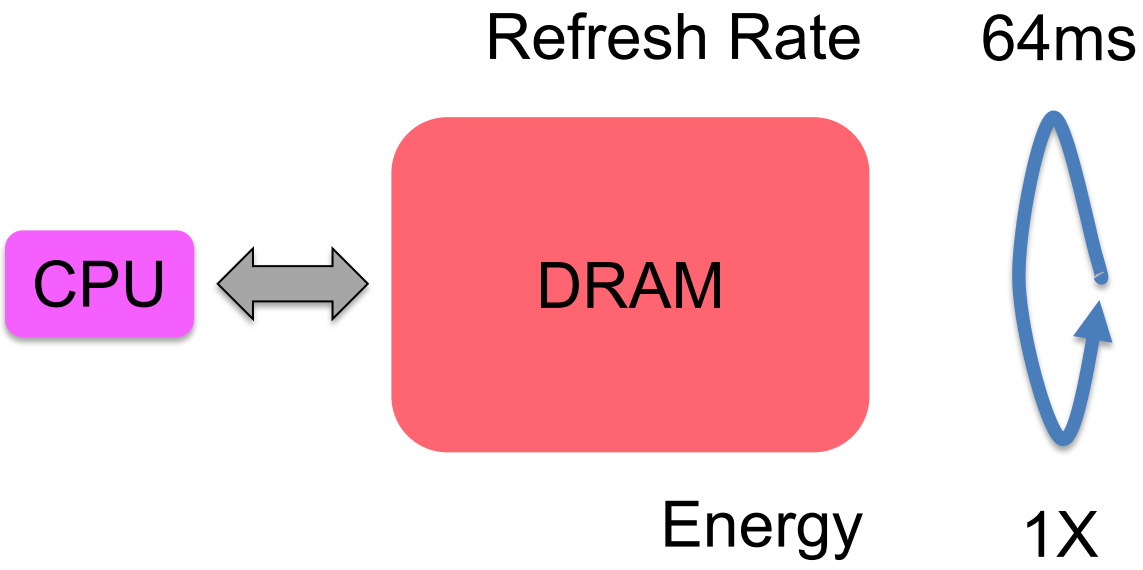
DRAM Refresh accounts for significant energy consumption in idle mode

courtesy: Samsung

LOWER REFRESH RATE FOR ENERGY

Current standard refresh rate: 64ms



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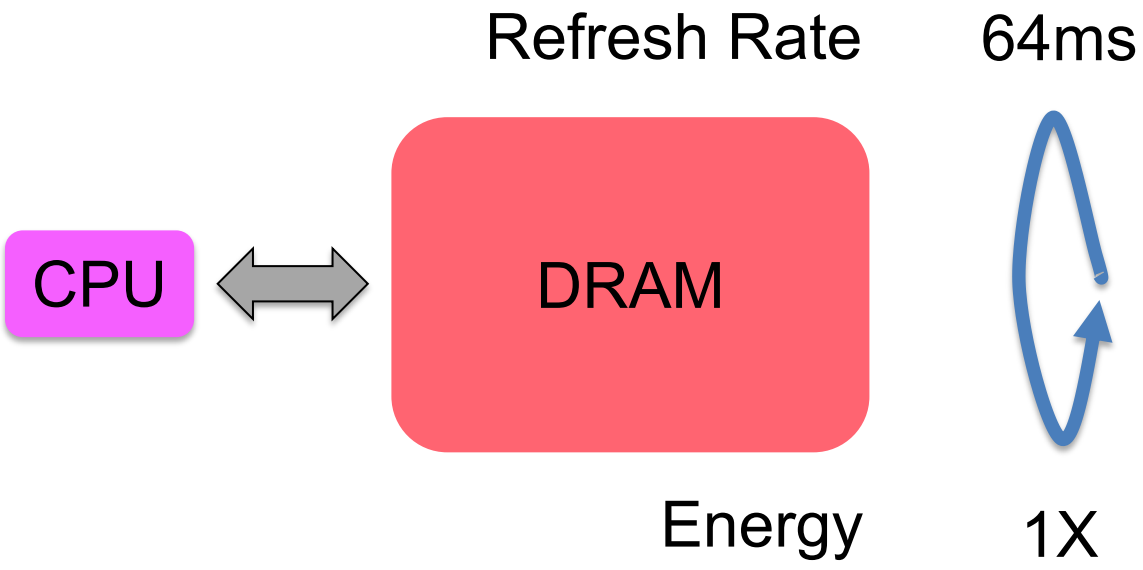

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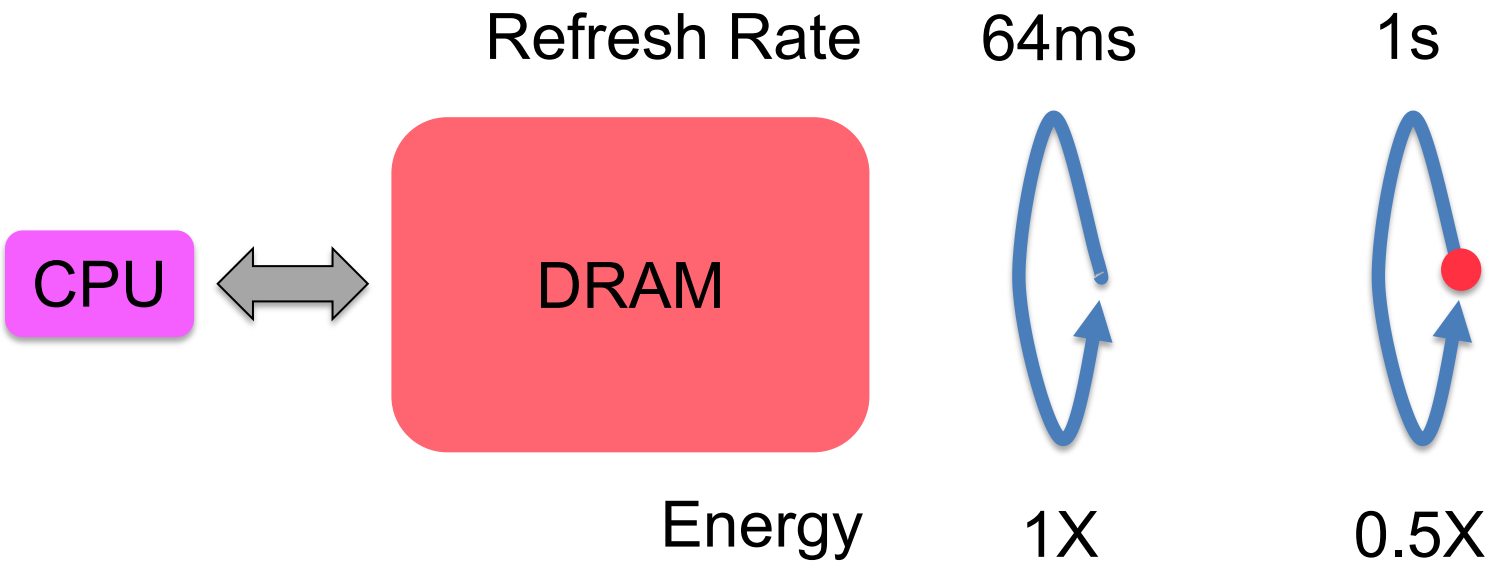

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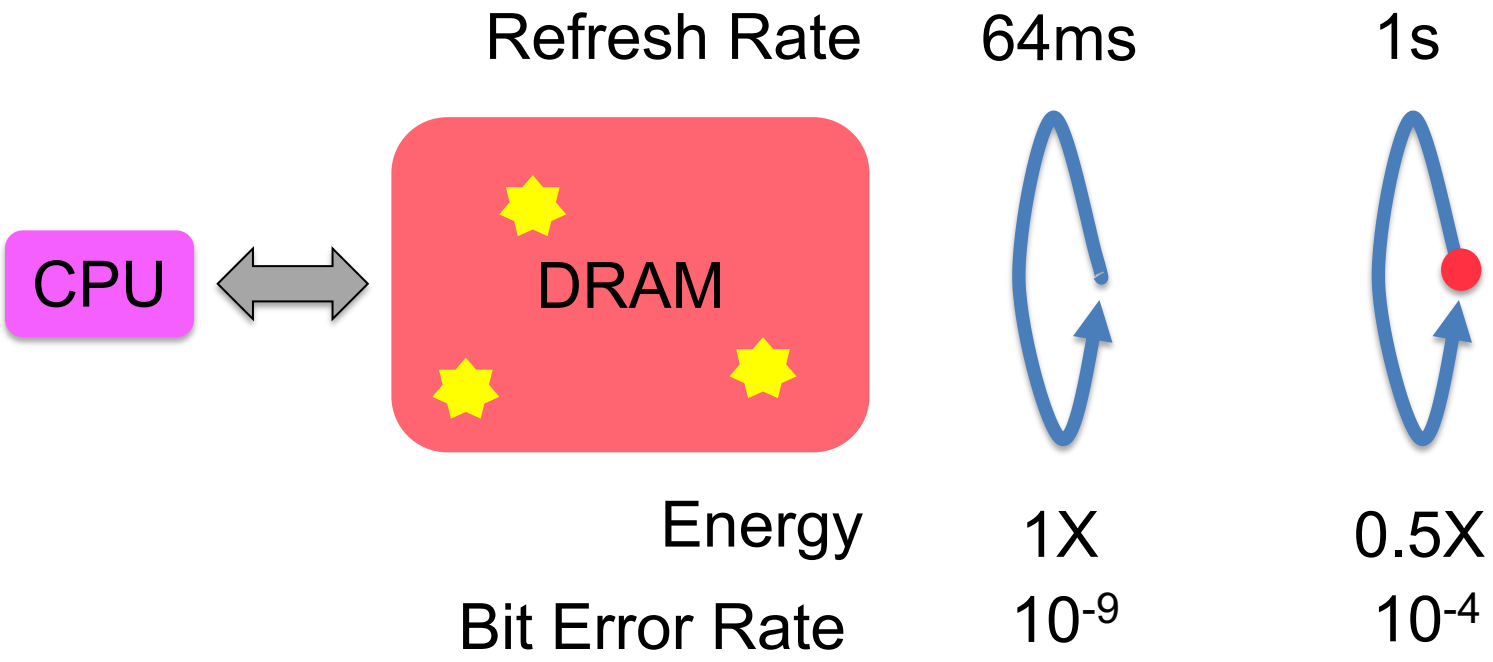

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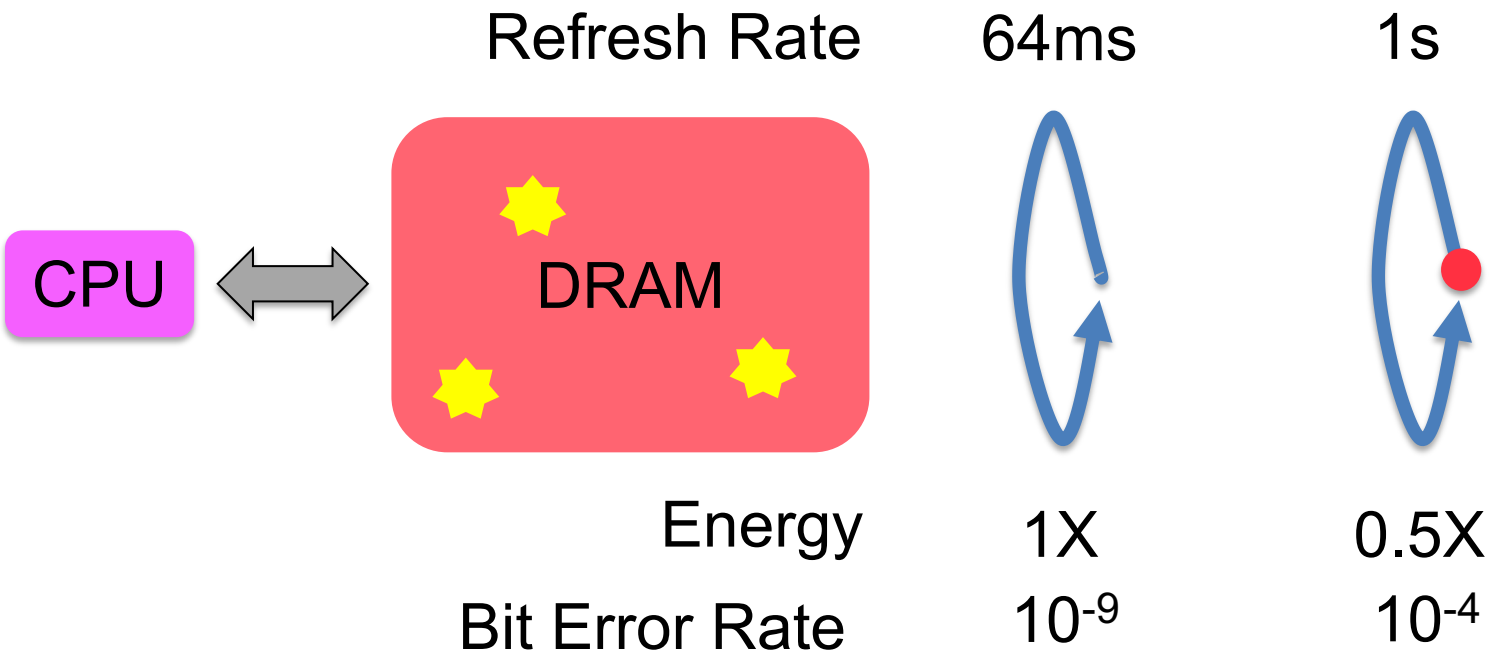
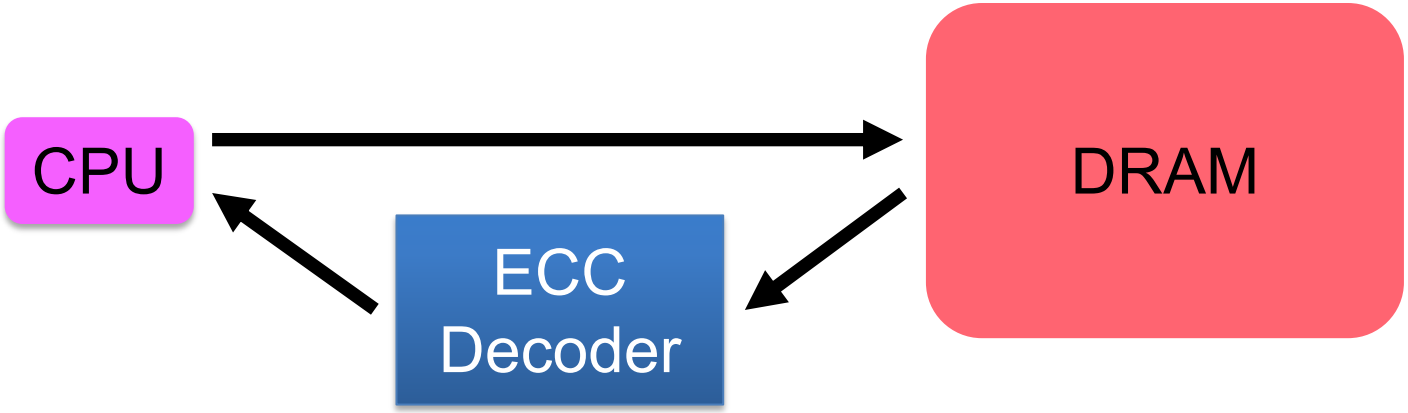


Use ECC to protect DRAM from refresh errors

ECC-6 INCURS LONG LATENCY FOR READ

Decoder latency is on the critical path



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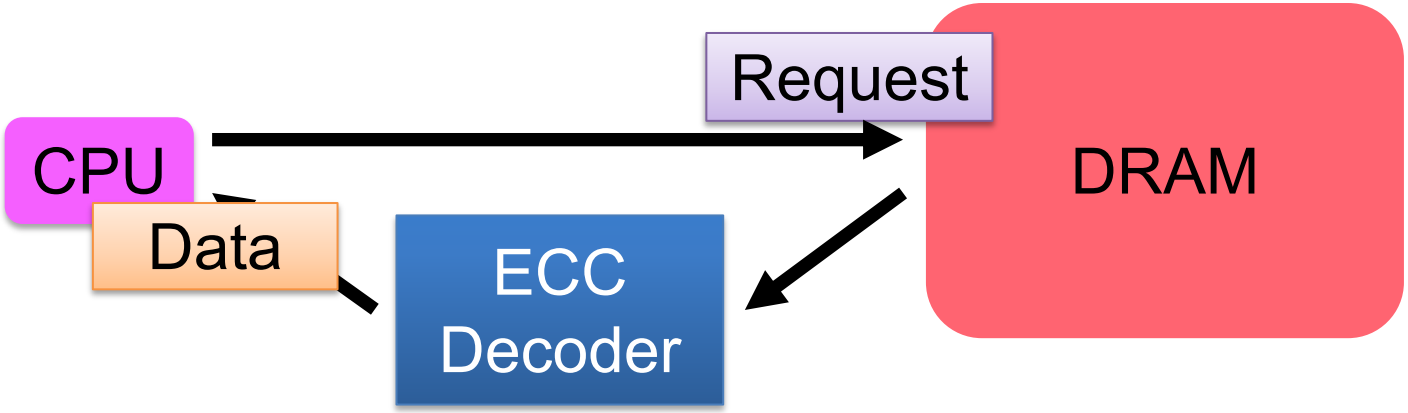

ECC-6: 30 cycles

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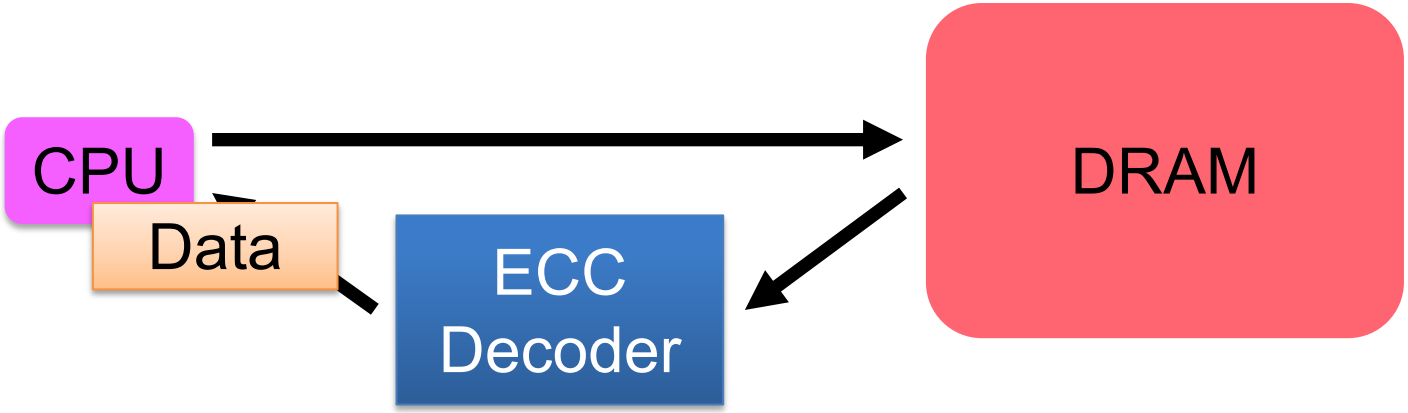


ECC-6: 30 cycles

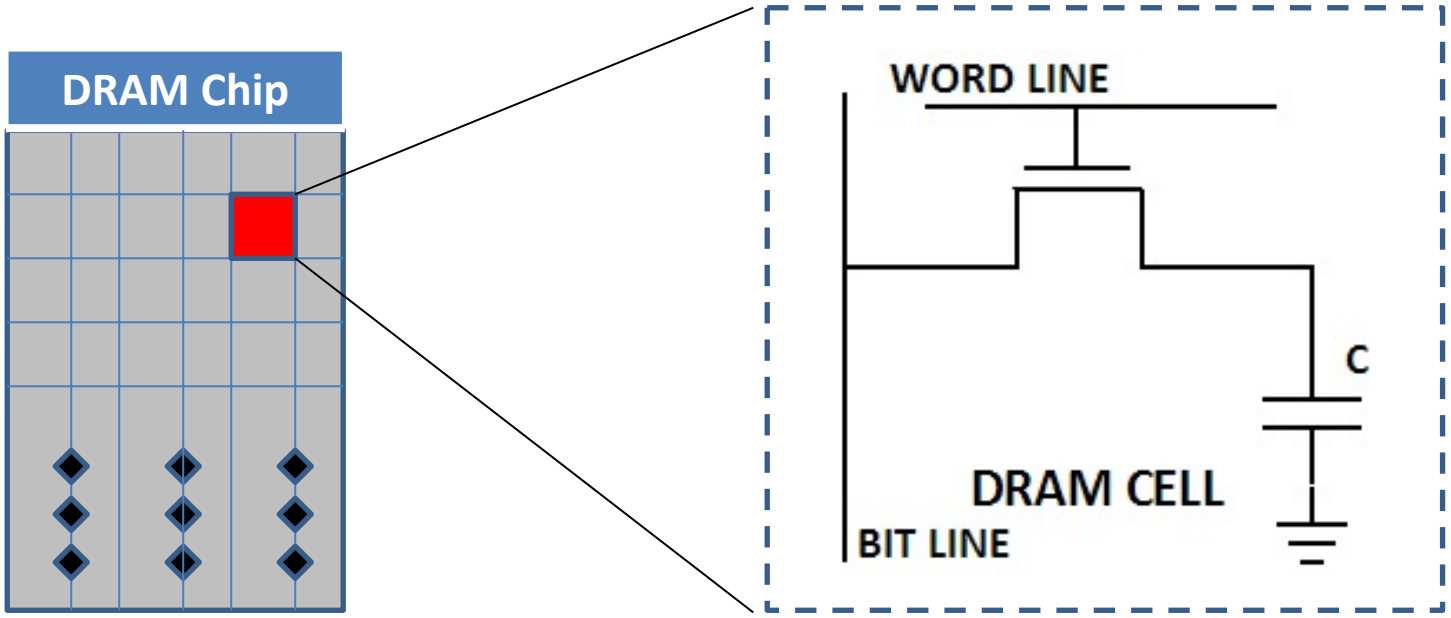
We want energy reduction in idle mode, and maintain performance in active mode

AGENDA

- Introduction
- **Background**
  - DRAM 101
  - Refresh and Errors
  - Error Correction Codes (ECC)
- Morphable ECC
- Results
- Summary

DRAM 101

- Dynamic Random Access Memory (DRAM)
- DRAM stores data as charge on capacitor



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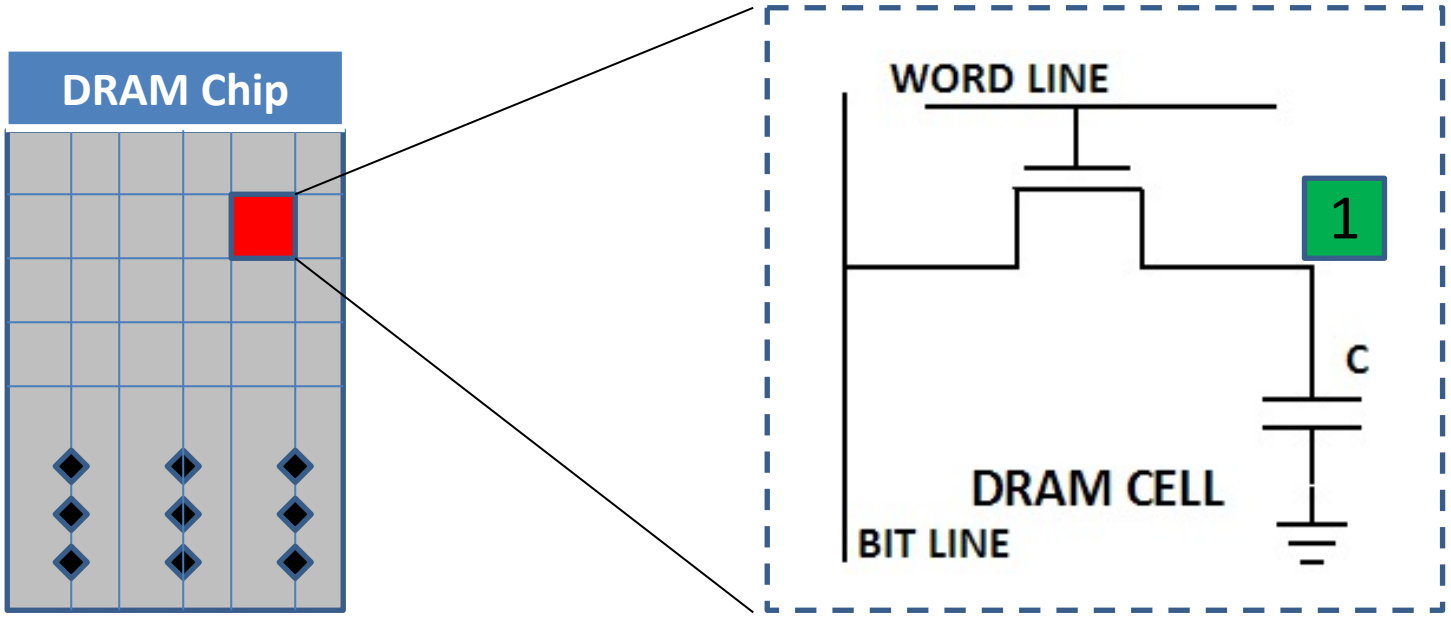

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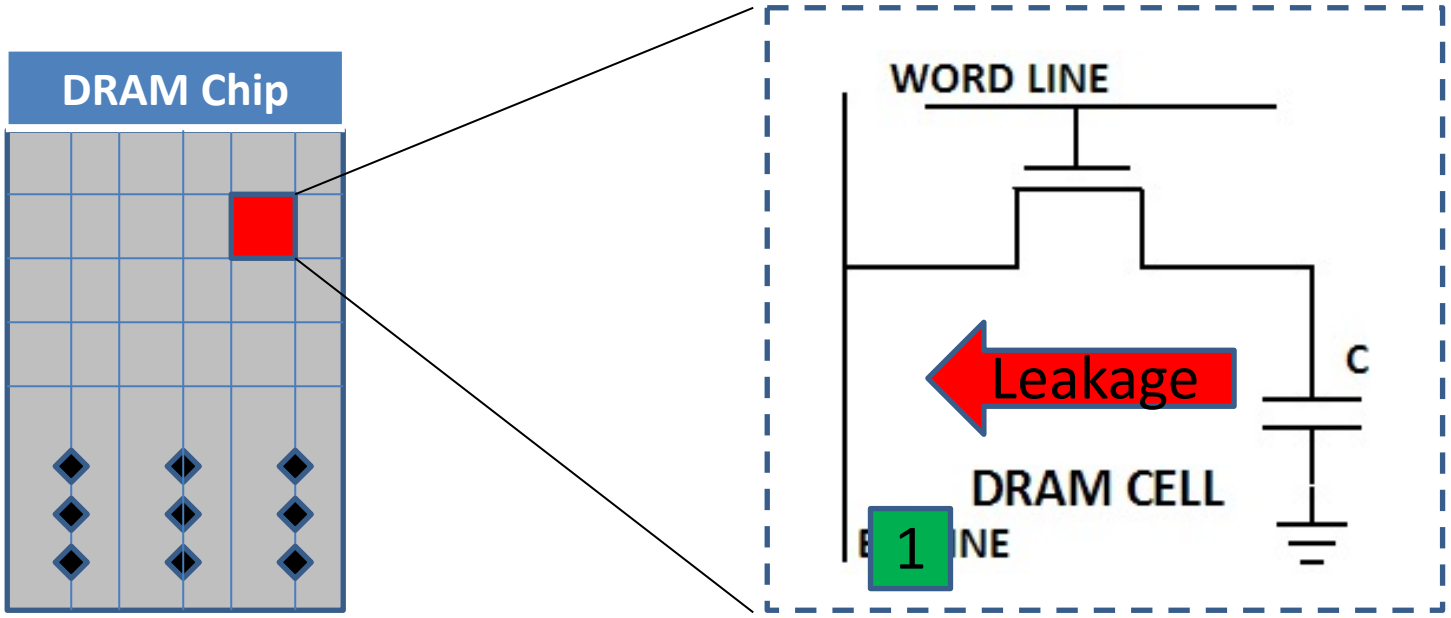
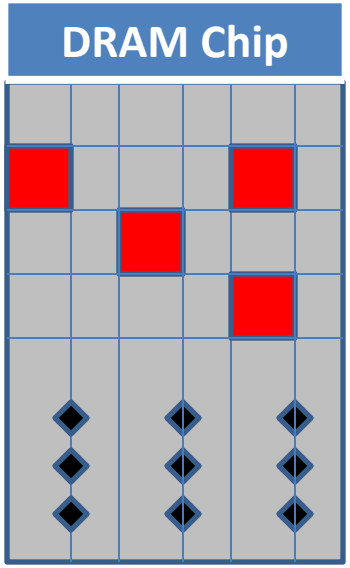


DRAM is a volatile memory → charges leak quickly

DRAM REFRESH

DRAM maintains data integrity by Refresh operations



JEDEC: 64ms

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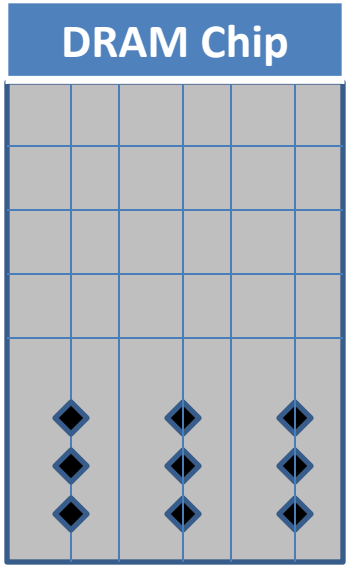

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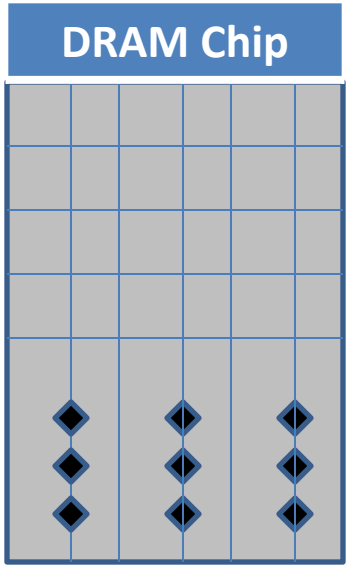

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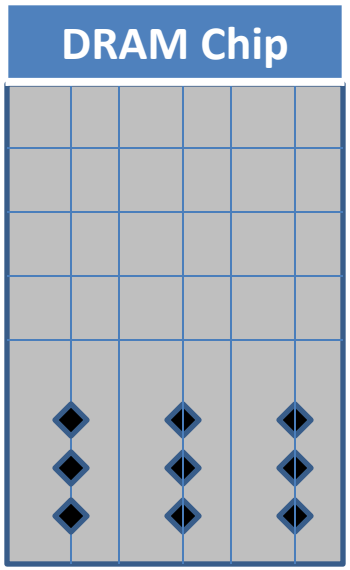

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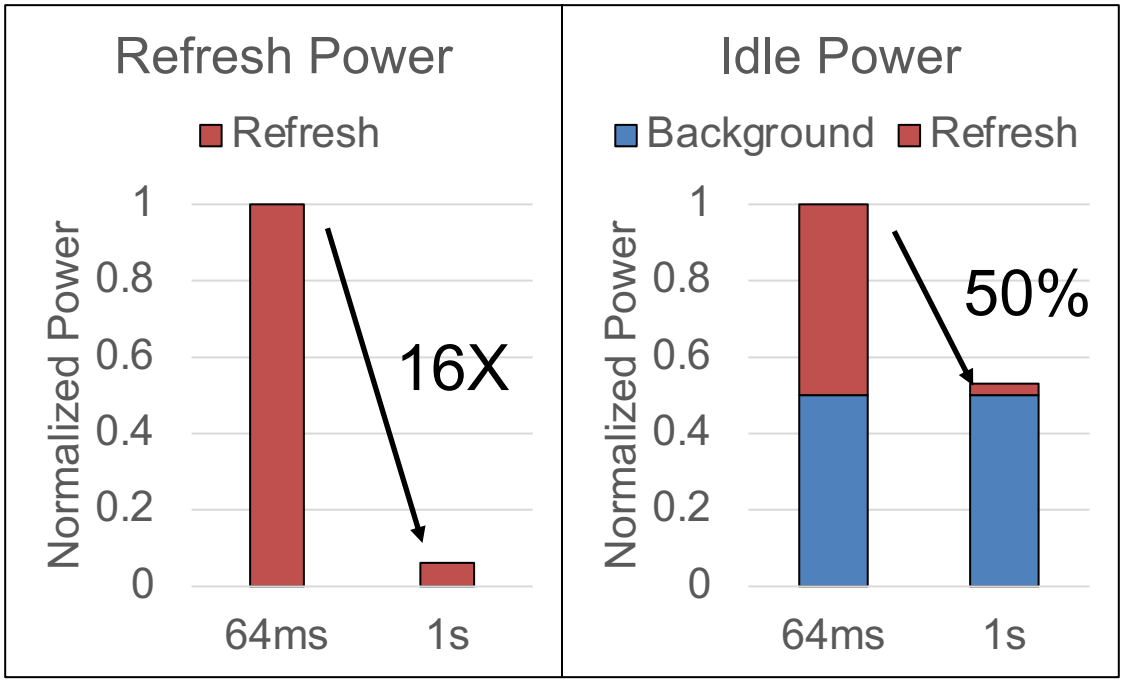
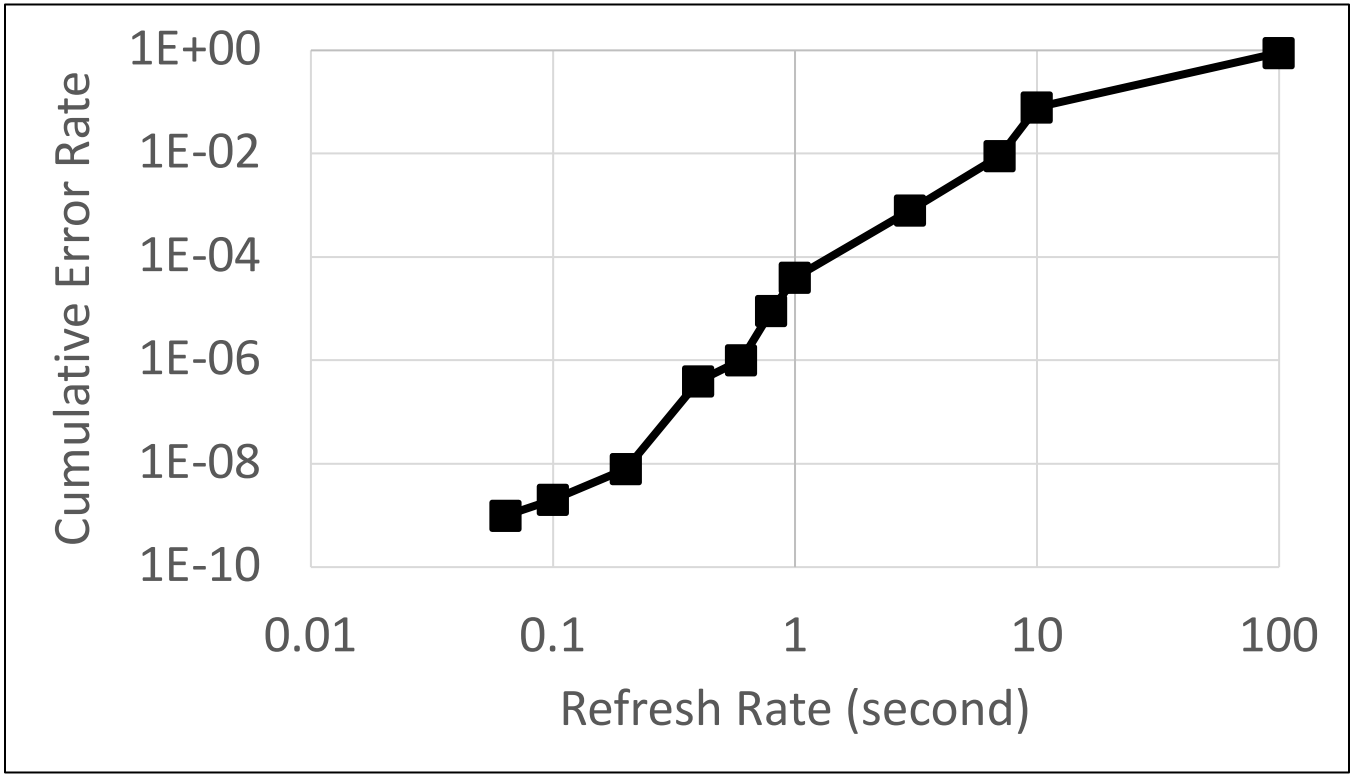


Lowering refresh rate reduces power

DRAM REFRESH RATE AND ERRORS

DRAM maintains data integrity by Refresh operations



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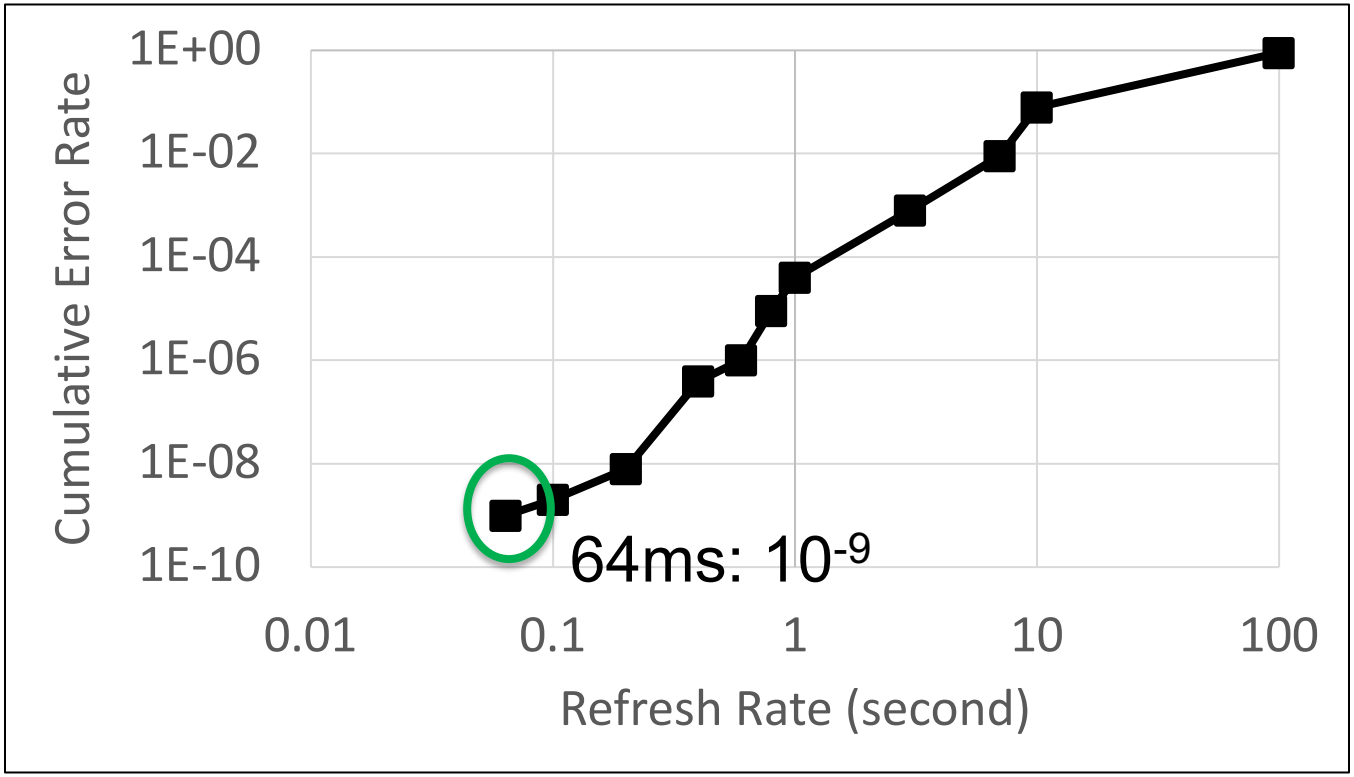

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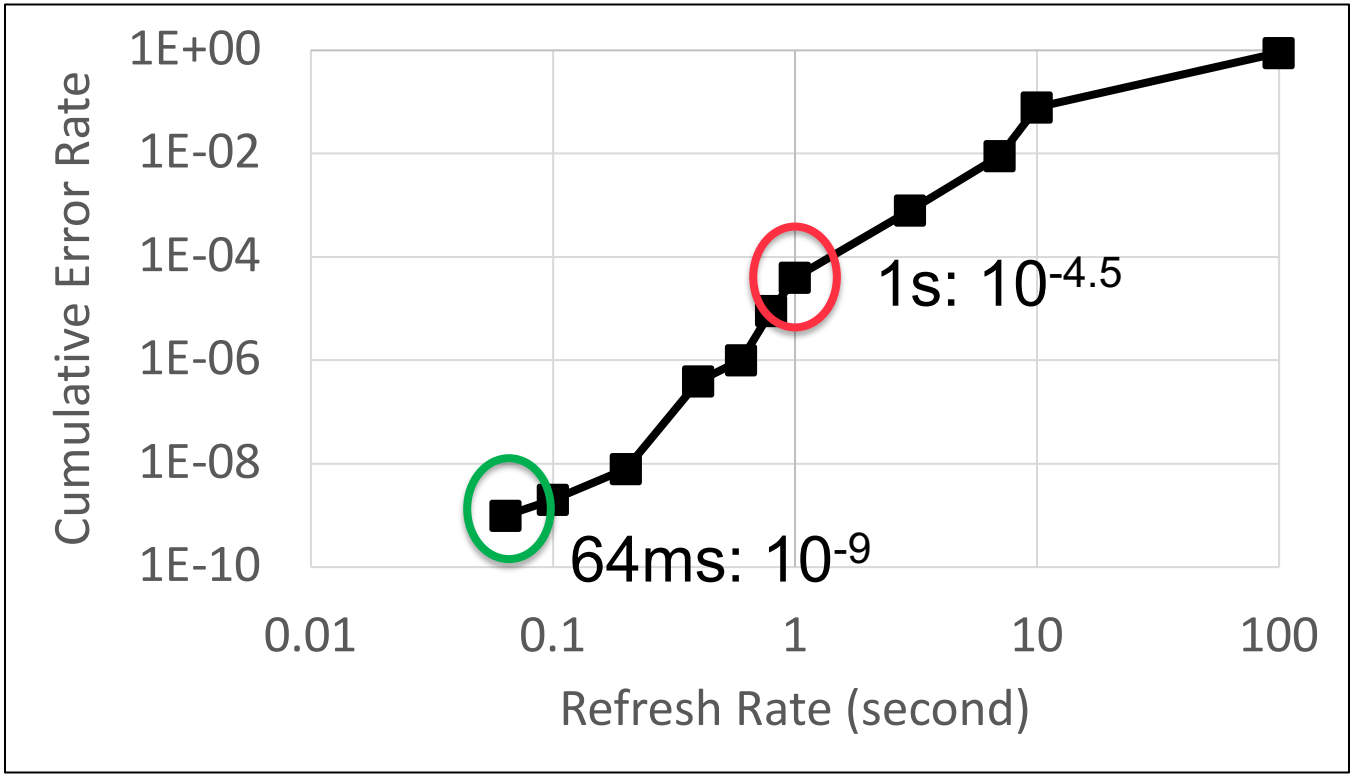

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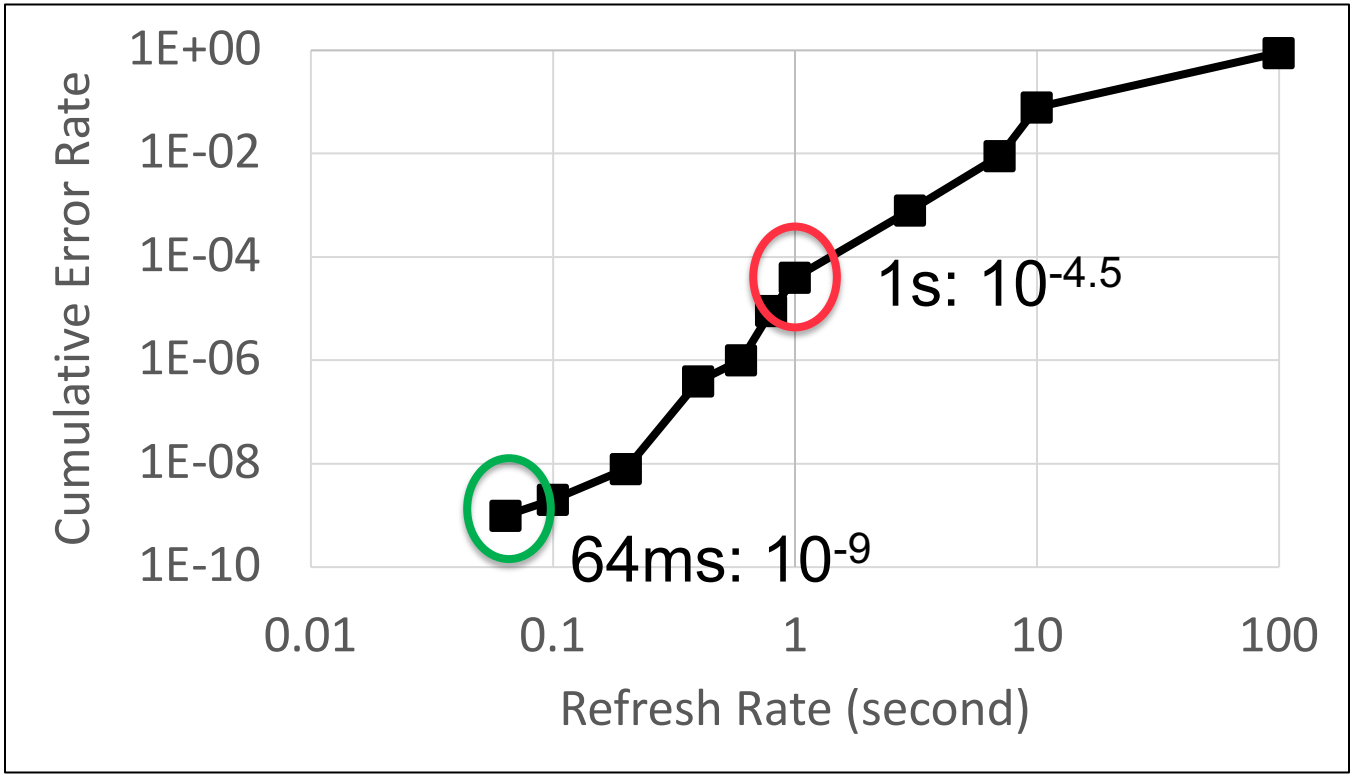
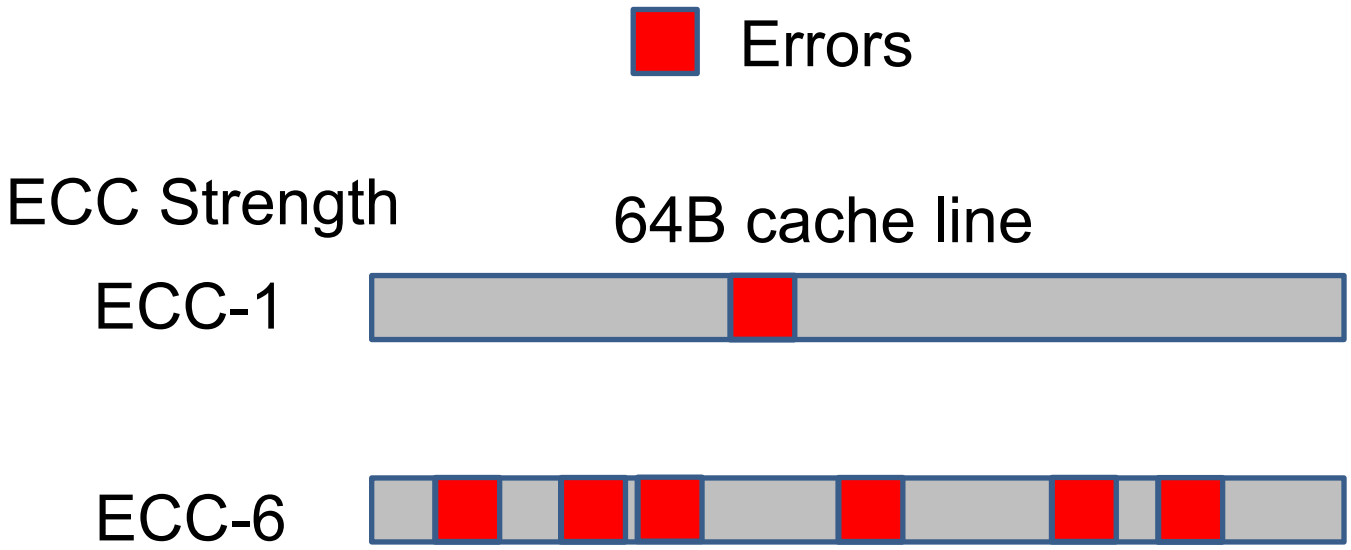


Lowering refresh rate increases bit error rate

ERROR CORRECTION CODE (ECC)

ECC: tolerate refresh errors

Q: how many errors should the system tolerate?



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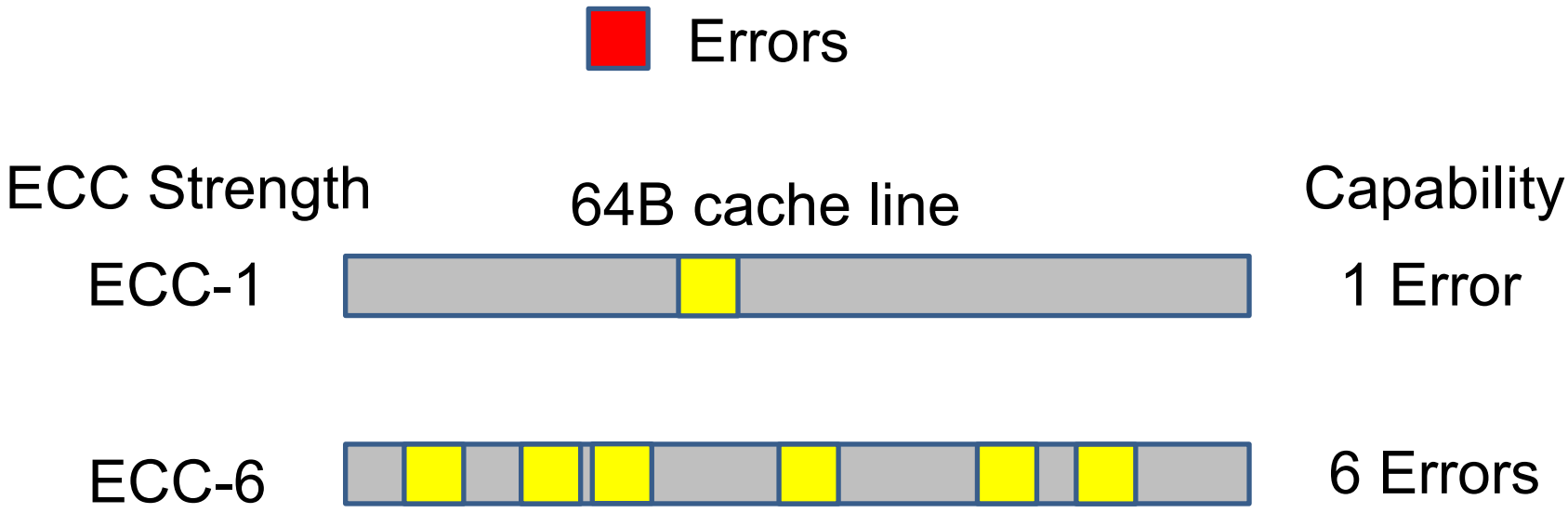

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ECC Strength	Line Failure	System Failure
ECC-1	1.8×10^{-2}	1.0
ECC-2	9.8×10^{-7}	1.0
ECC-4	1.6×10^{-11}	2.7×10^{-4}
ECC-5	4.9×10^{-14}	8.1×10^{-7}
ECC-6	1.2×10^{-16}	1.8×10^{-9}

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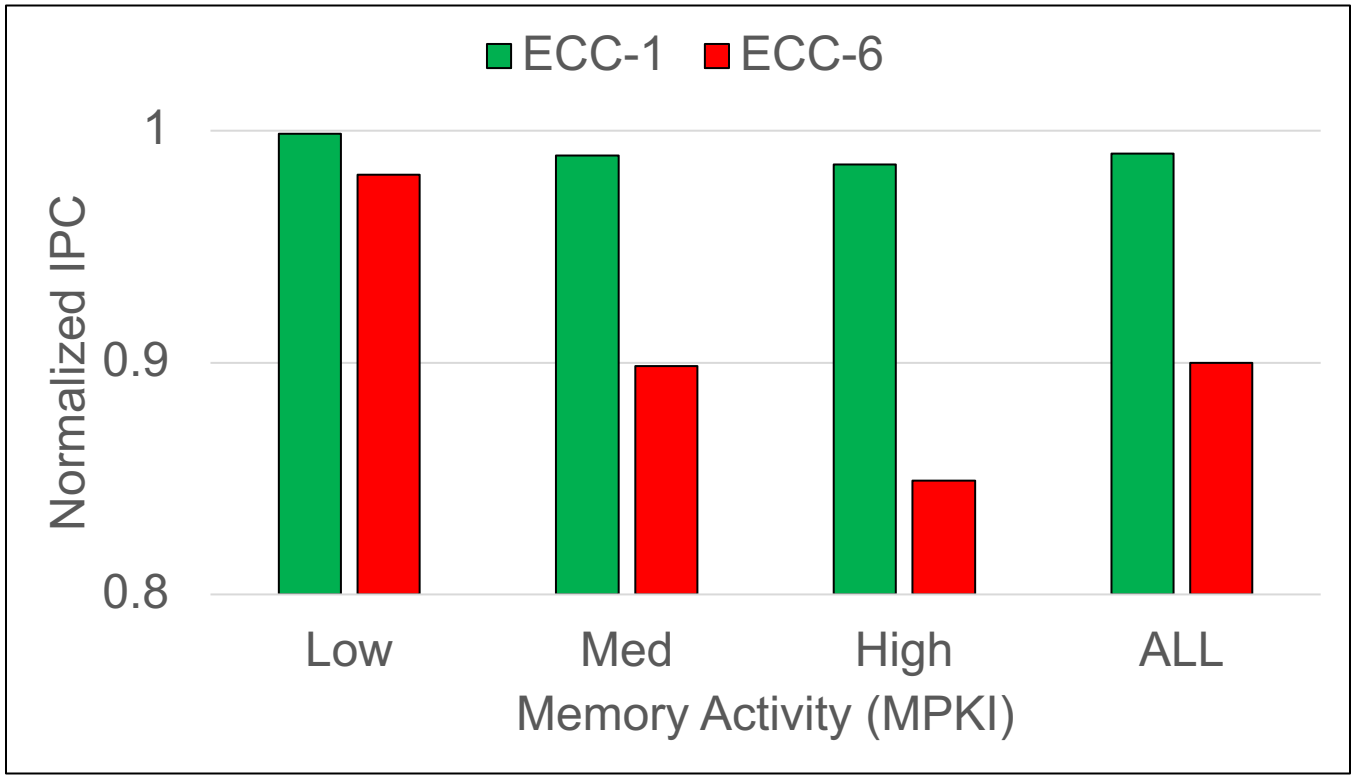
Refresh rate of 1s needs ECC-6 for errors

DRAWBACKS OF ECC-6

Single Core, 1MB Cache, 1GB DRAM



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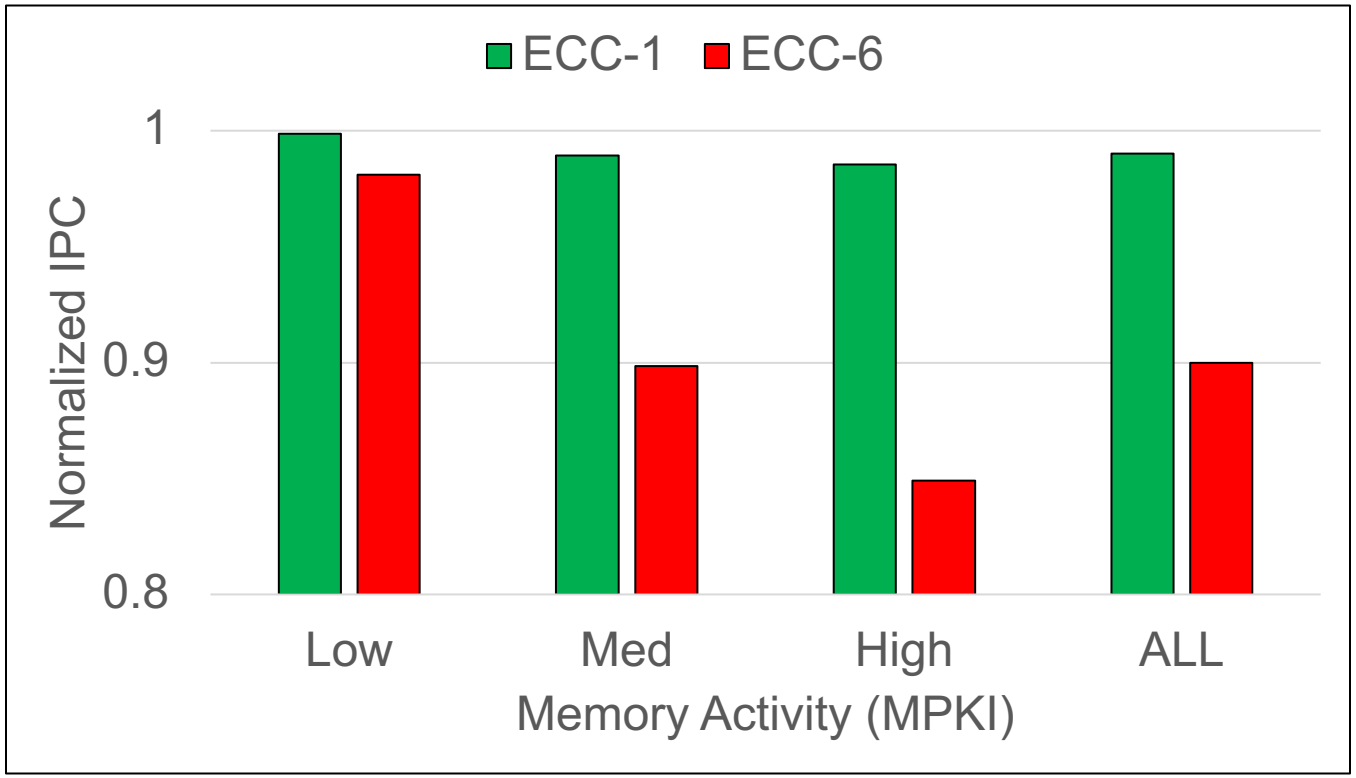

ECC-6 incurs huge performance degradation

WHAT IS THE IDEAL CASE?

	Goal
Active Mode	**Performance** (Refresh Power Negligible)
Idle Mode	**Energy** (Performance Not Critical)

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	Goal	Strong ECC
Active Mode	**Performance** (Refresh Power Negligible)	✘ Bad
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WHAT IS THE IDEAL CASE?

	Goal	Strong ECC	Weak ECC
Active Mode	**Performance** (Refresh Power Negligible)	✘ Bad	✔ Good
Idle Mode	**Energy** (Performance Not Critical)	✔ Good	✘ Bad

WHAT IS THE IDEAL CASE?

	Goal	Strong ECC	Weak ECC
Active Mode	**Performance** (Refresh Power Negligible)	✘ Bad	✔ Good
Idle Mode	**Energy** (Performance Not Critical)	✔ Good	✘ Bad

Ideally, we want ECC-1 in active mode, and ECC-6 in idle mode

WHAT IS THE IDEAL CASE?

	Goal	Strong ECC	Weak ECC
Active Mode	**Performance** (Refresh Power Negligible)	?	✔ Good
Idle Mode	**Energy** (Performance Not Critical)	✔ Good	?

Ideally, we want ECC-1 in active mode, and ECC-6 in idle mode

AGENDA

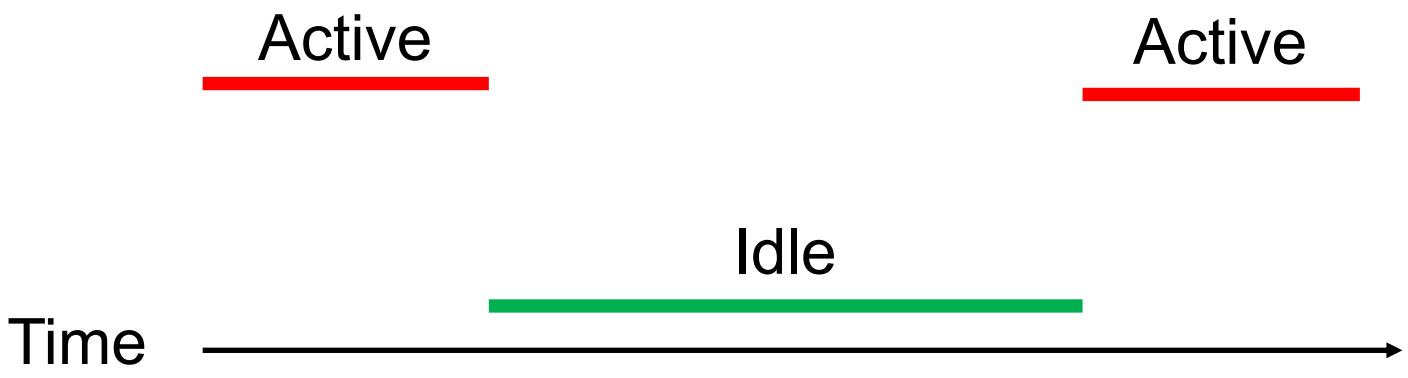
- Introduction
- Background
- **Morphable ECC (MECC)**
  - Overview
  - Design
  - ECC Support and Storage
- Results
- Summary

MECC: OVERVIEW

Active

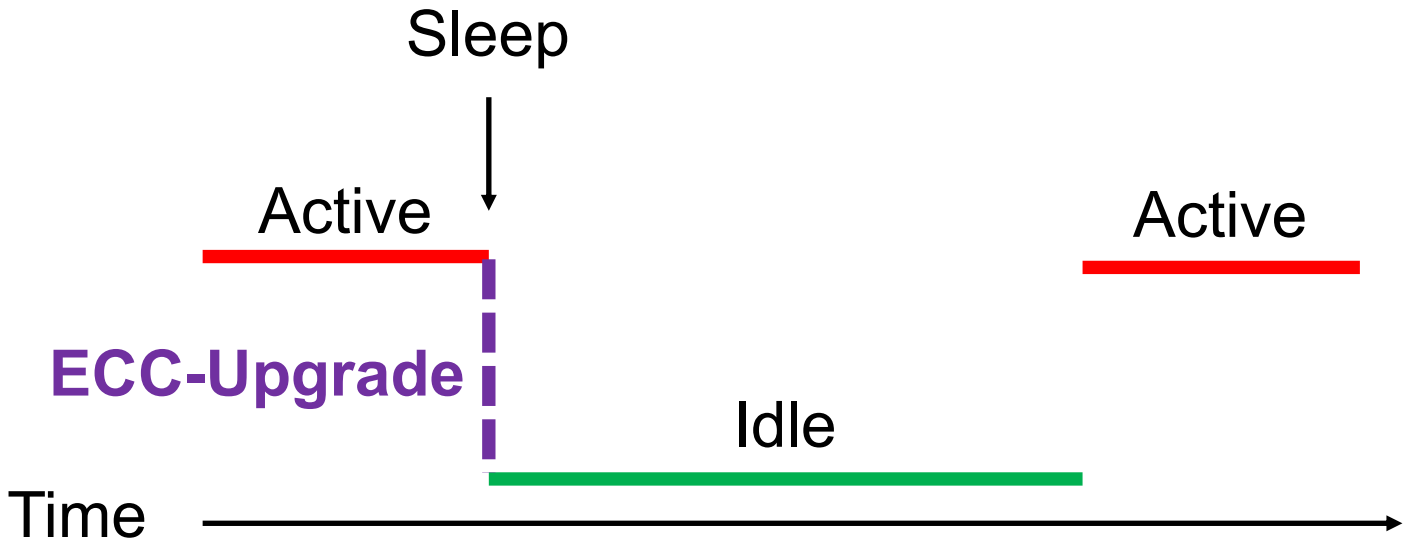
REFRESH	Normal
ECC	Weak

MECC: OVERVIEW



REFRESH	Normal	Slow	Normal
ECC	Weak	Strong	Weak

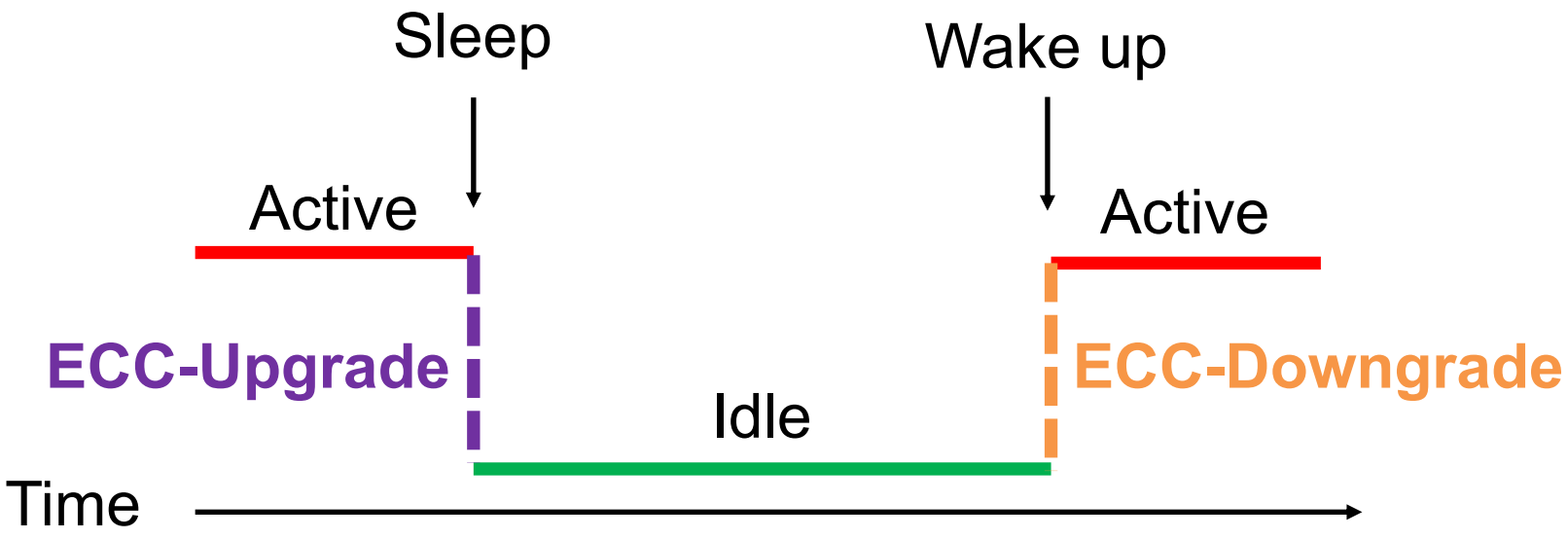
MECC: OVERVIEW



REFRESH	Normal	Slow	Normal
ECC	Weak	Strong	Weak

ECC-Upgrade

MECC: OVERVIEW



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ECC	Weak	Strong	Weak

ECC-Upgrade

ECC-Downgrade

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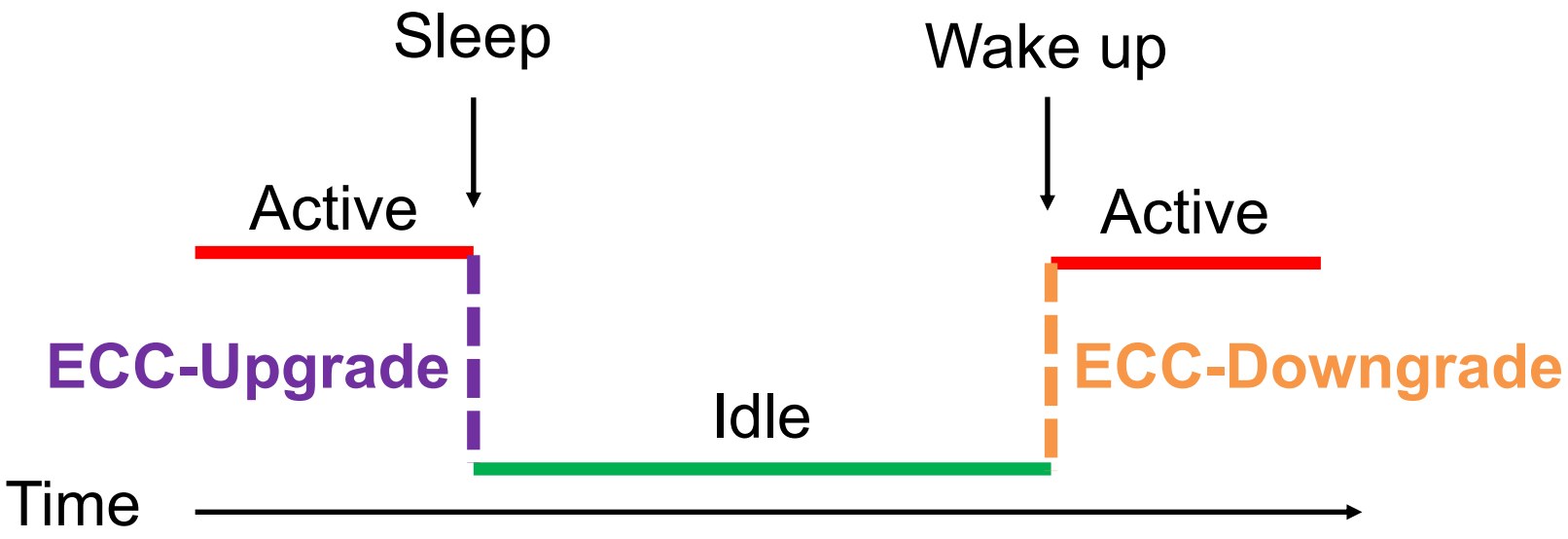
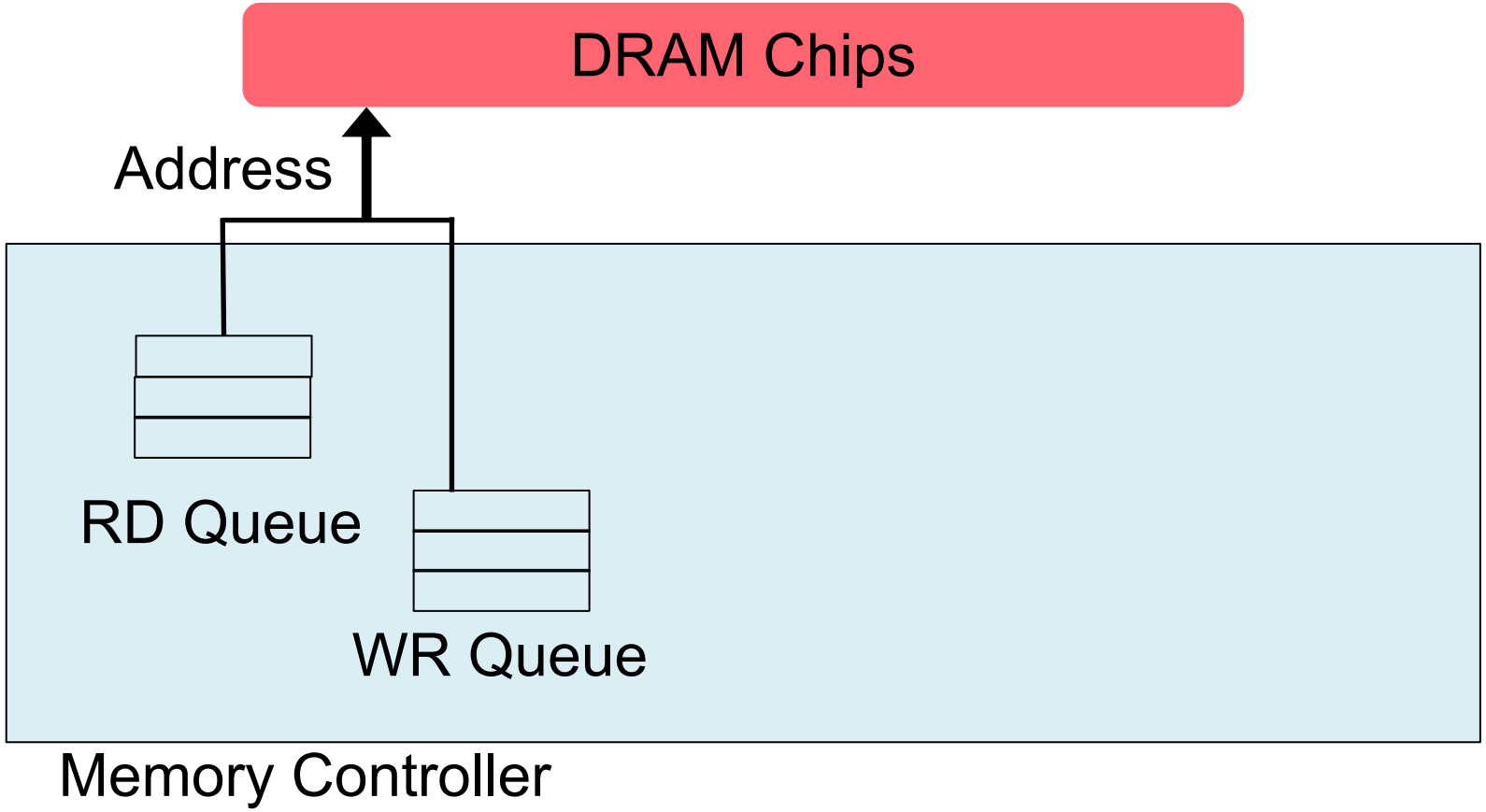


REFRESH	Normal	Slow	Normal
ECC	Weak	Strong	Weak

ECC-Upgrade ECC-Downgrade

MECC uses two ECCs based on modes

MECC: DESIGN



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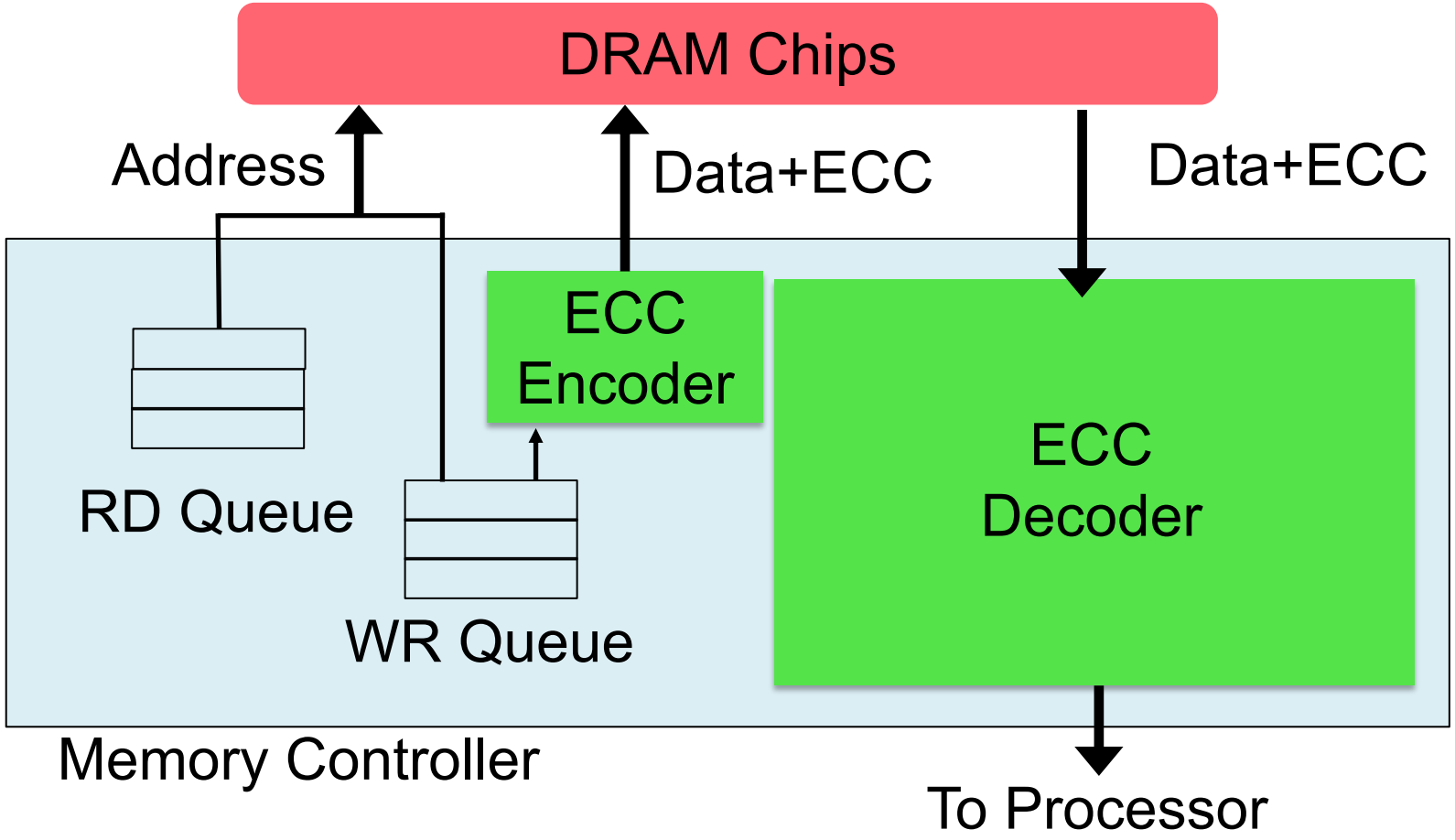
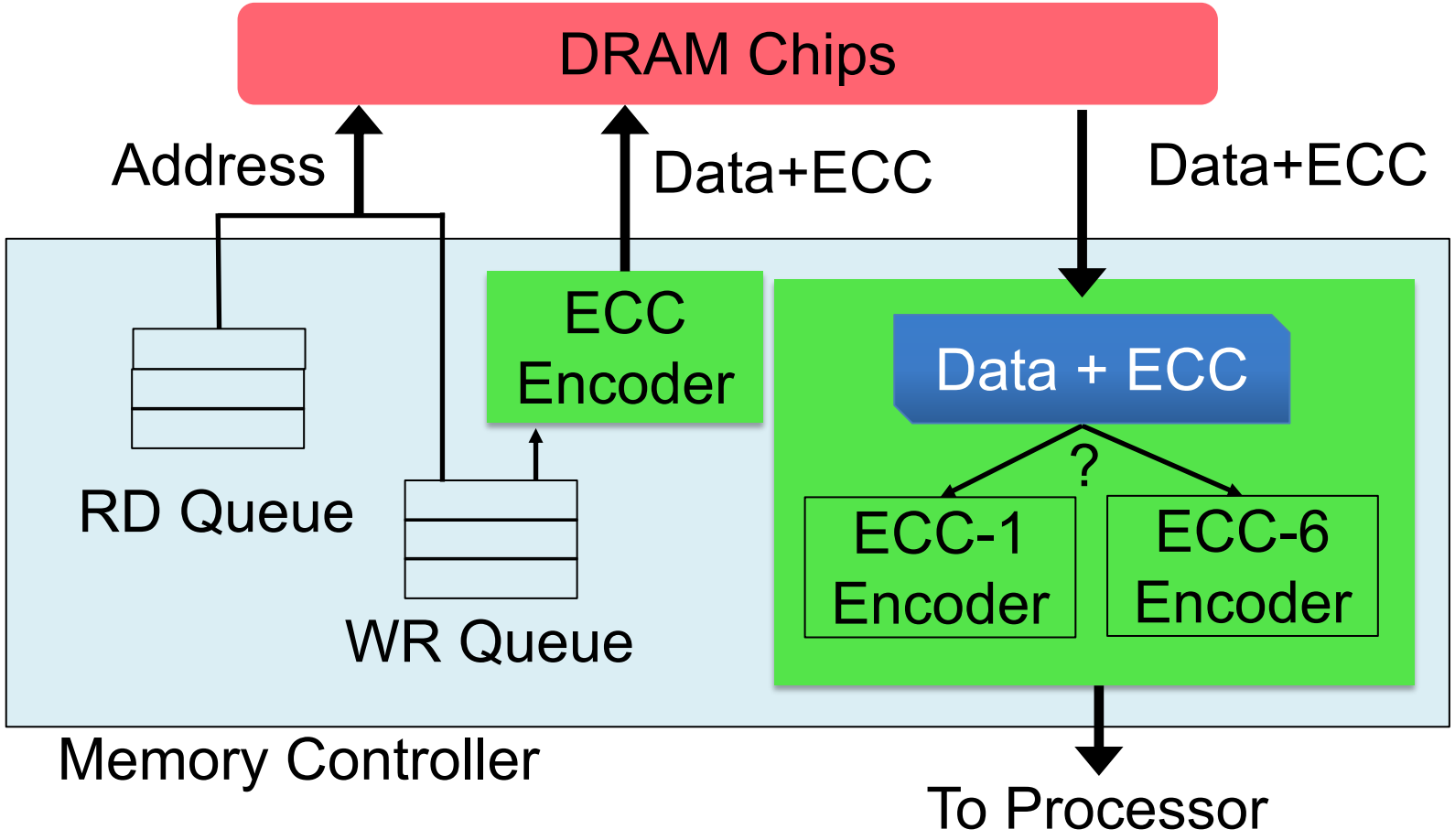

DRAM Chips
Address
Data+ECC
Data+ECC
ECC
Encoder
ECC
Decoder
RD Queue
WR Queue
Memory Controller
To Processor

MECC: DESIGN


DRAM Chips
Address
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Data+ECC
ECC Encoder
Data + ECC
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WR Queue
ECC-1 Encoder
ECC-6 Encoder
Memory Controller
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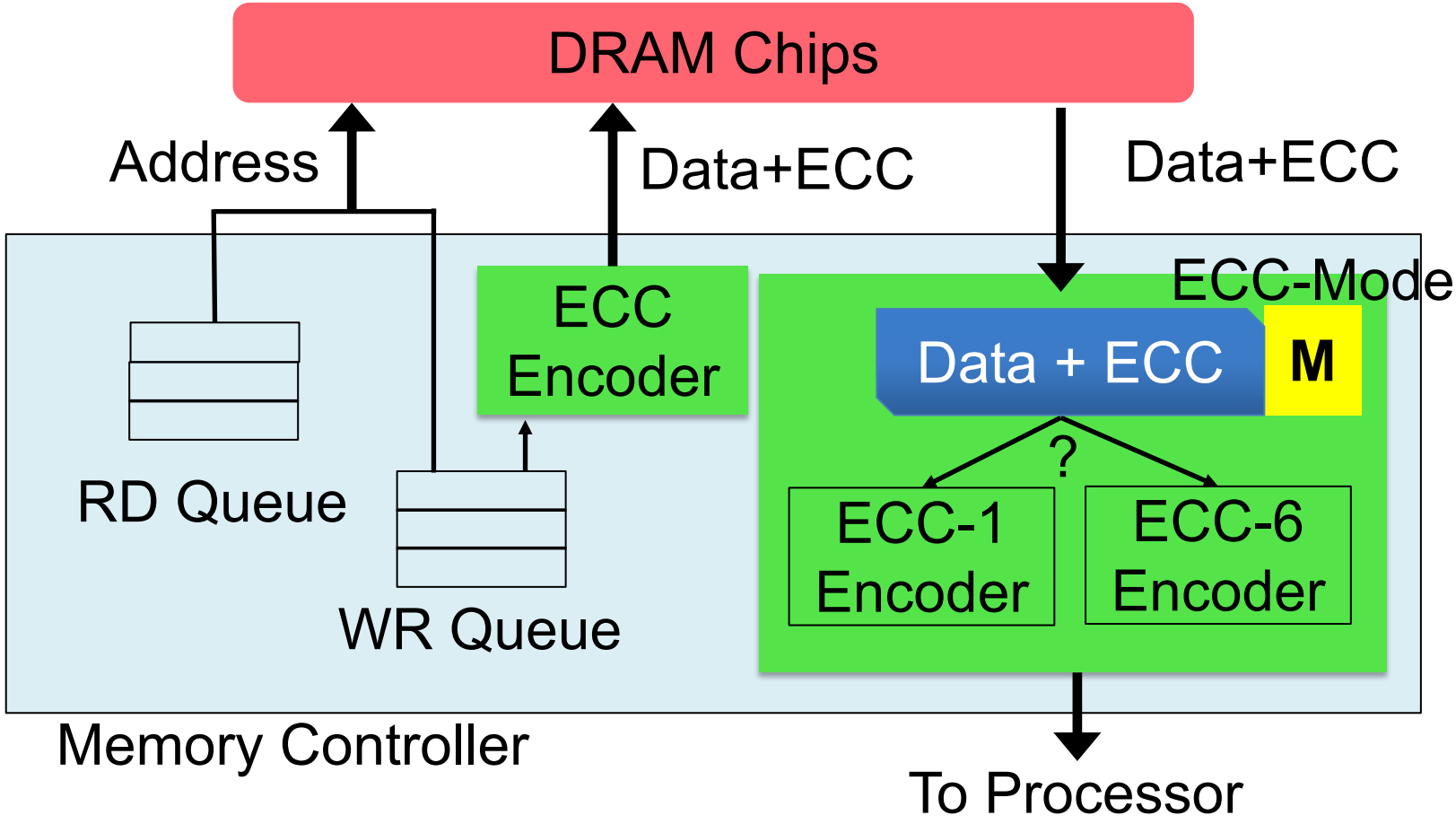
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Address
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ECC
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ECC-Mode
Data + ECC
M
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ECC-1
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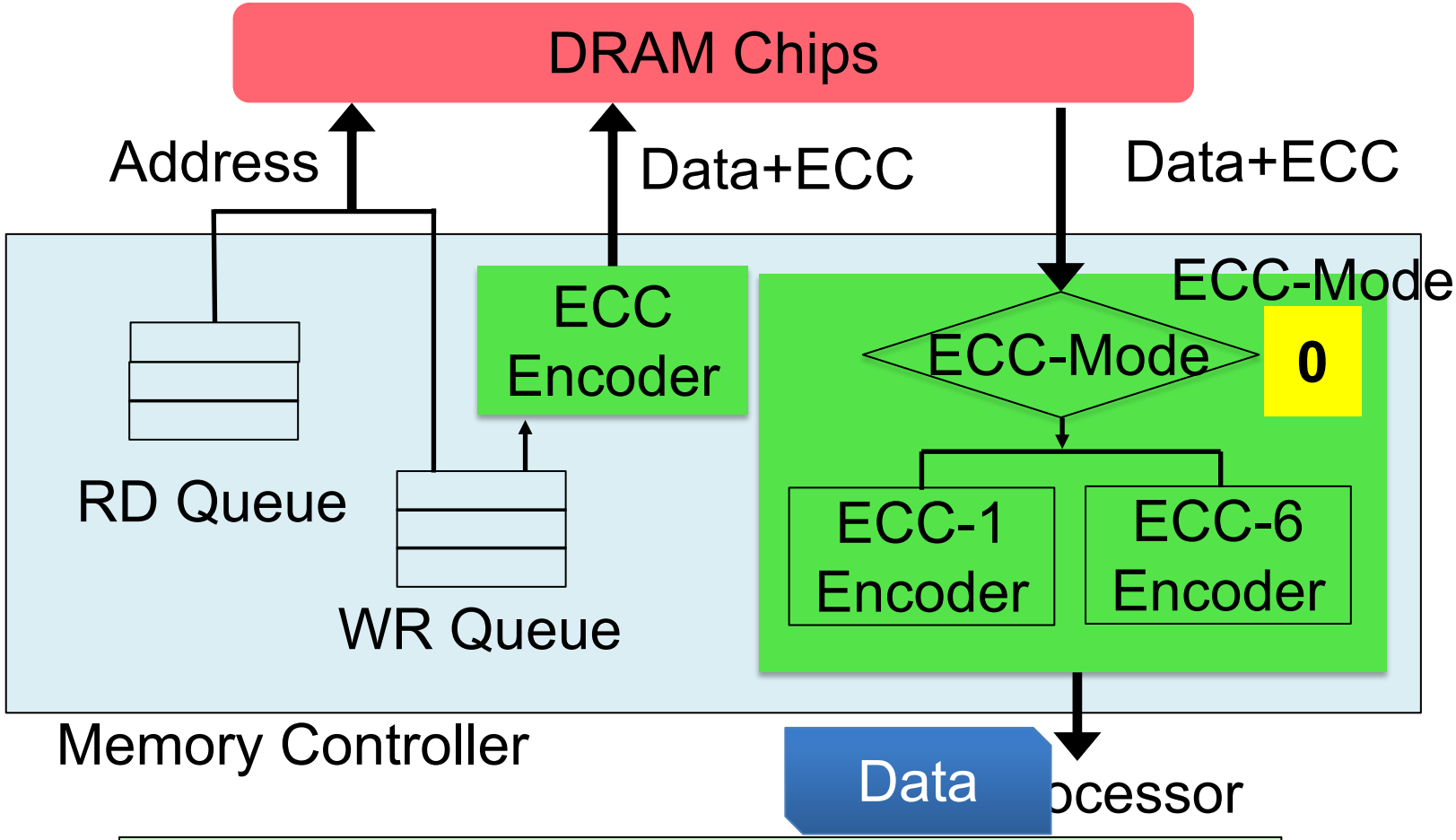

Memory controller uses ECC-mode bits to decode with different ECCs

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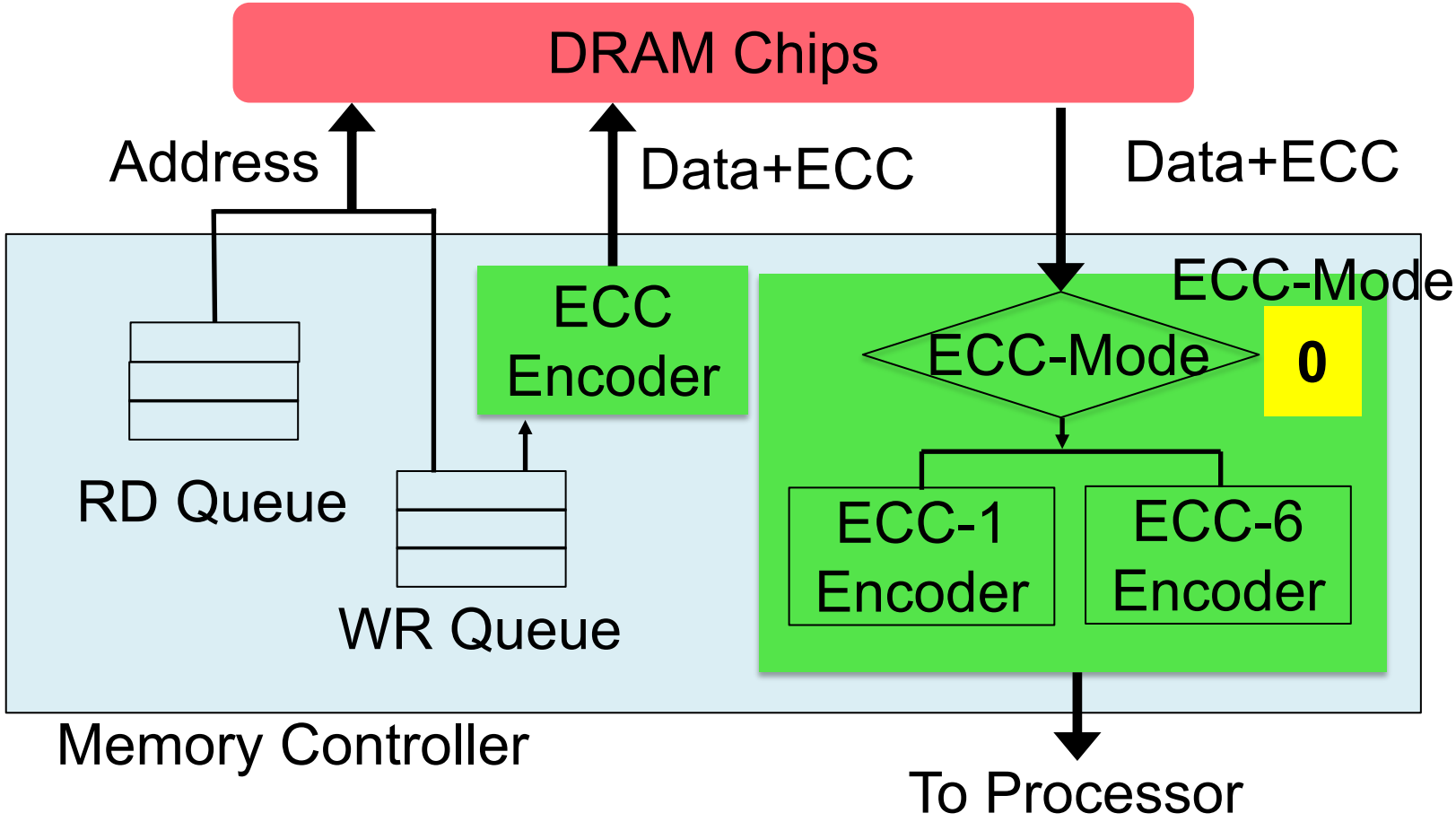

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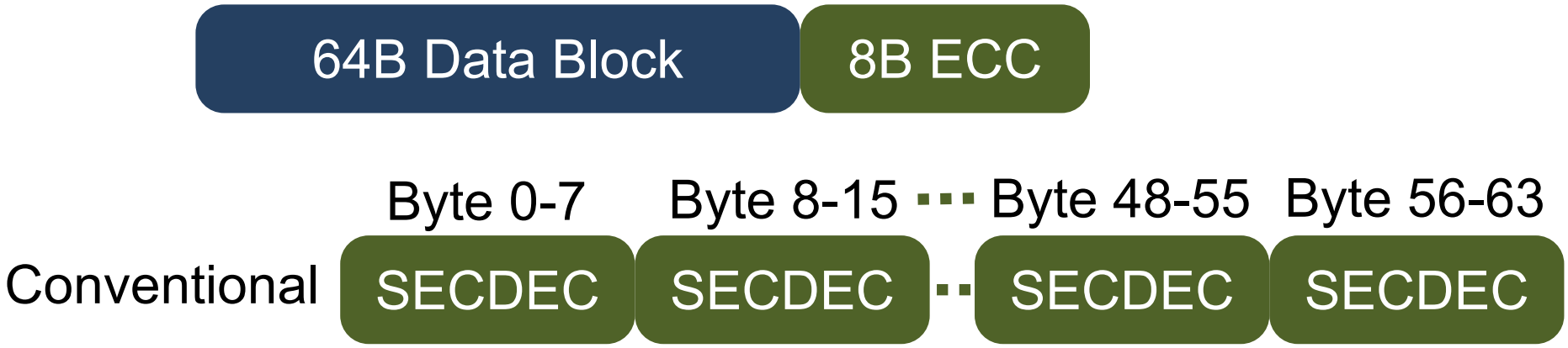
MECC: ECC STORAGE



MECC: ECC STORAGE

MECC ECC-1 11 bits

MECC ECC-6 60 bits

MECC: ECC STORAGE

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\+

MECC ECC-6 60 bits

= 60 bits

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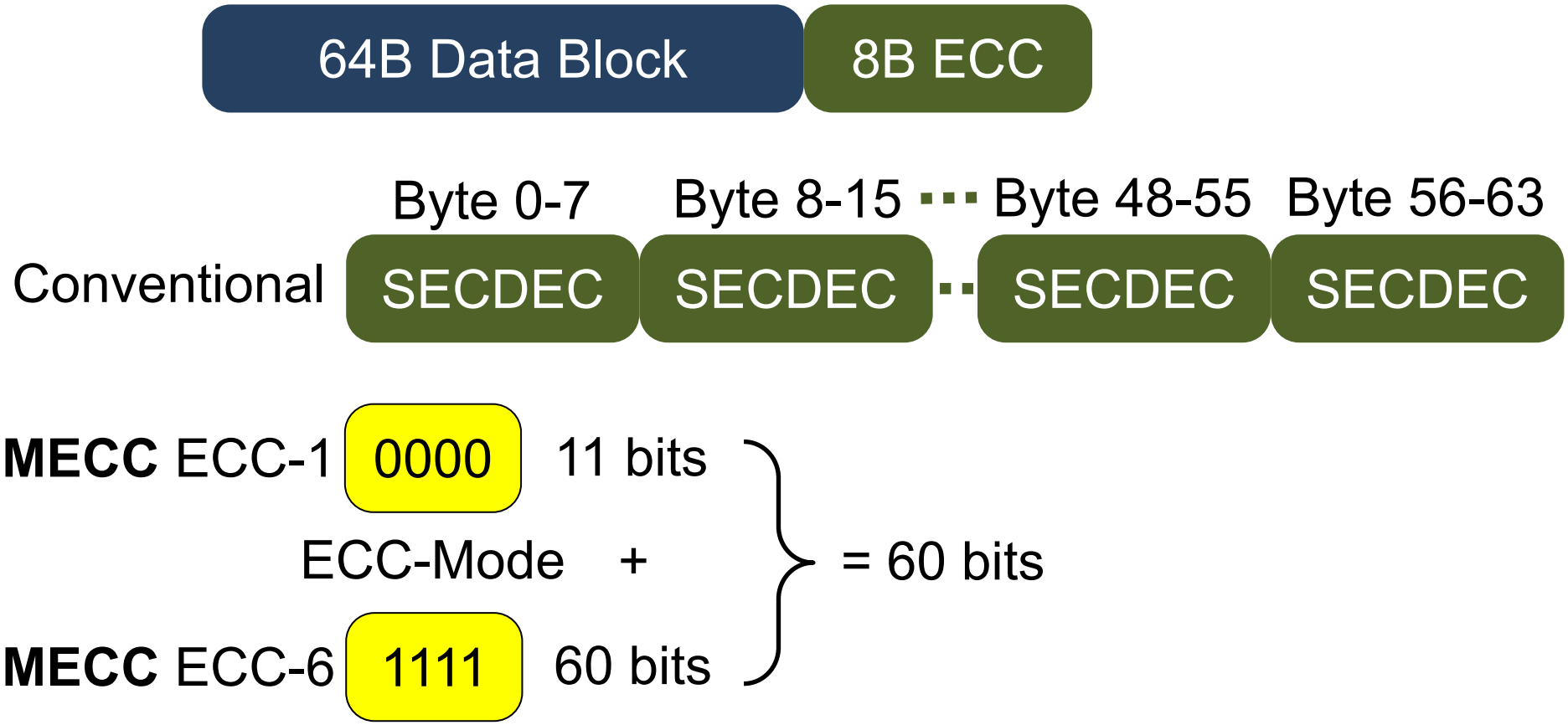

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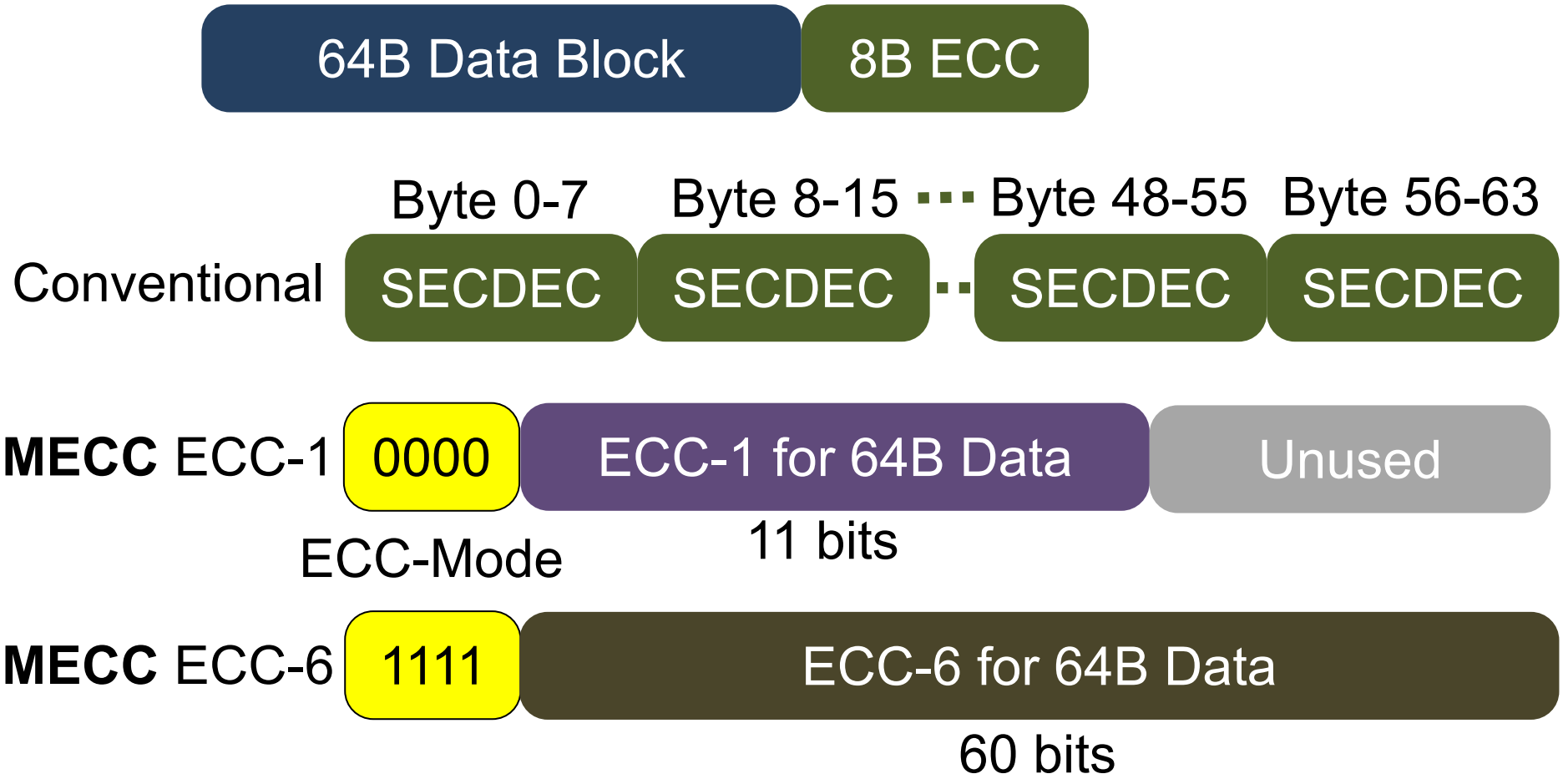

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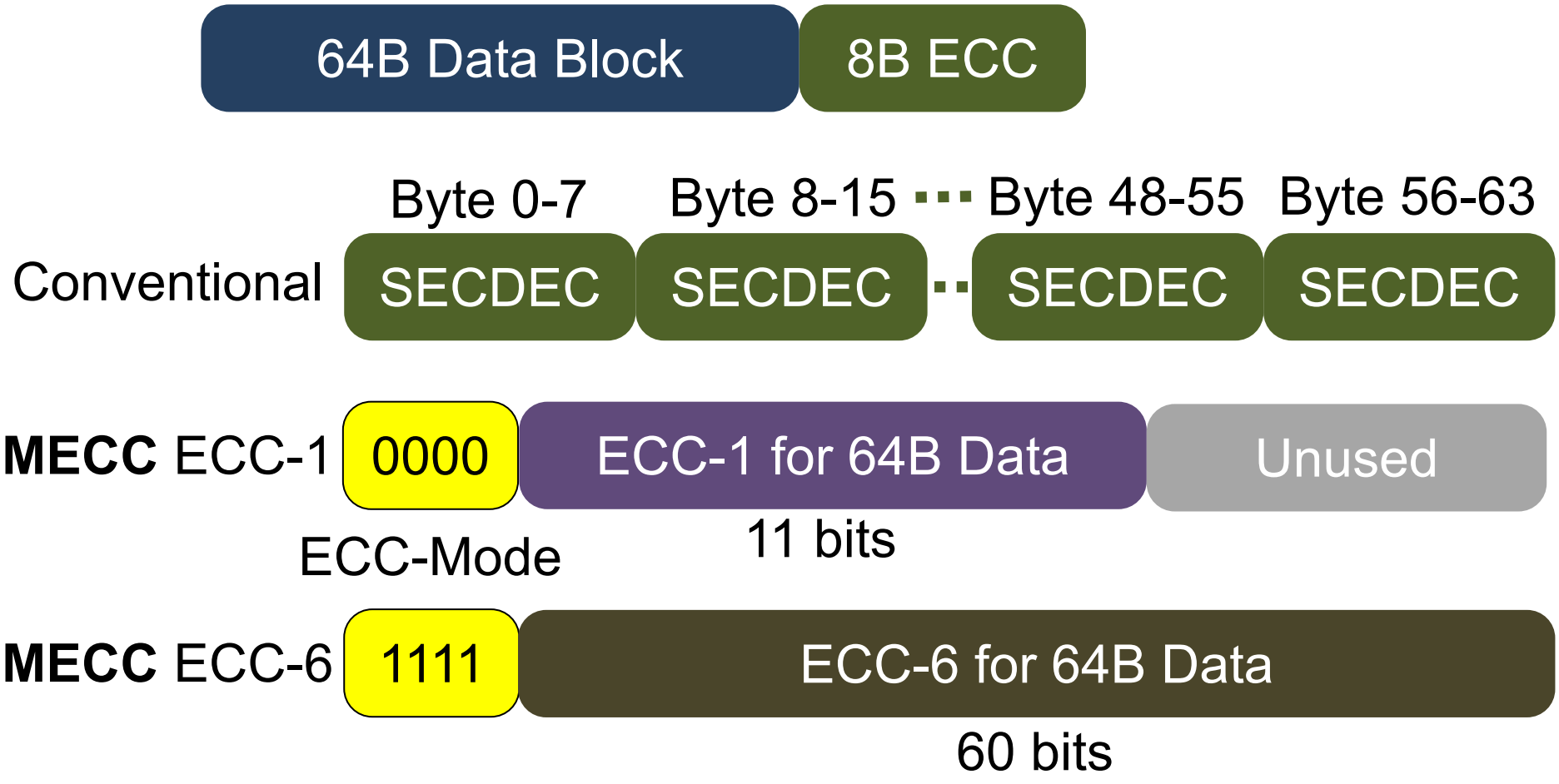

MECC uses existing space to store 2 ECCs

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- **Results**
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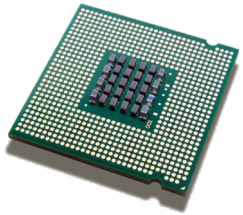
METHODOLOGY



CPU

Off-chip DRAM

Core Chips:

- 1 cores 1.6 GHz
- 2-wide In-Order
- 1MB cache

	LPDDR2
Capacity	1GB
Bus	DDR 200MGHz
Organization	1 channels, 4 banks

- USIMM for DRAM model and power
- Baseline: No Error Correction Code
- SPEC2006 (exclude mcf): low, medium, high MPKI workloads

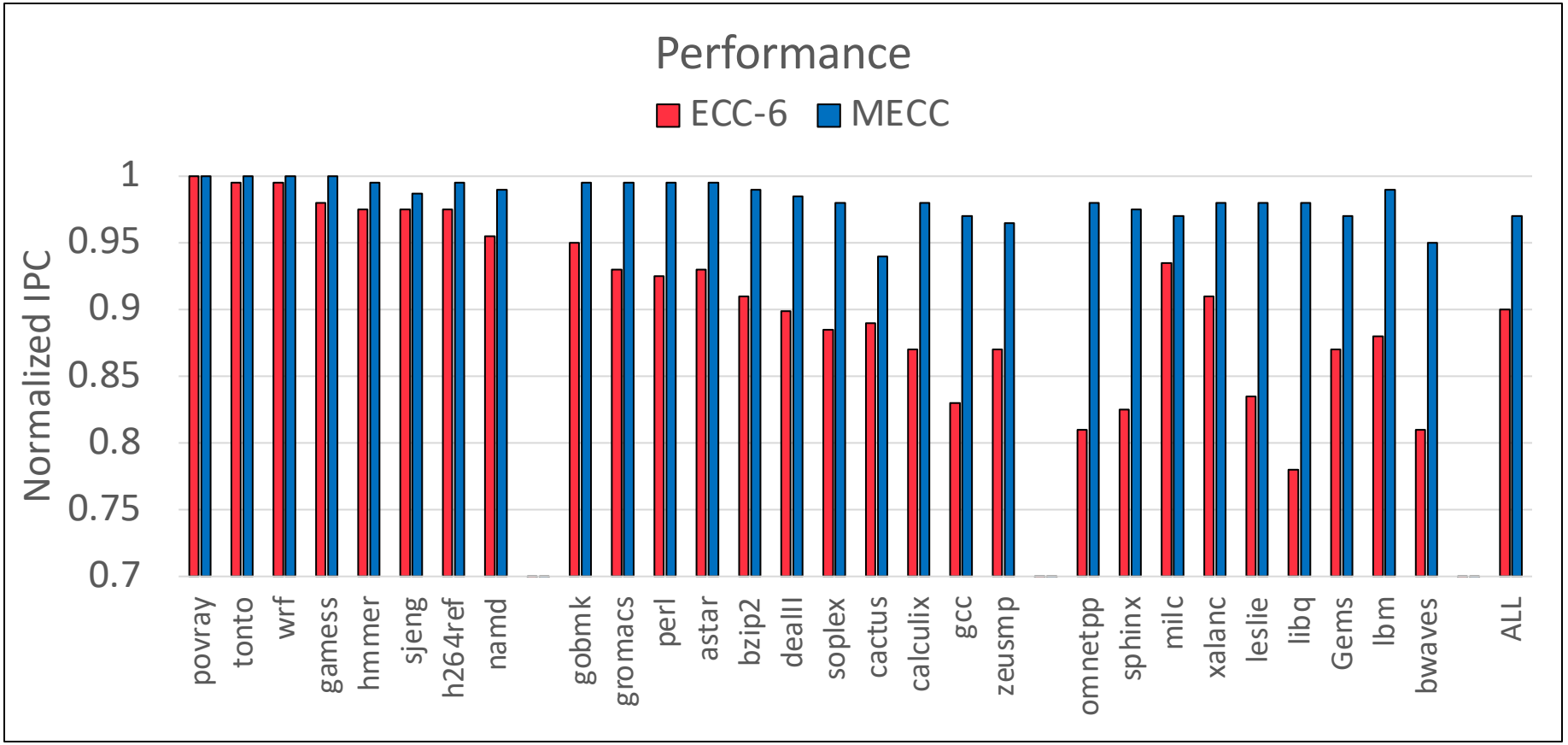
POWER AND ENERGY CONSUMPTION

Parameters	Values	Description
VDD	1.7 V	Operating Voltage
IDD0	95 mA	1 bank active precharge current
IDD2P	0.6 mA	Precharge power-down standby current
IDD3P	3 mA	Active power-down standby current
IDD4	135 mA	Burst read/write: 1 bank active
IDD5	100 mA	Auto refresh
IDD8	1.3 mA	Self refresh

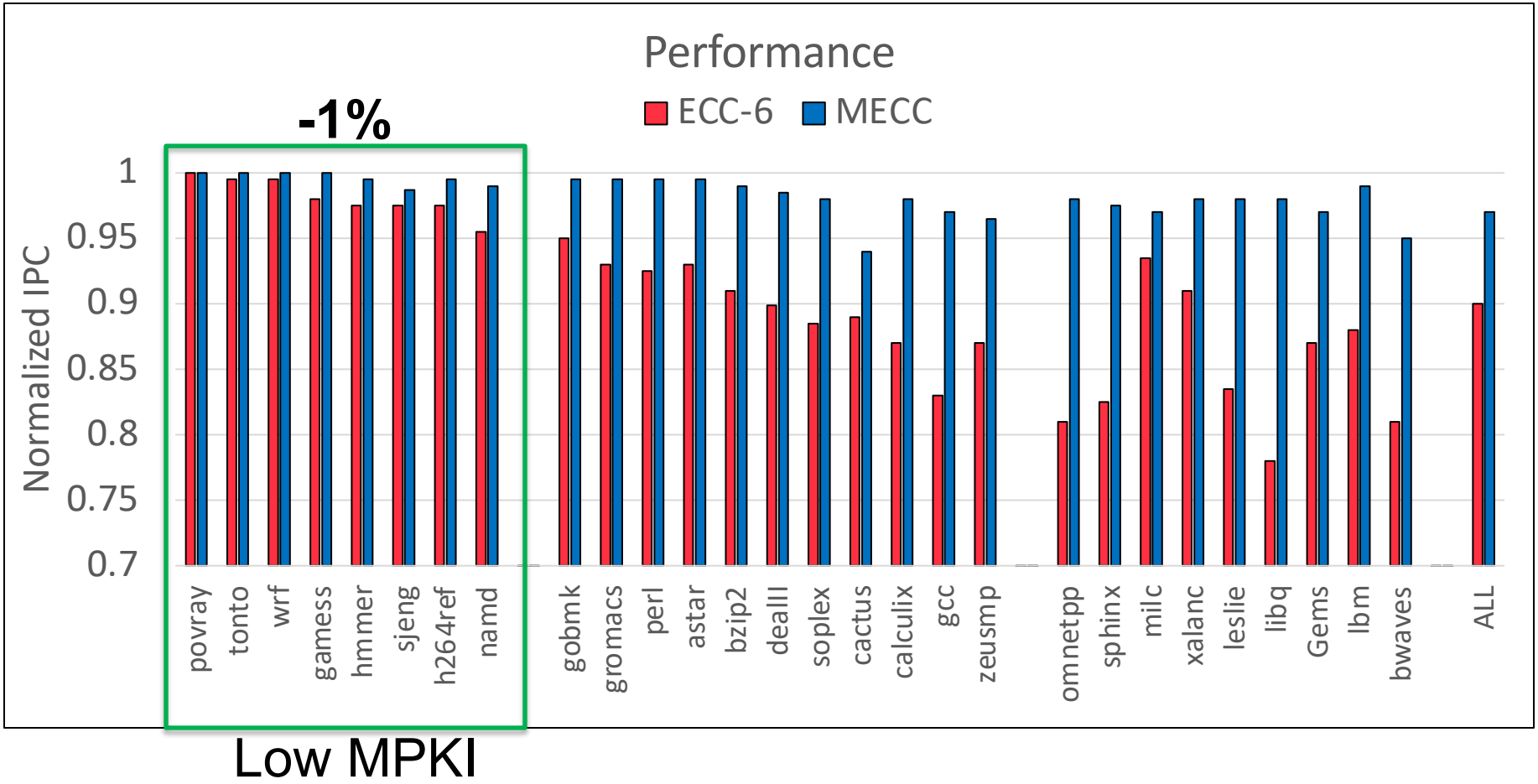
$$\text{Power in Idle Mode} = (P_{\text{refresh original}} * T_{\text{original}} / T_{\text{MECC}}) + P_{\text{other}}$$

courtesy: Micron LPDDR2 Specs

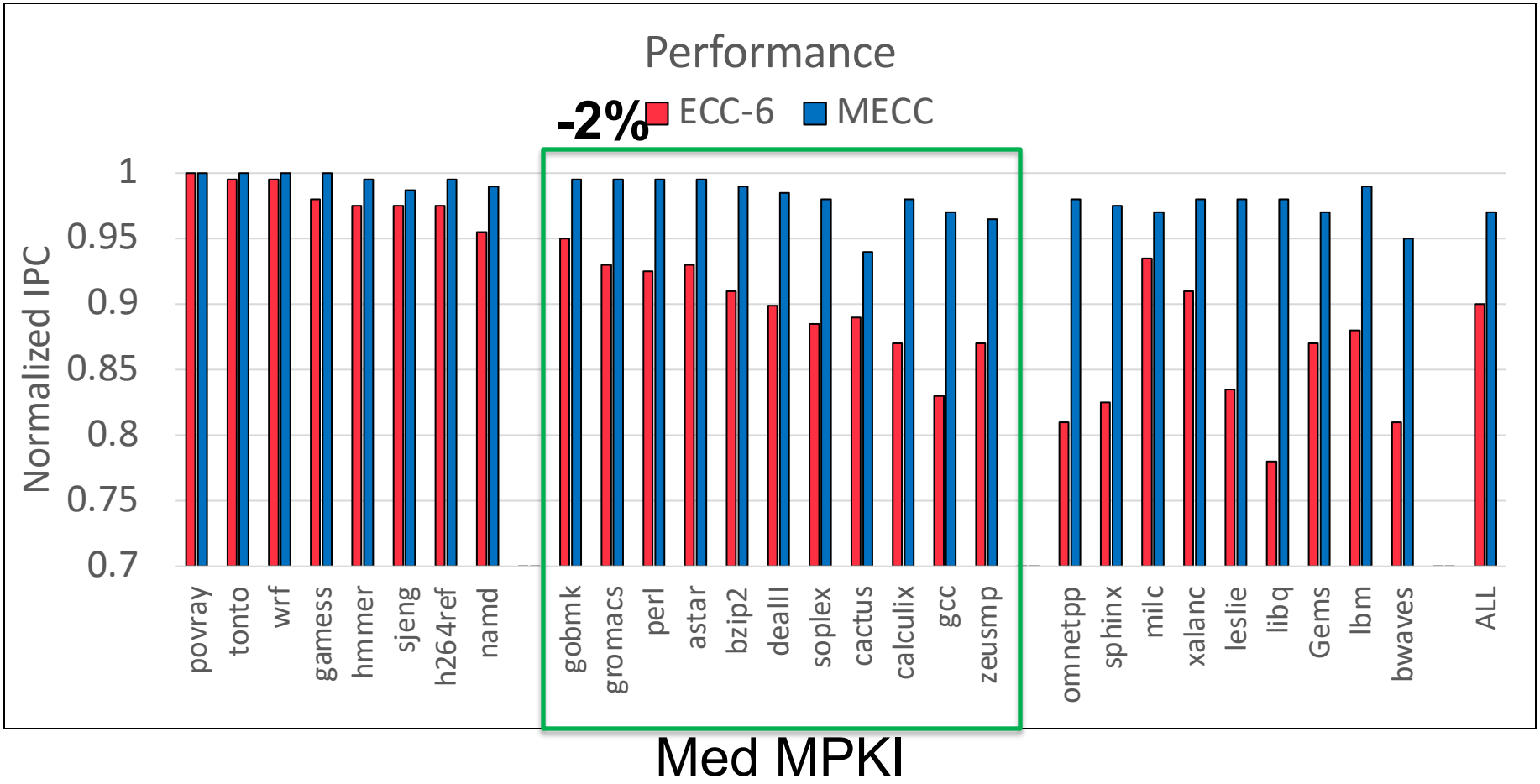
PERFORMANCE IN ACTIVE MODE



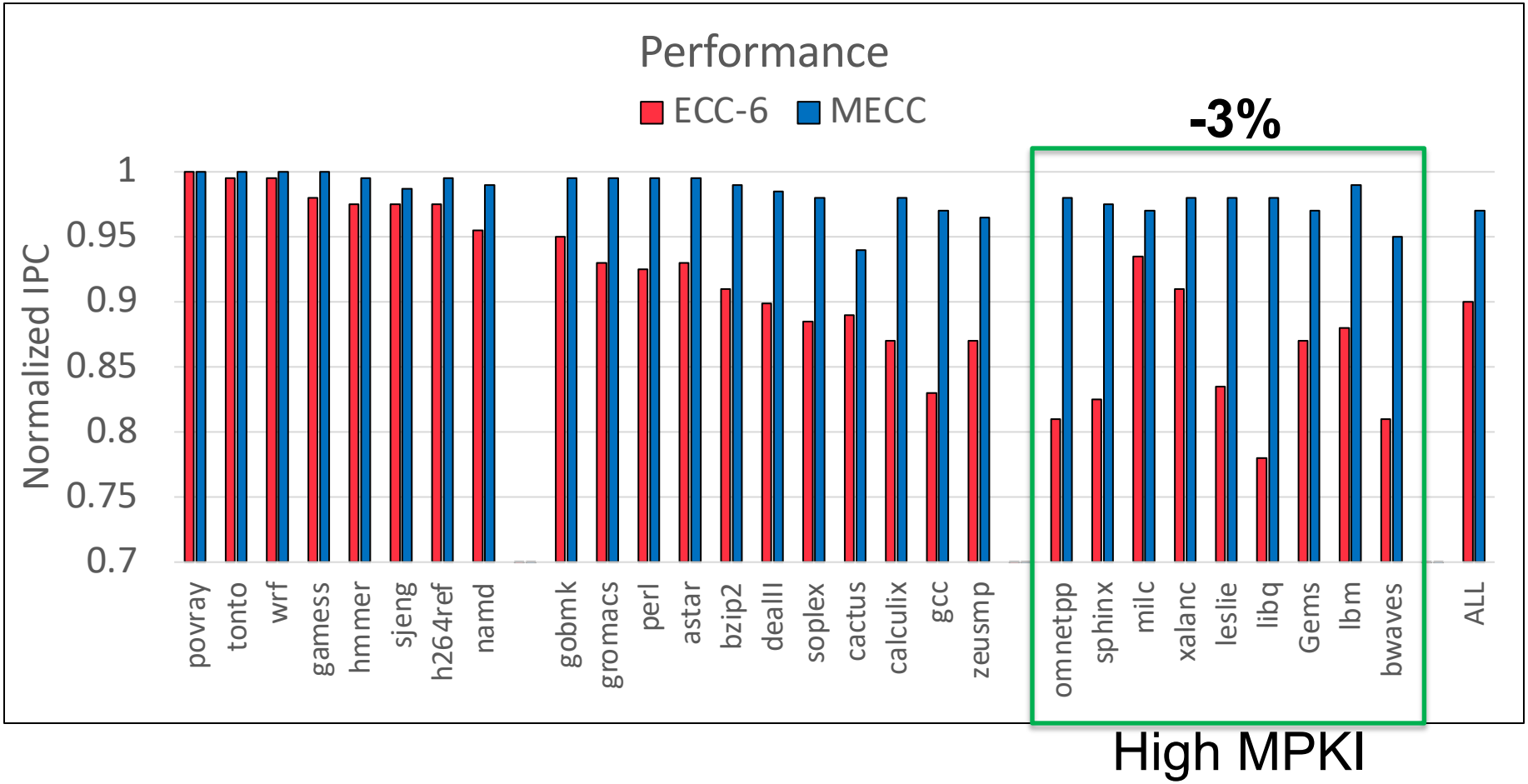
PERFORMANCE IN ACTIVE MODE



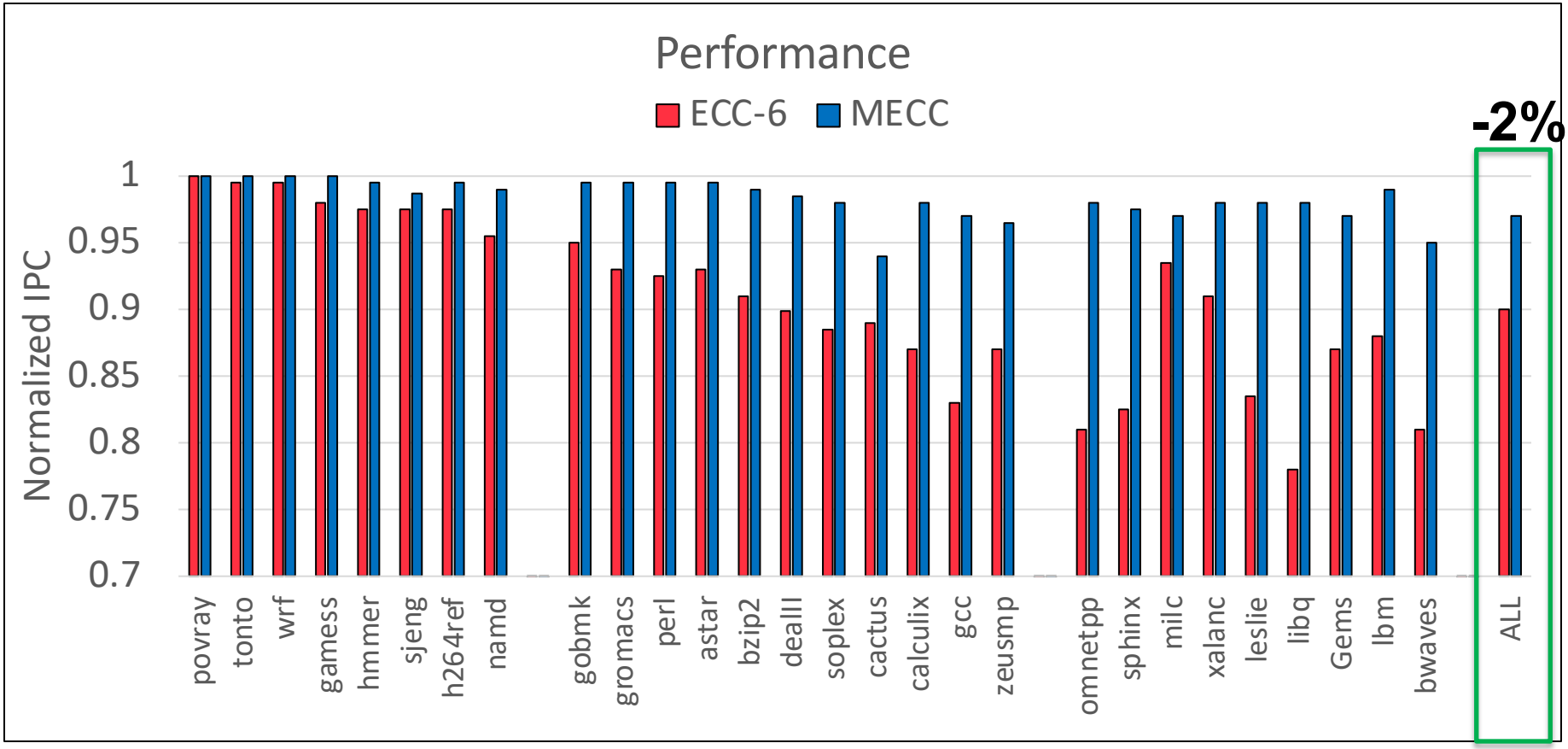
PERFORMANCE IN ACTIVE MODE



PERFORMANCE IN ACTIVE MODE

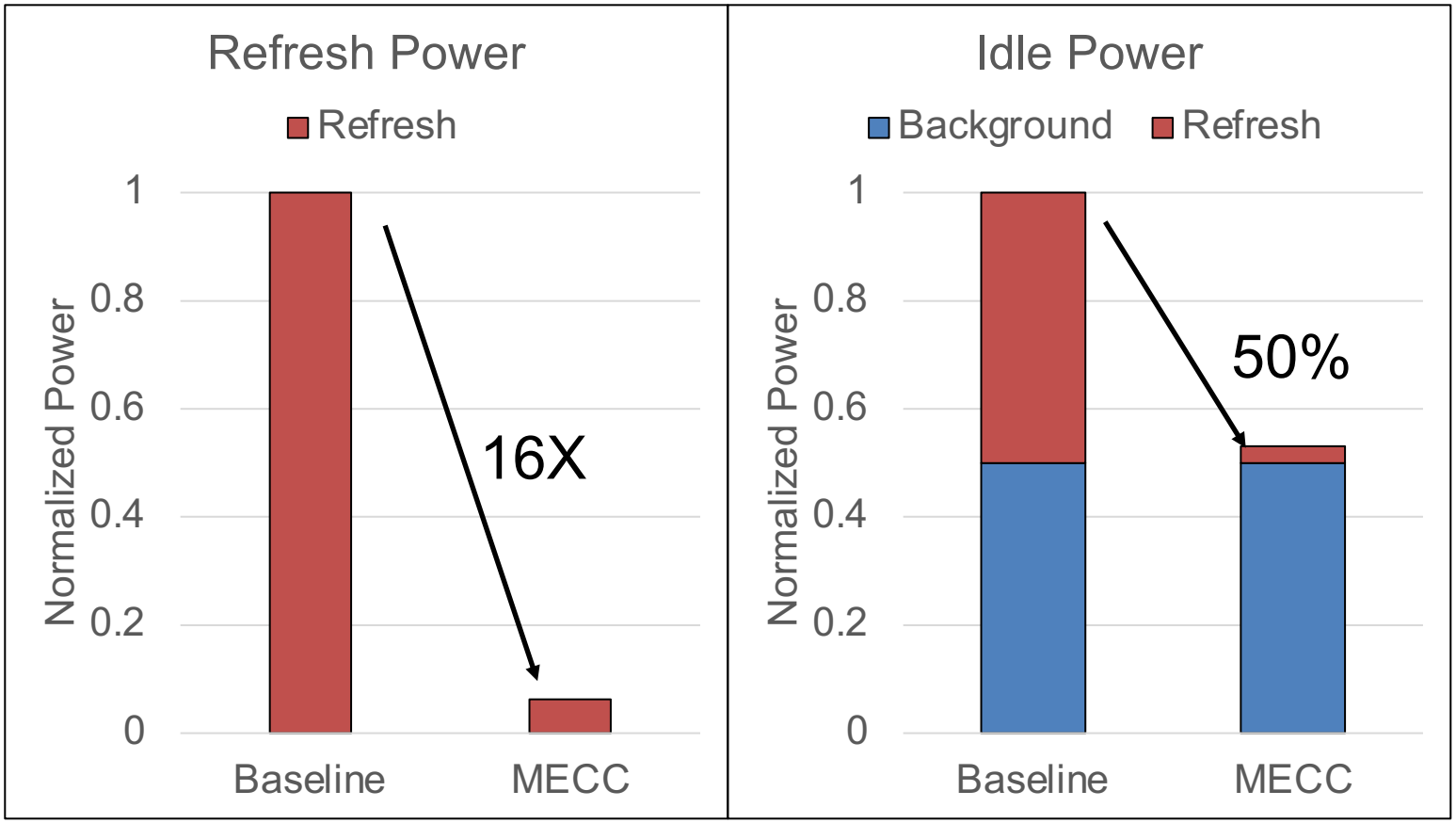


PERFORMANCE IN ACTIVE MODE



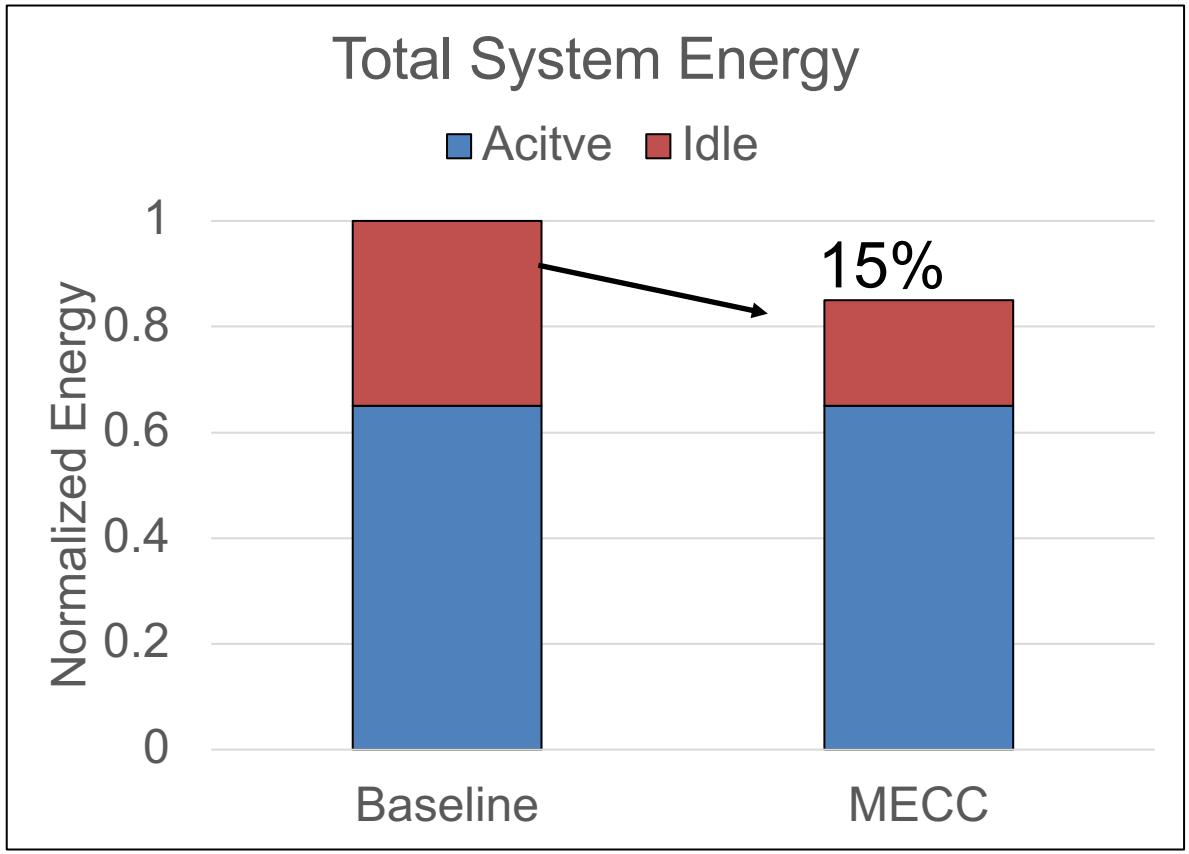
MECC limits the degradation within 2%

POWER SAVING IN IDLE MODE



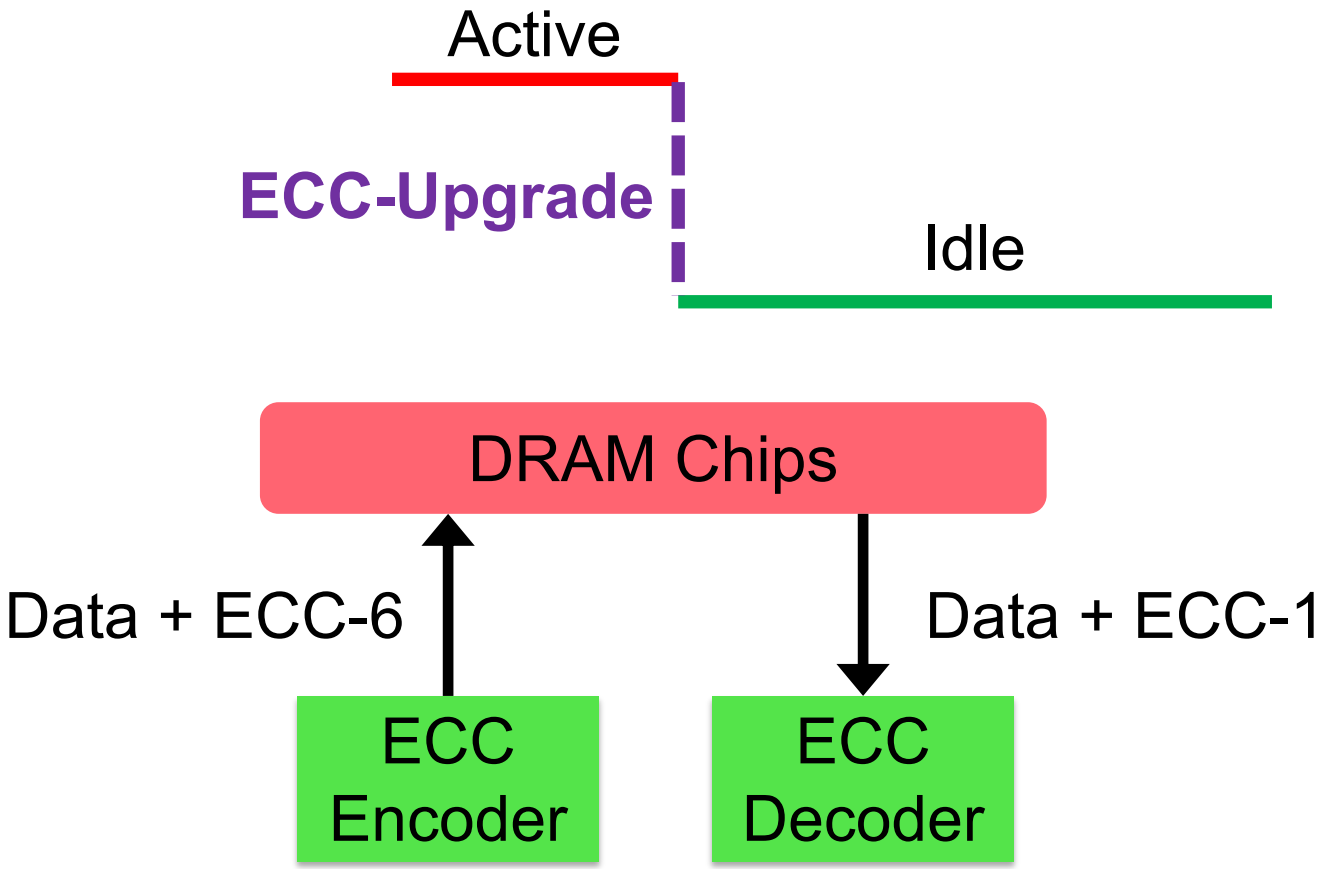
MECC saves idle power by 50%

TOTAL ENERGY SAVINGS

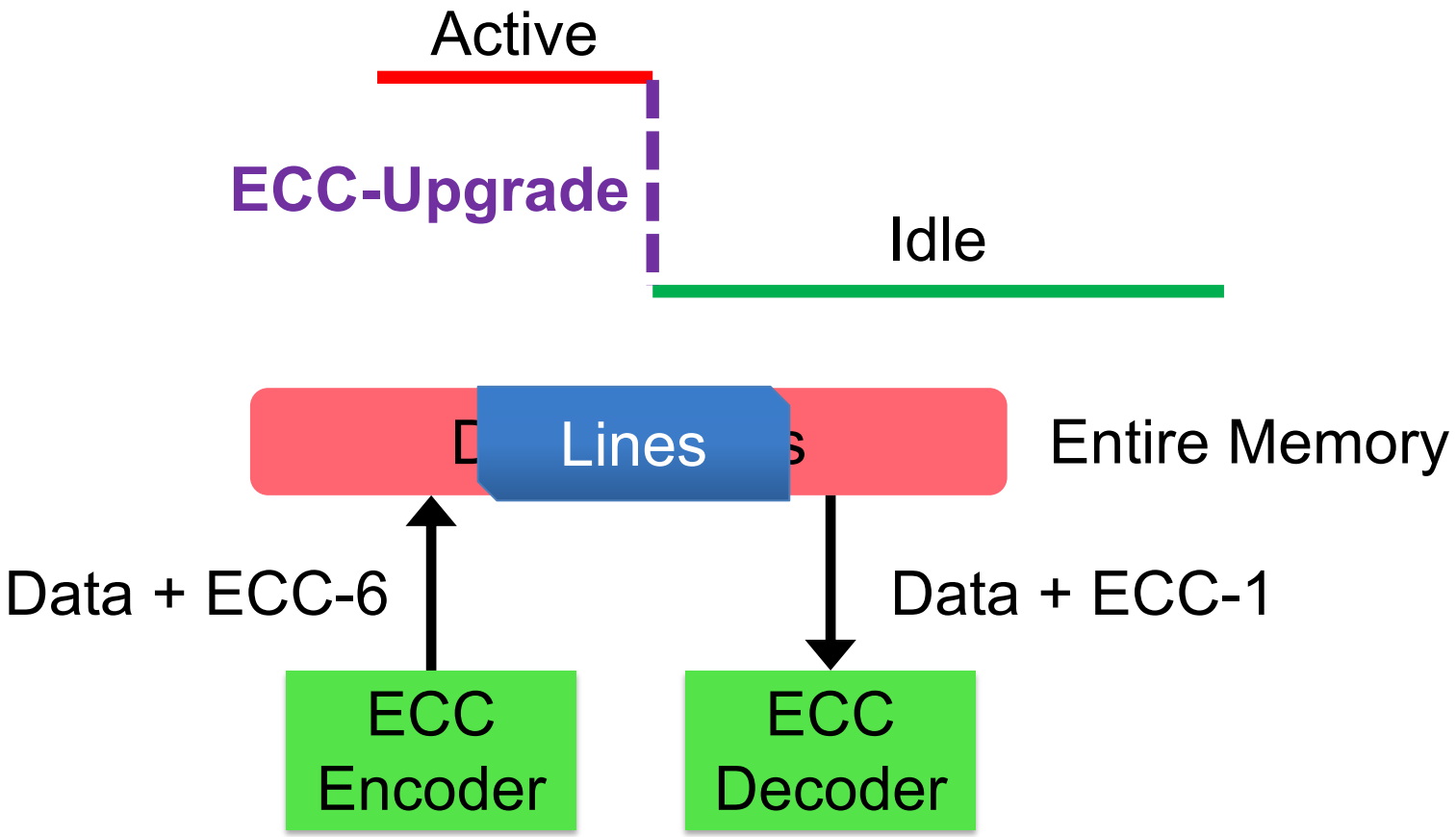


MECC saves total energy by 15%

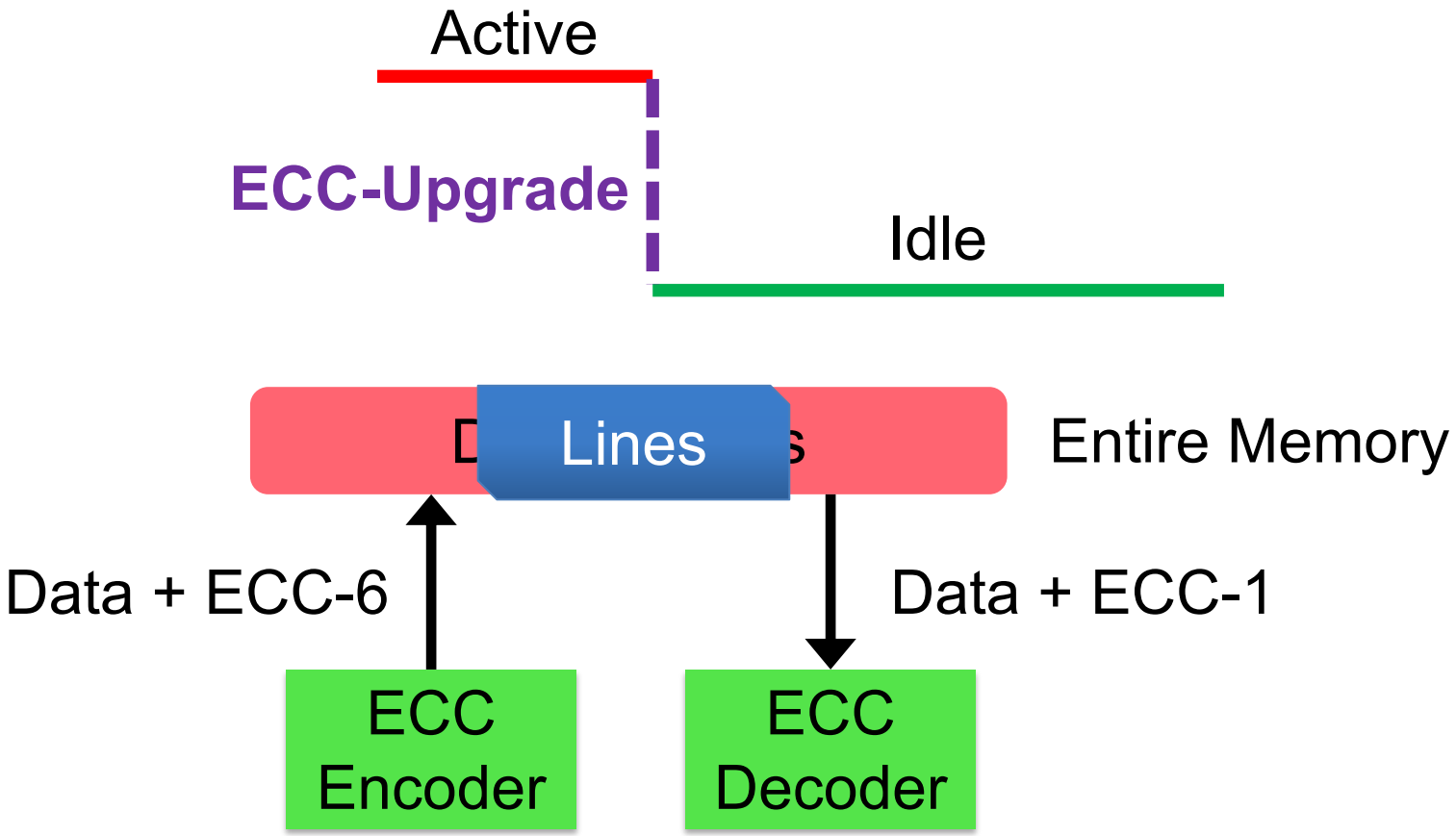
ECC-UPGRADE


Active
ECC-Upgrade
Idle
DRAM Chips
Data + ECC-6
Data + ECC-1
ECC Encoder
ECC Decoder

ECC-UPGRADE

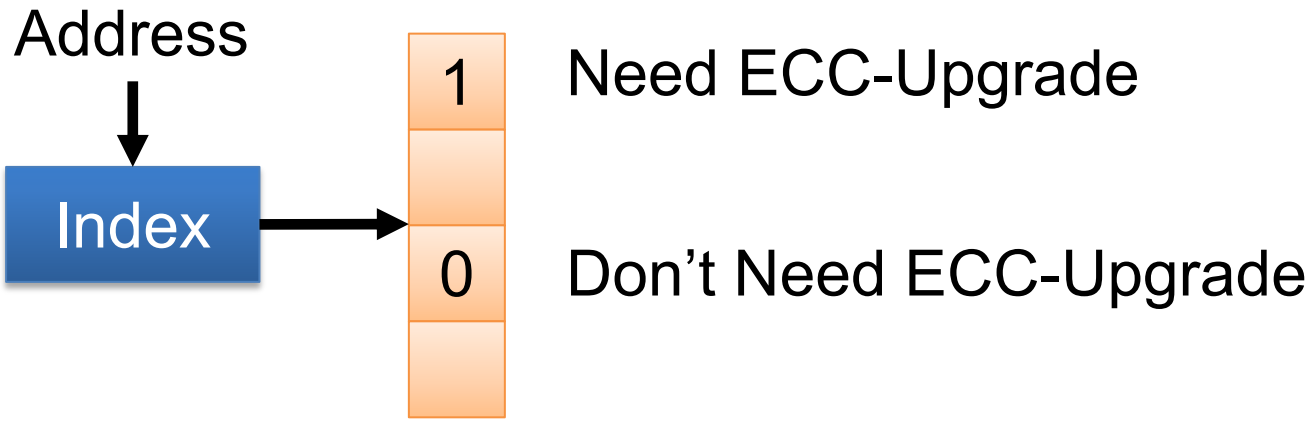

Active
ECC-Upgrade
Idle
Lines
Entire Memory
Data + ECC-6
Data + ECC-1
ECC Encoder
ECC Decoder

ECC-UPGRADE

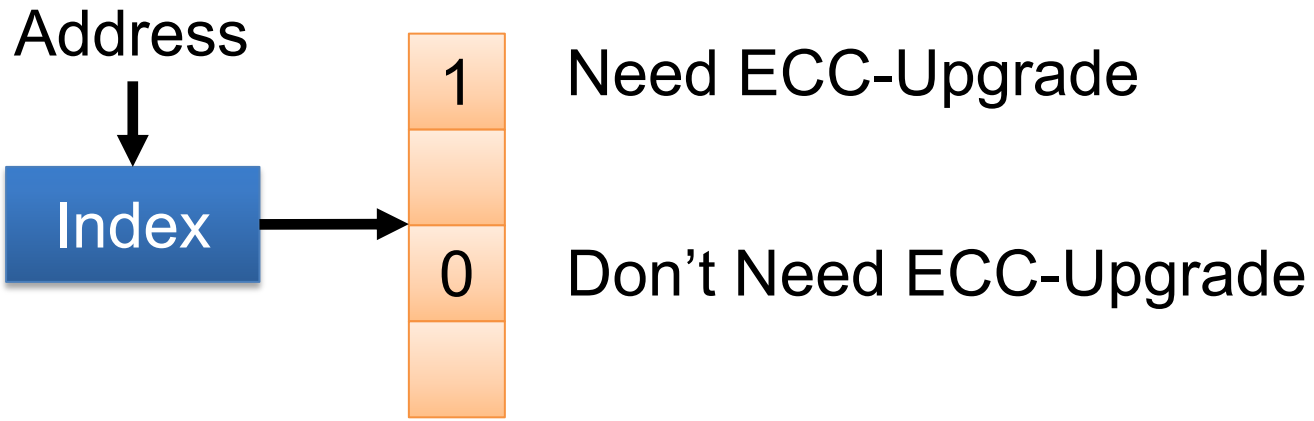


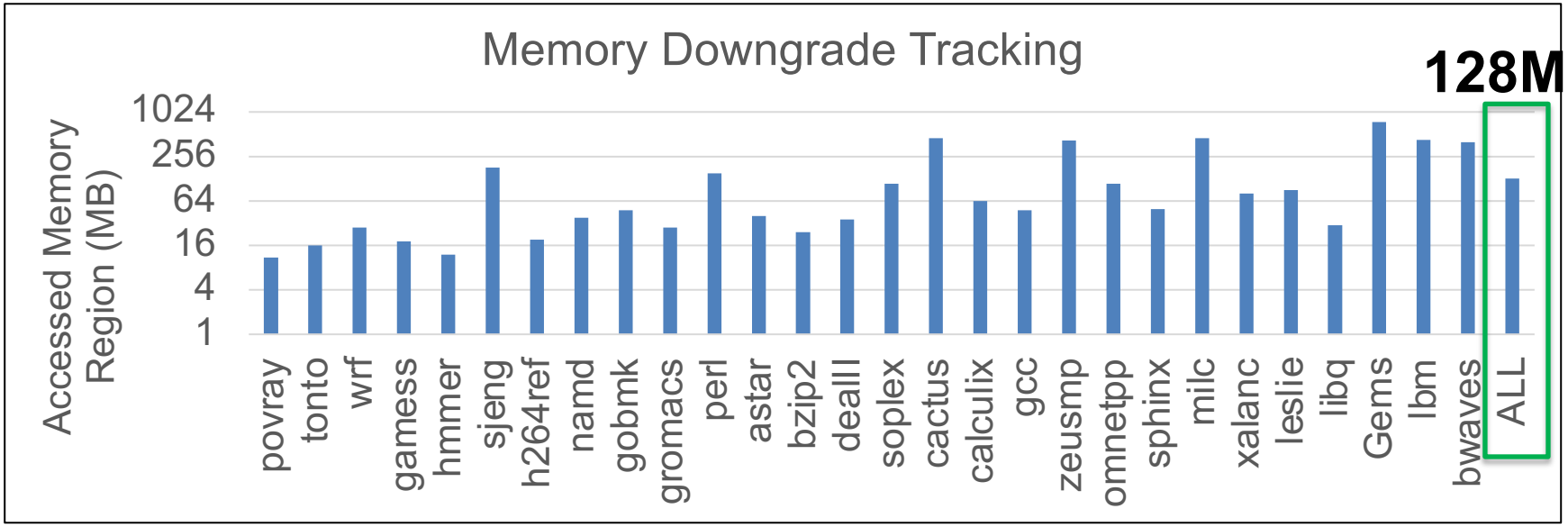
Can we enhance the ECC-Upgrade?

MEMORY DOWNGRADE TRACKING (MDT)



MEMORY DOWNGRADE TRACKING (MDT)





MDT avoids unnecessary ECC-Upgrades

FREQUENT TRANSITION OF ECC STATES

courtesy: Samsung, Bluetooth, Facebook, Twitter

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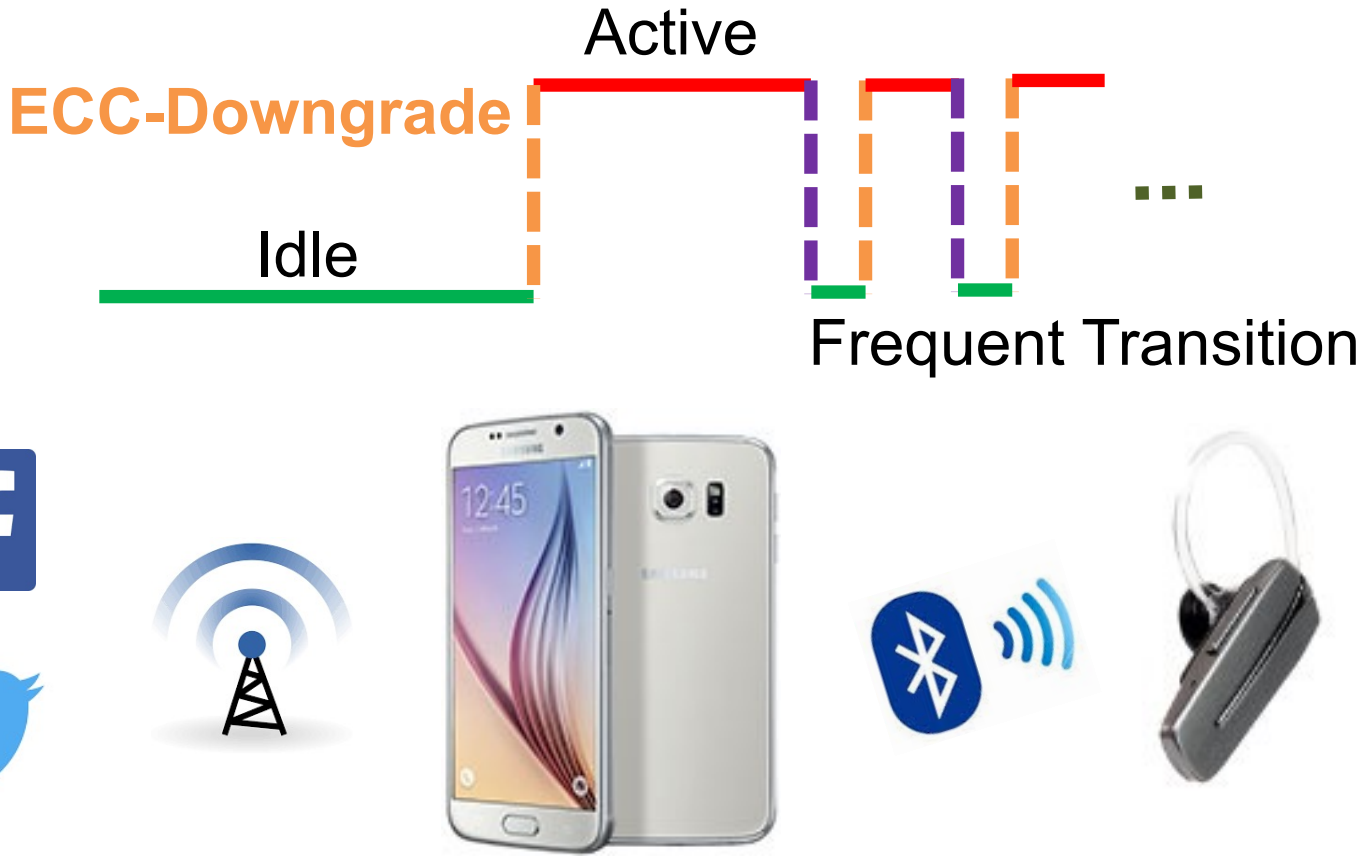
FREQUENT TRANSITION OF ECC STATES



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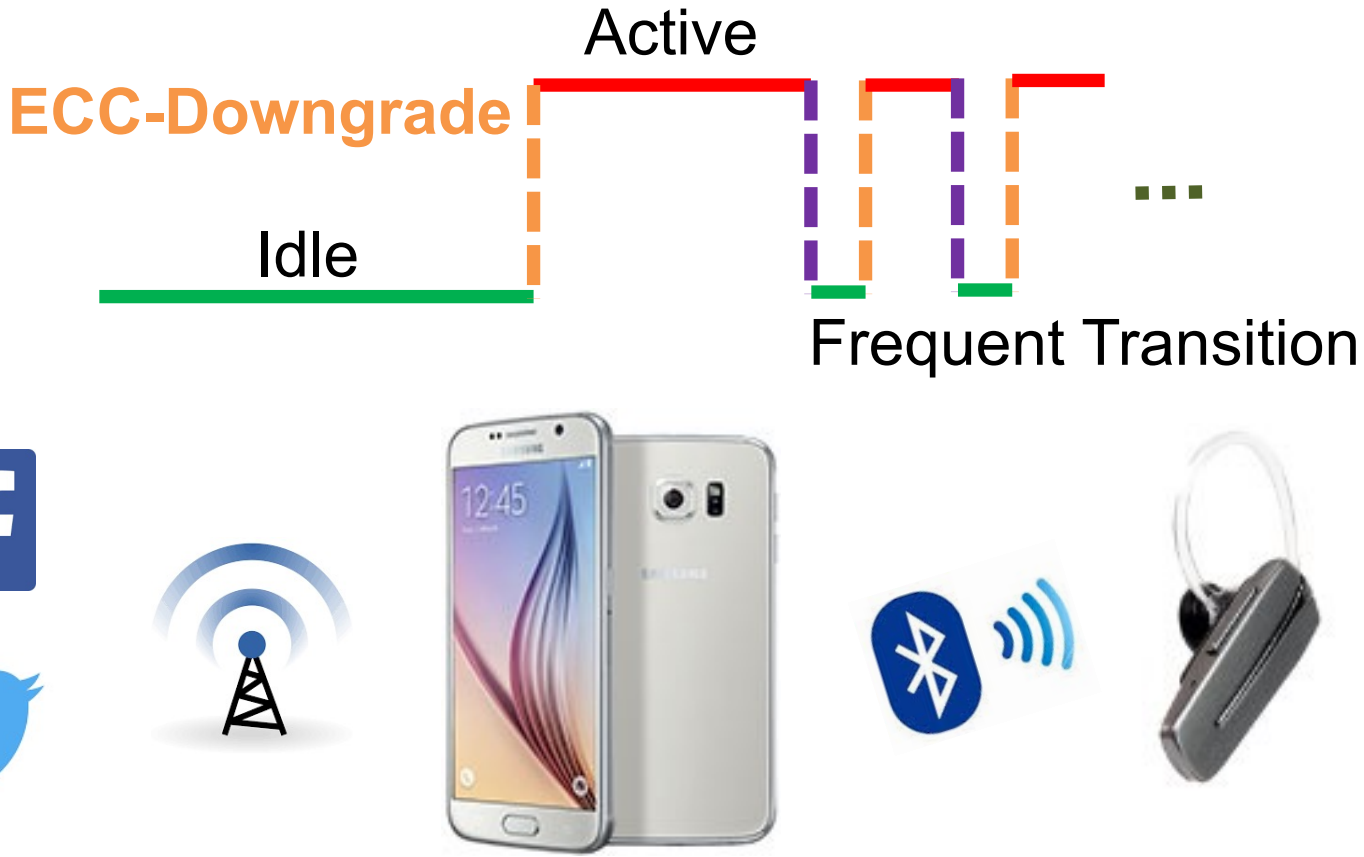
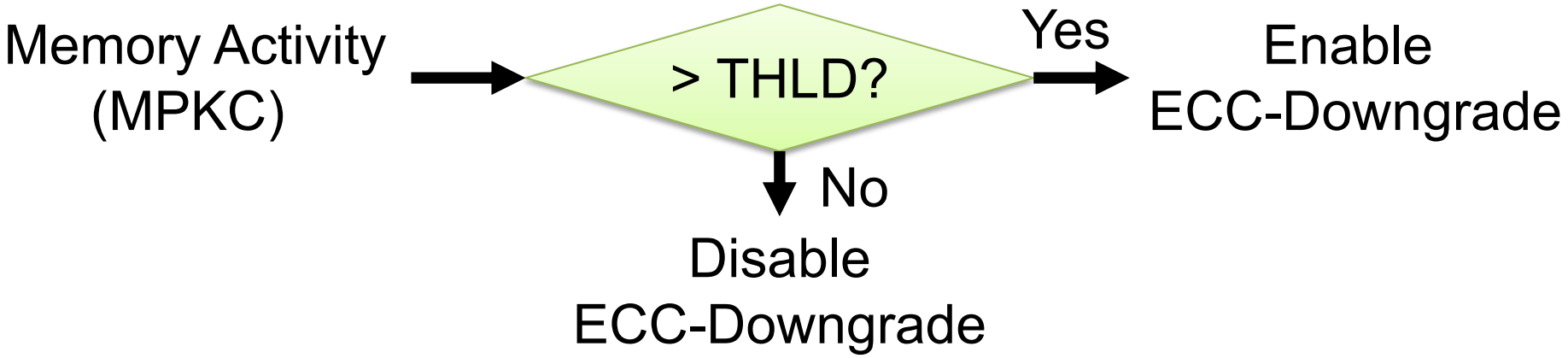
FREQUENT TRANSITION OF ECC STATES



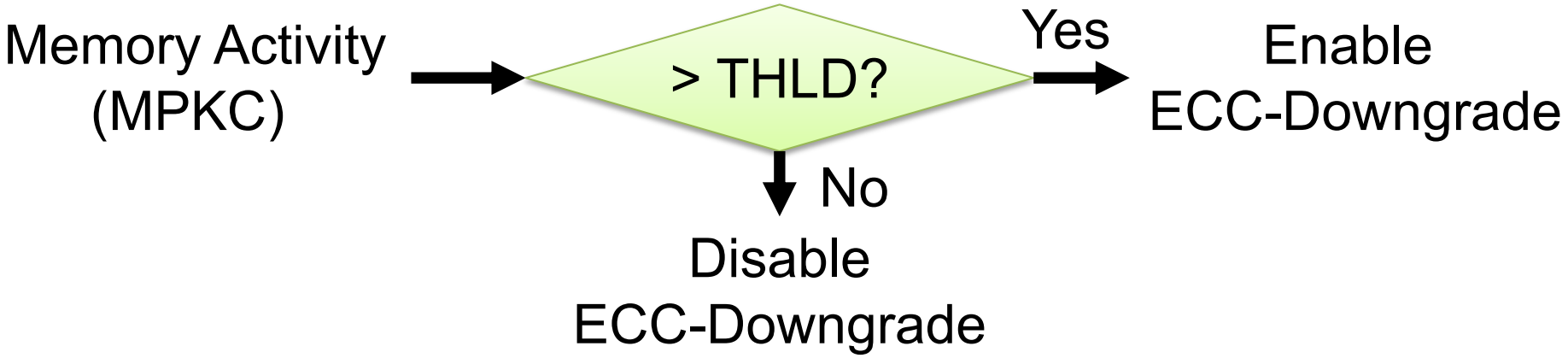
Can we enhance the ECC-Downgrade?

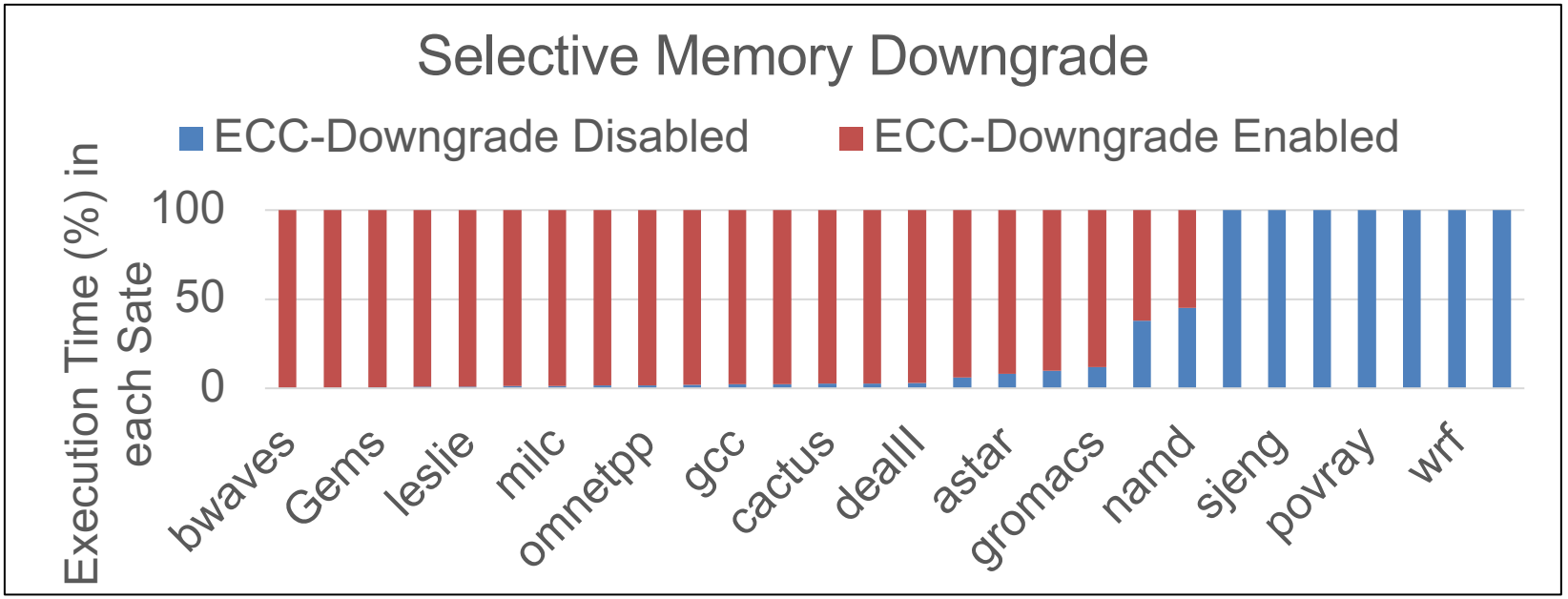
courtesy: Samsung, Bluetooth, Facebook, Twitter

SELECTIVE MEMORY DOWNGRADE (SMD)

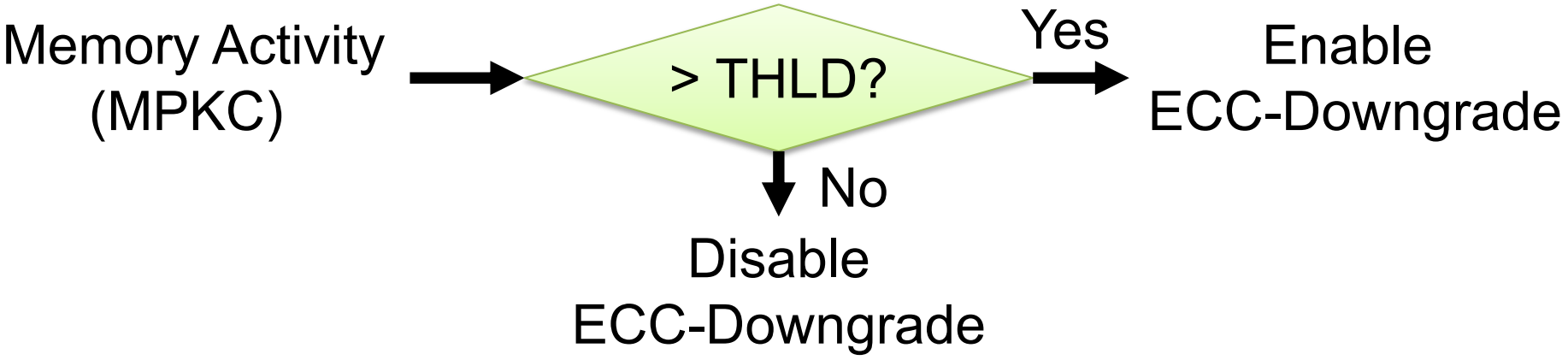


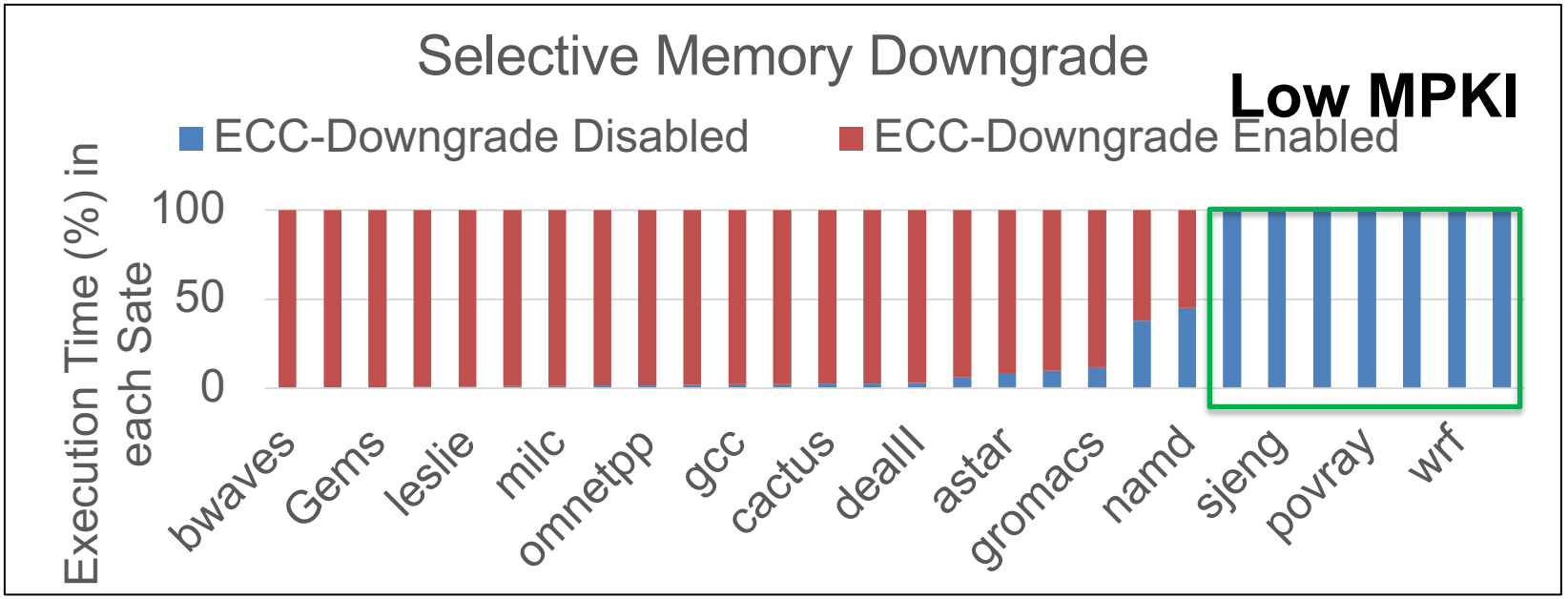
SELECTIVE MEMORY DOWNGRADE (SMD)





SELECTIVE MEMORY DOWNGRADE (SMD)





SMD avoids frequent transition of ECCs

EXECUTIVE SUMMARY

- Energy consumption determines the usability of emerging mobile computing devices
- DRAM refresh operations accounts for significant fraction of memory system's energy

	Strong ECC	Weak ECC
Active Mode (refresh power negligible)	Bad Performance	**Good Performance**
Idle Mode (performance not critical)	**Huge Energy Savings**	No Energy Saving

- Results: -50% idle power, -15% overall energy, with only 2% performance degradation

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Morphable ECC

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REDUCING REFRESH POWER IN MOBILE DEVICES WITH MORPHABLE ECC

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06/24/2015
Rio de Janeiro, Brazil

Chiachen Chou, Georgia Tech

Prashant Nair, Georgia Tech

Moinuddin K. Qureshi, Georgia Tech