Touché : Towards Ideal and Efficient Cache Compression By Mitigating Tag Area Overheads

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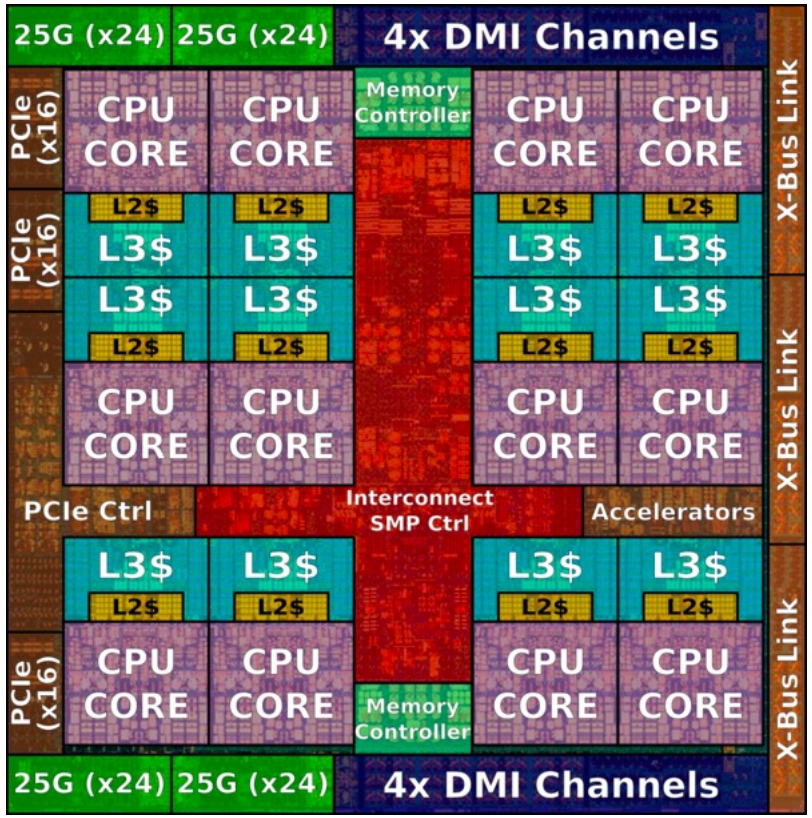
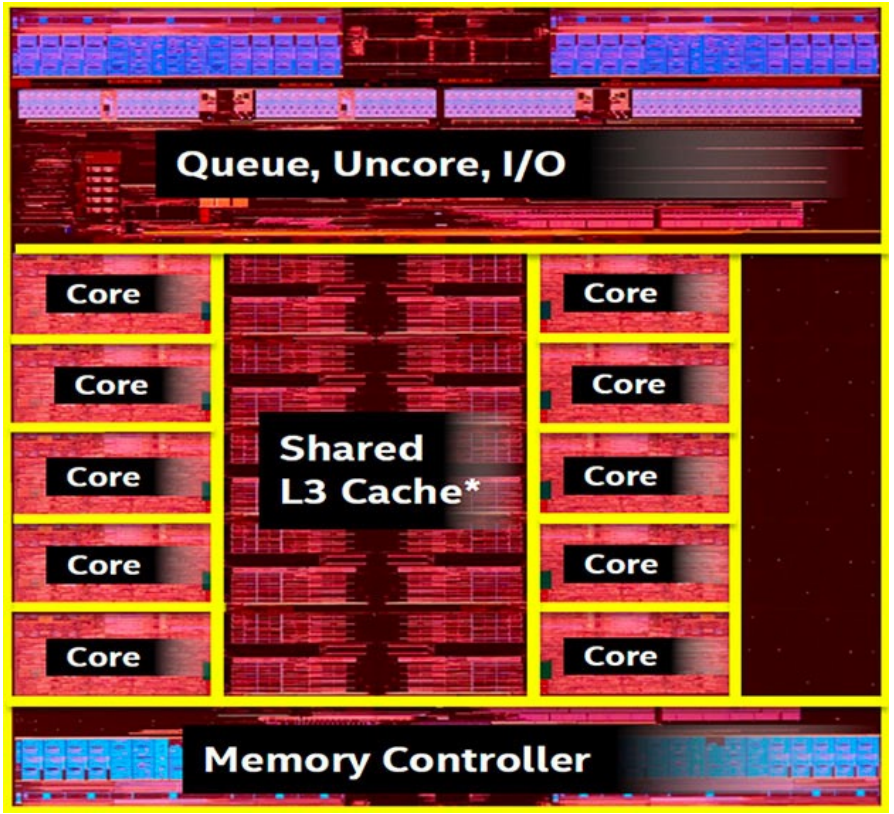
KNU IBM Research UBC

Last-Level Cache: Why Size Matters?

Last-Level Cache (LLC) is shared, occupies significant chip area



IBM Power 9



Intel i7

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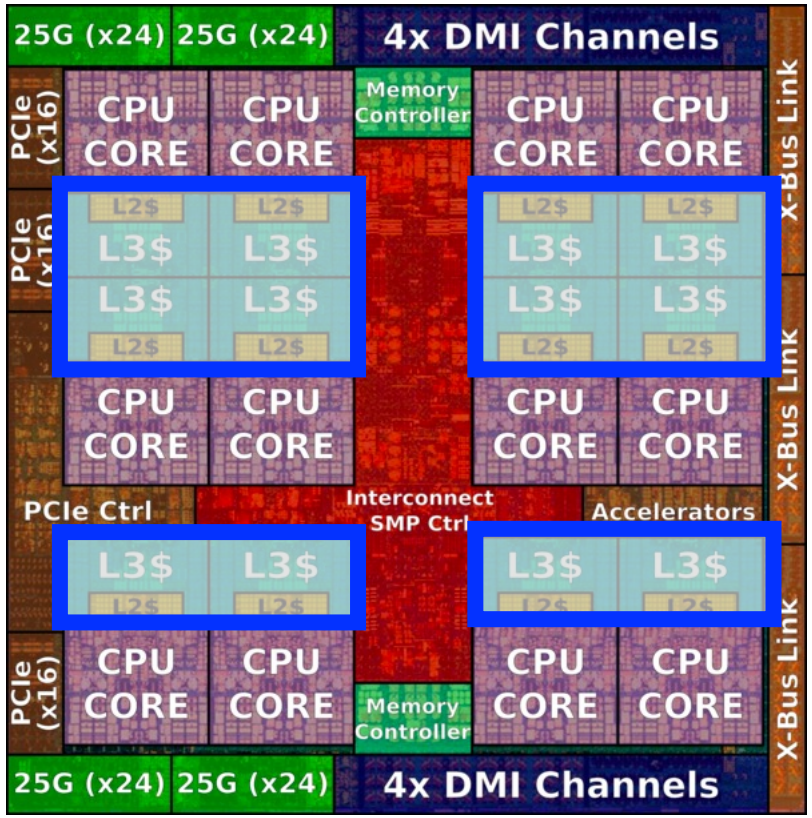

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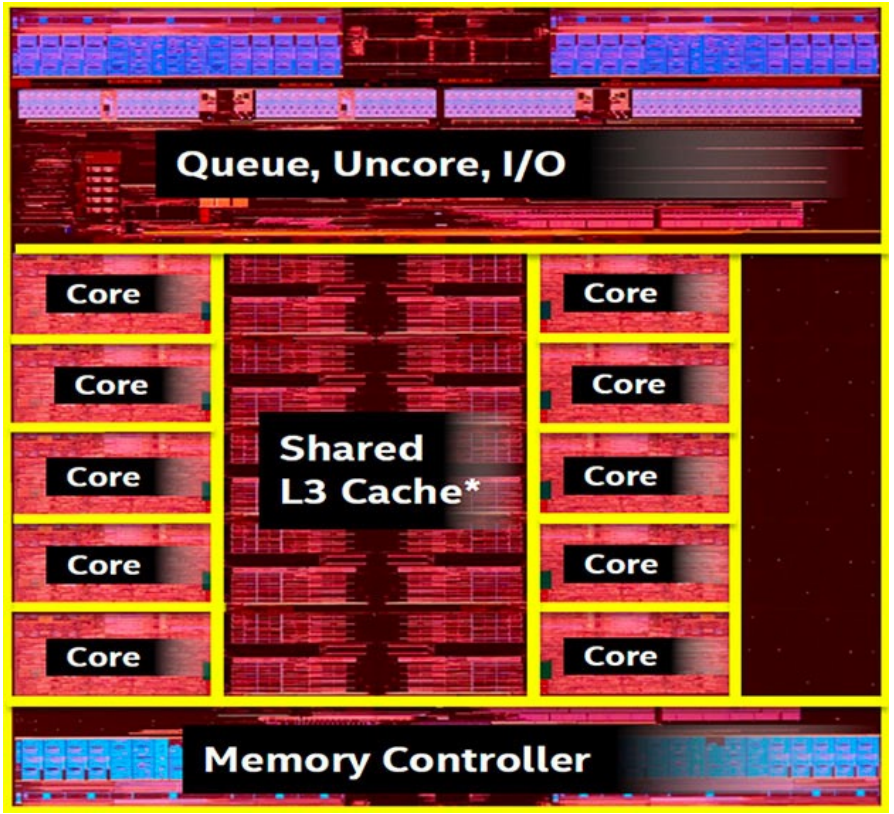

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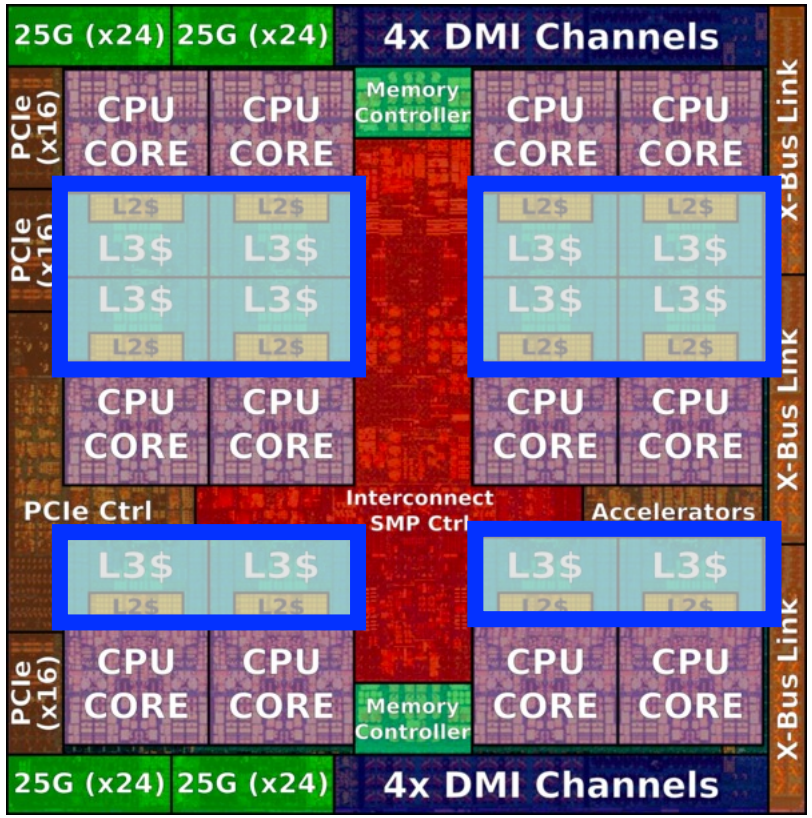

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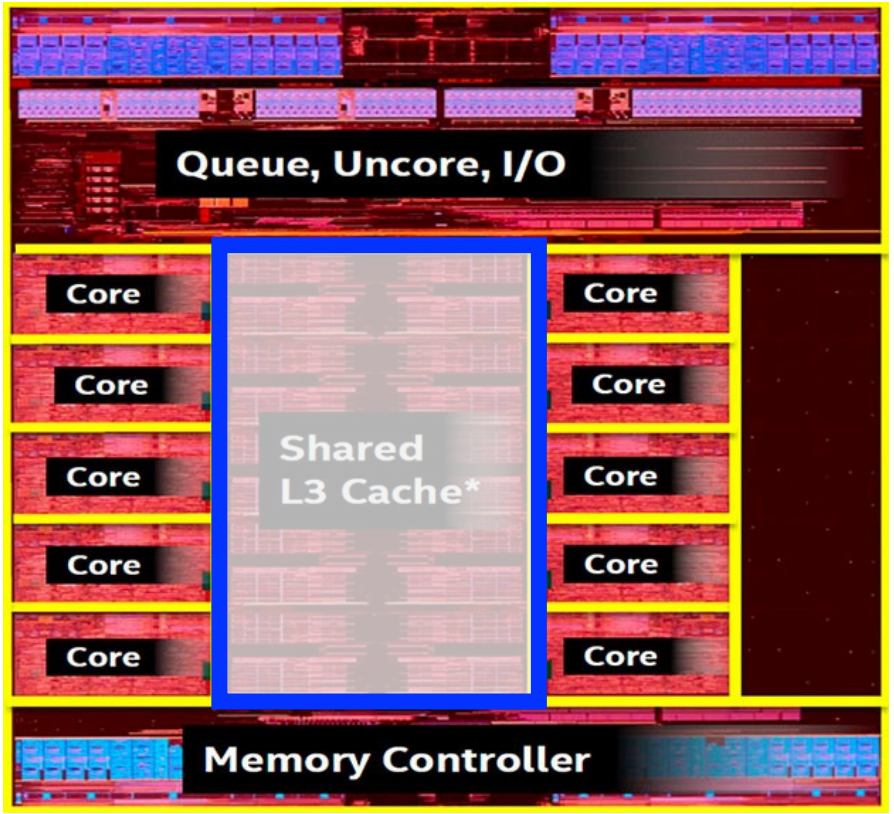

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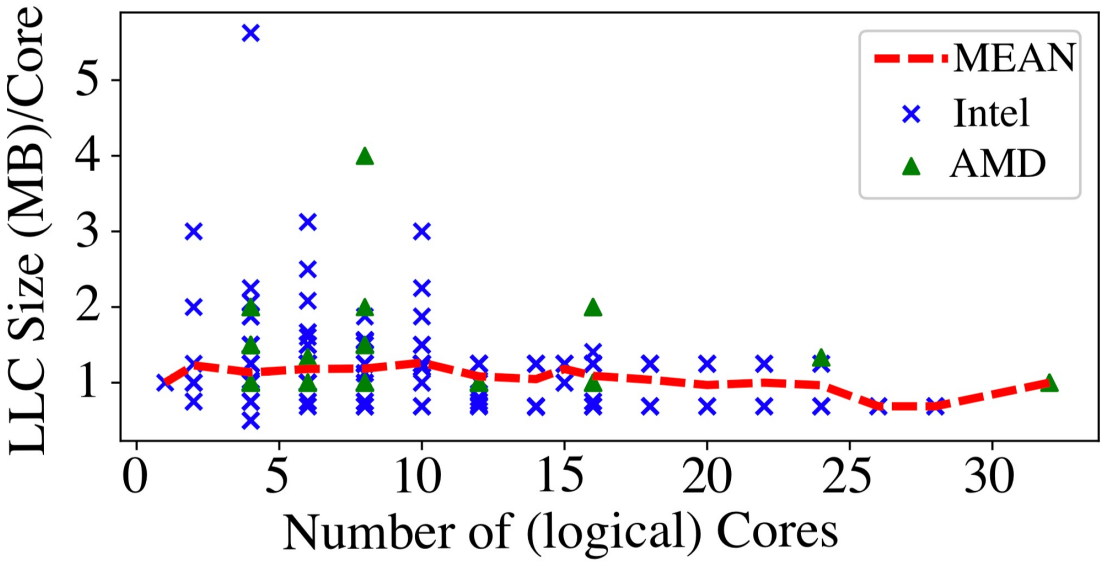
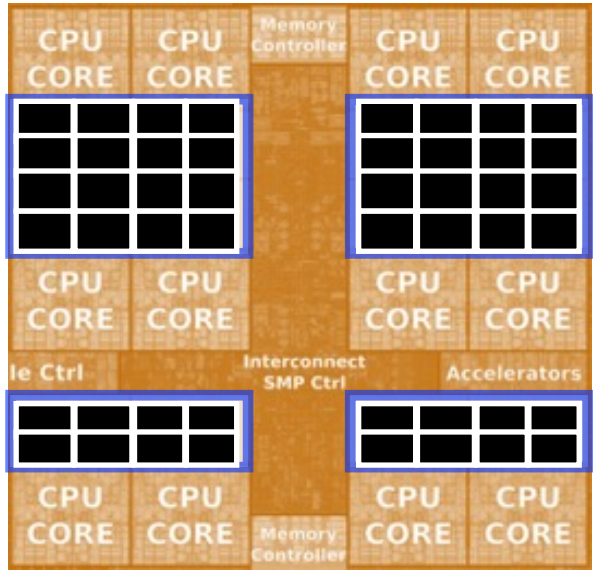


LLC Capacity/Core ➡ Stagnant

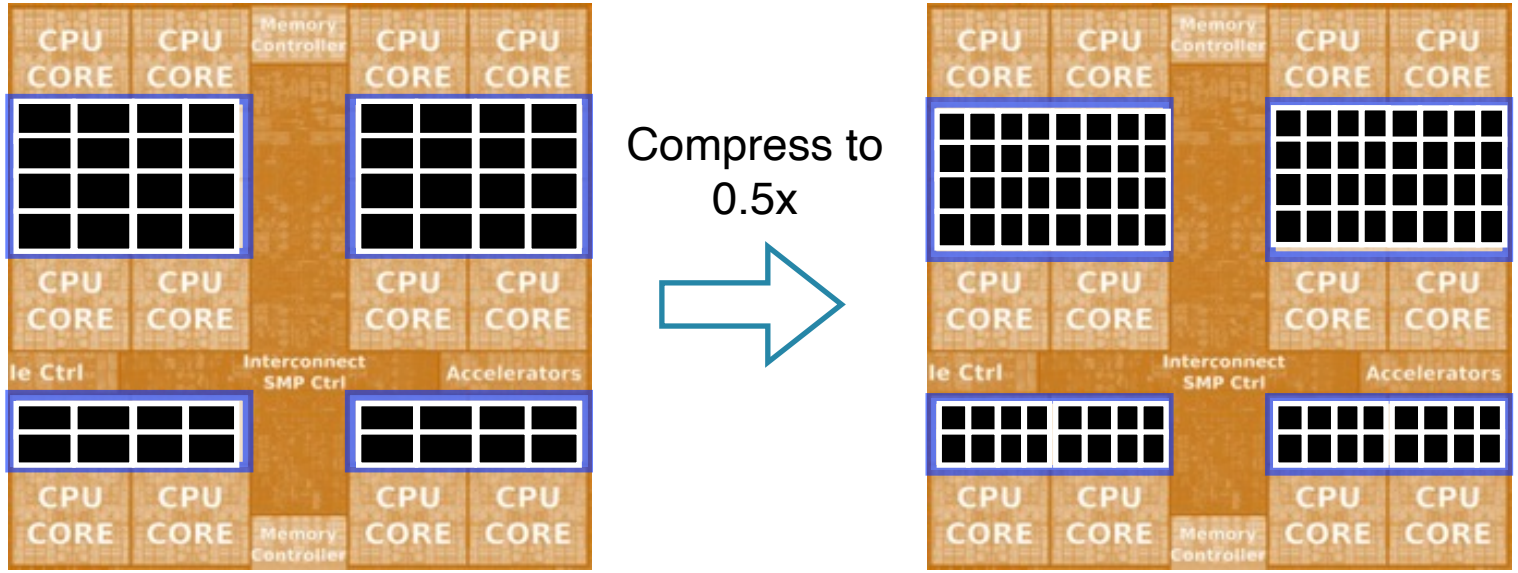
Bigger Applications

Cache Compression Can Save The Day!



With data compression, we can improve the effective LLC Capacity

Cache Compression Can Save The Day!



2x effective capacity

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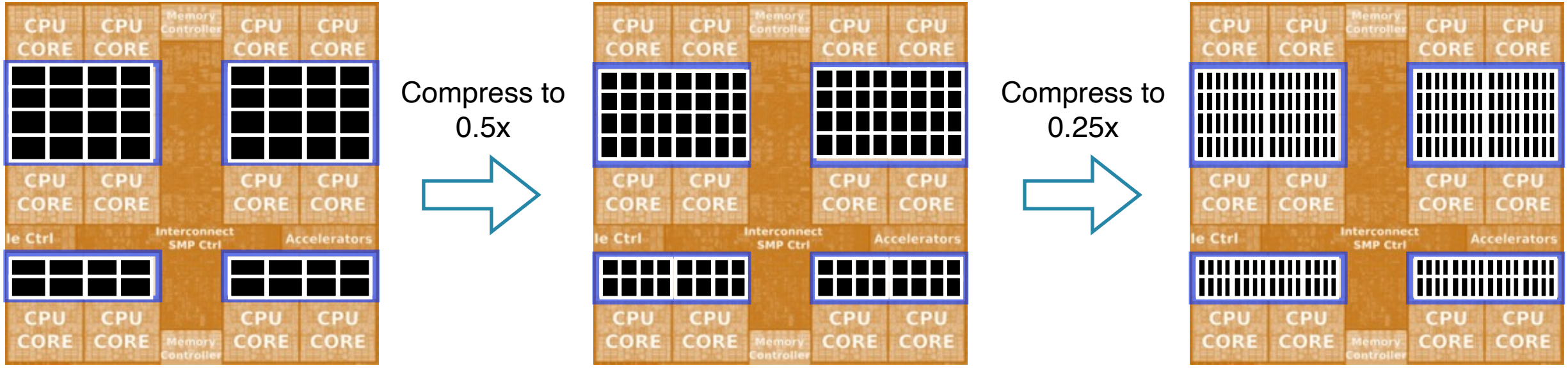
Cache Compression Can Save The Day!



2x effective capacity

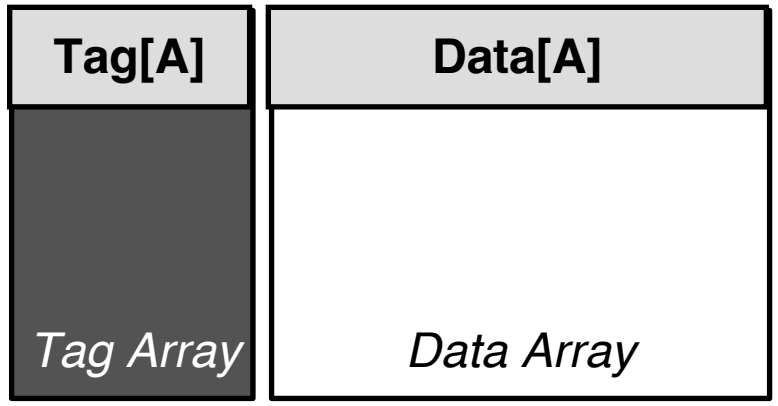
4x effective capacity

With data compression, we can improve the effective LLC Capacity

Cache Compression Can Save The Day!

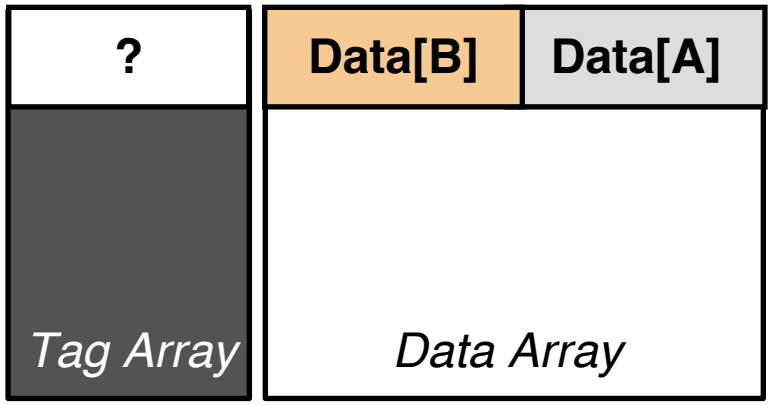
BUT, there is a catch!

Cache Compression: Tradeoffs



Uncompressed Cache

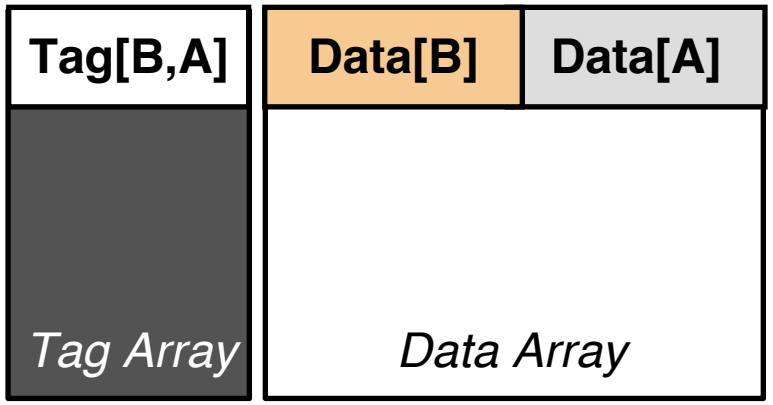
Cache Compression: Tradeoffs



Compressed Cache

Cache Compression: Tradeoffs

IDEAL COMPRESSION



No Additional Area Overheads

Cache Compression: Tradeoffs

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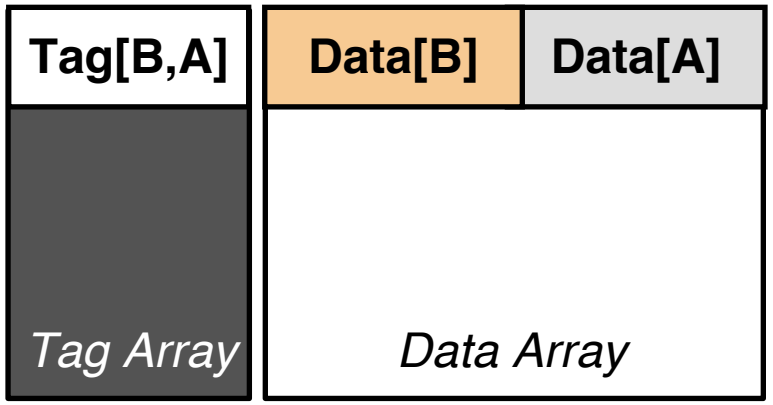

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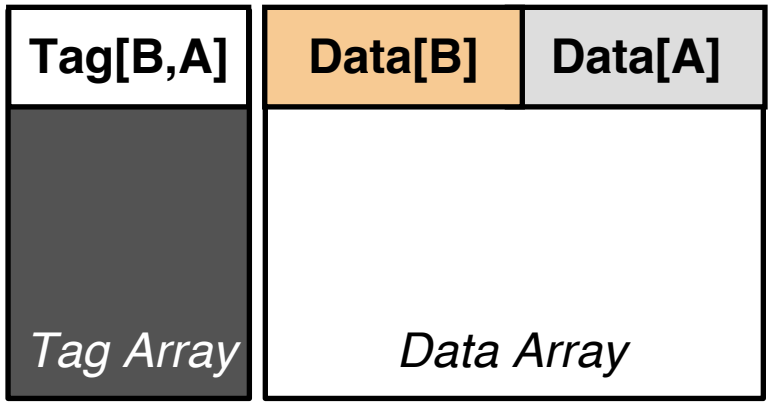

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PRACTICAL COMPRESSION

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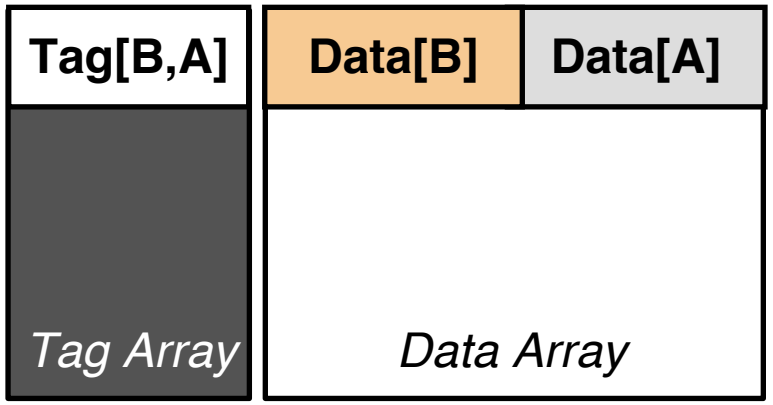

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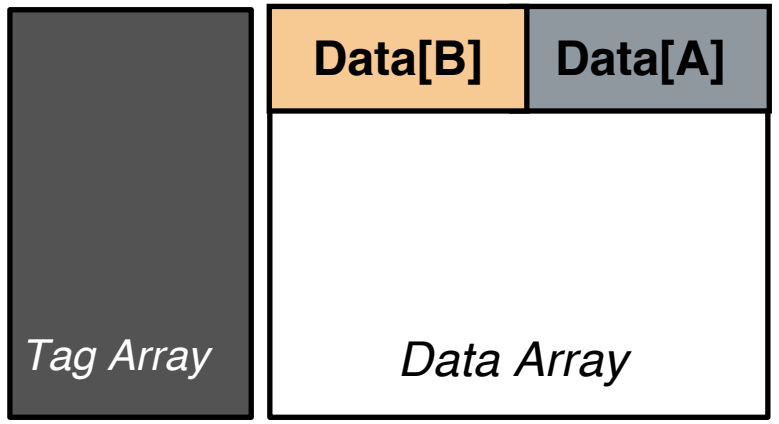

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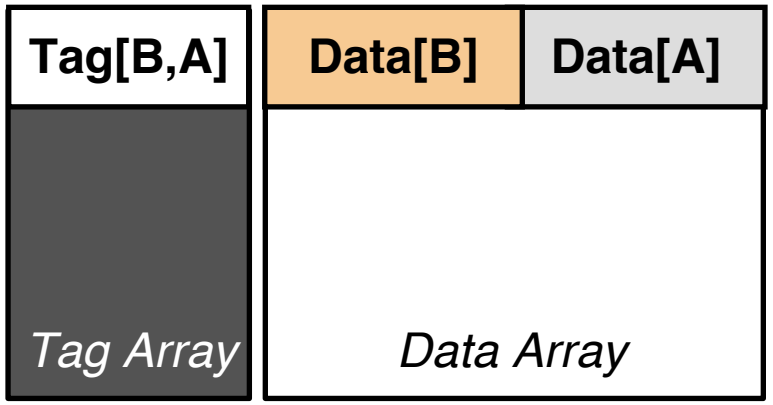

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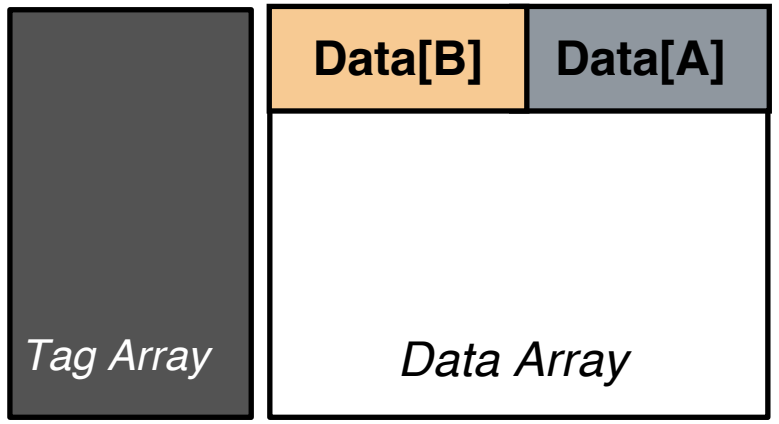
PRACTICAL COMPRESSION

Adding additional tag array



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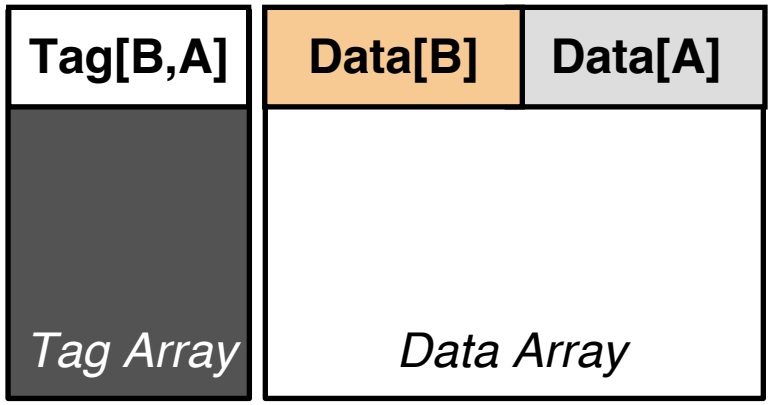

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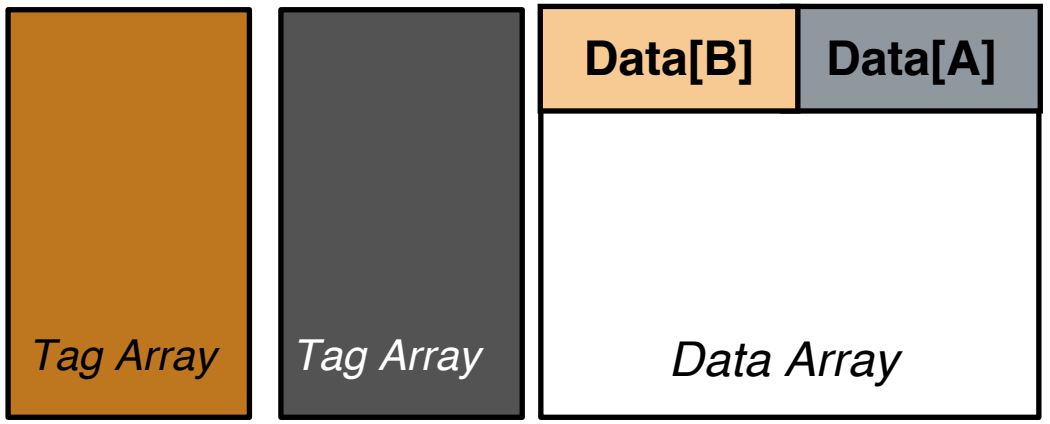

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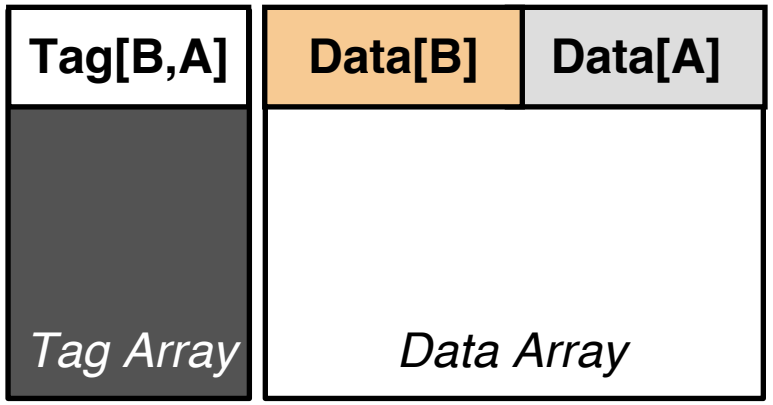

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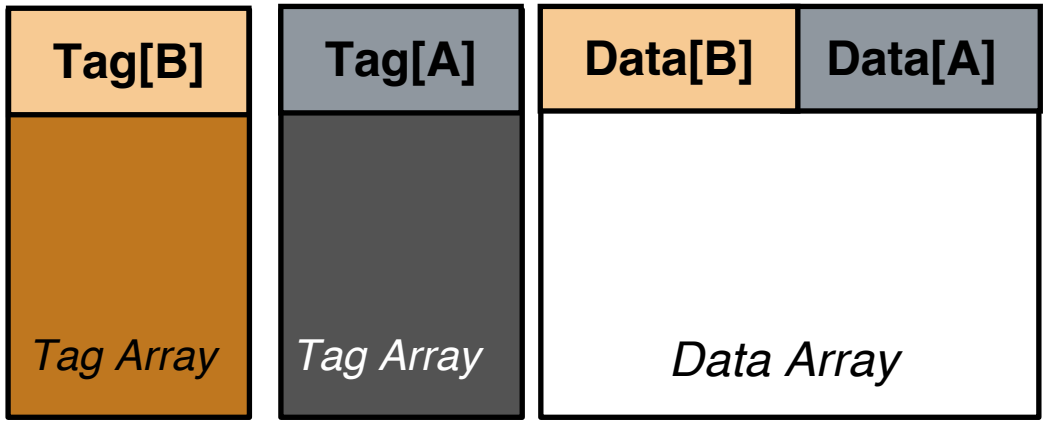

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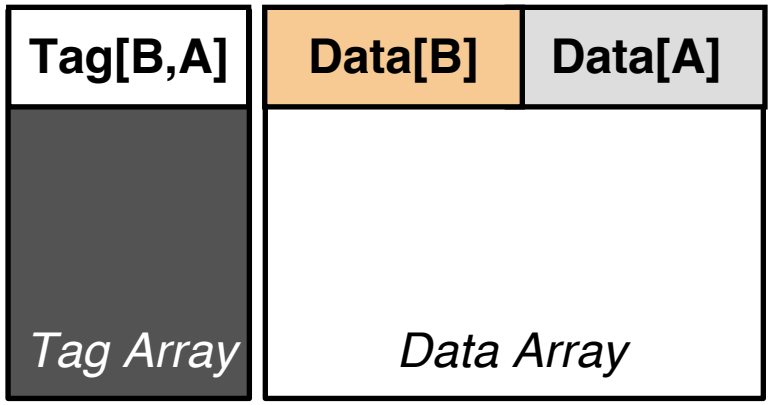

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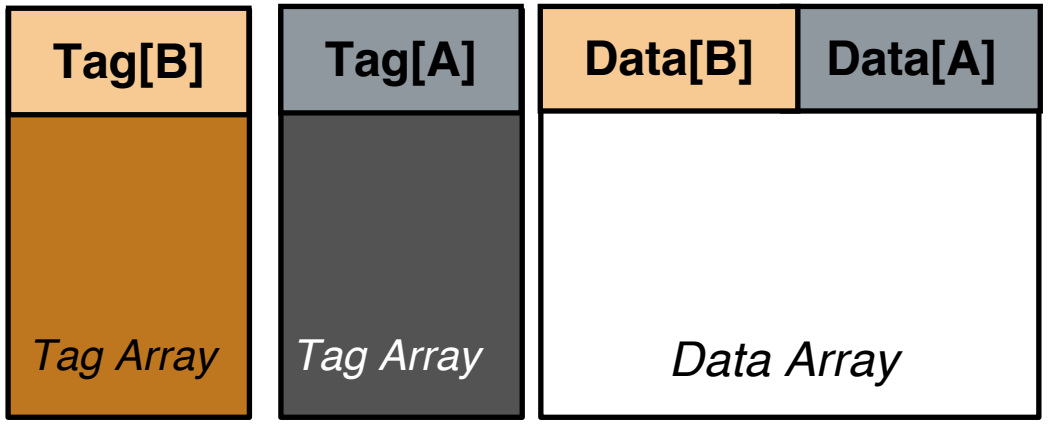

2x Tag Area

Cache Compression: Tradeoffs

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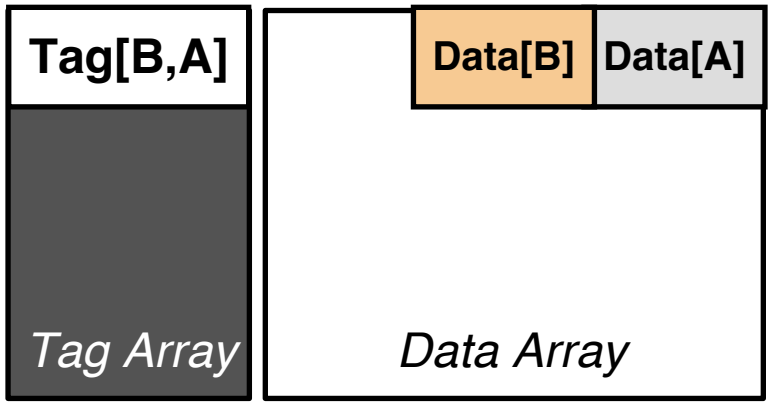

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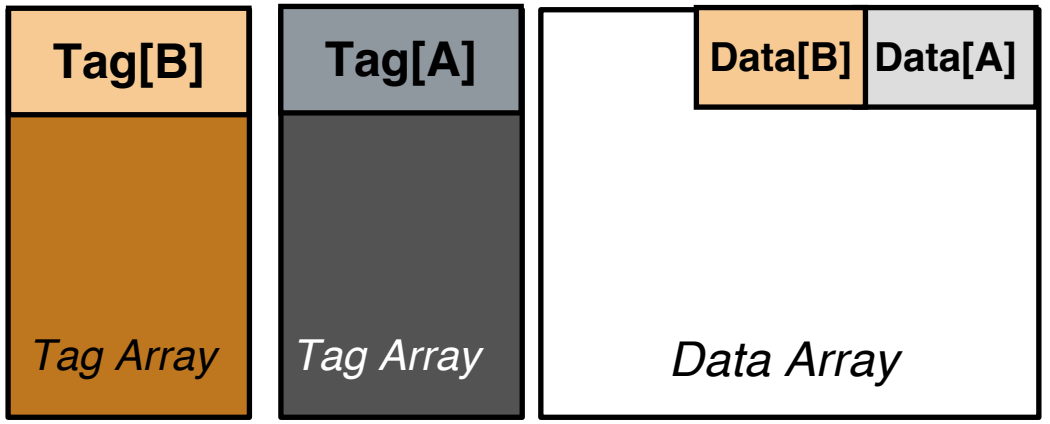

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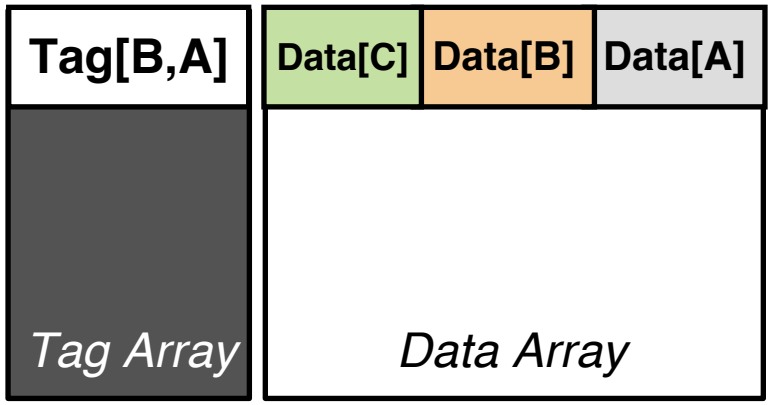

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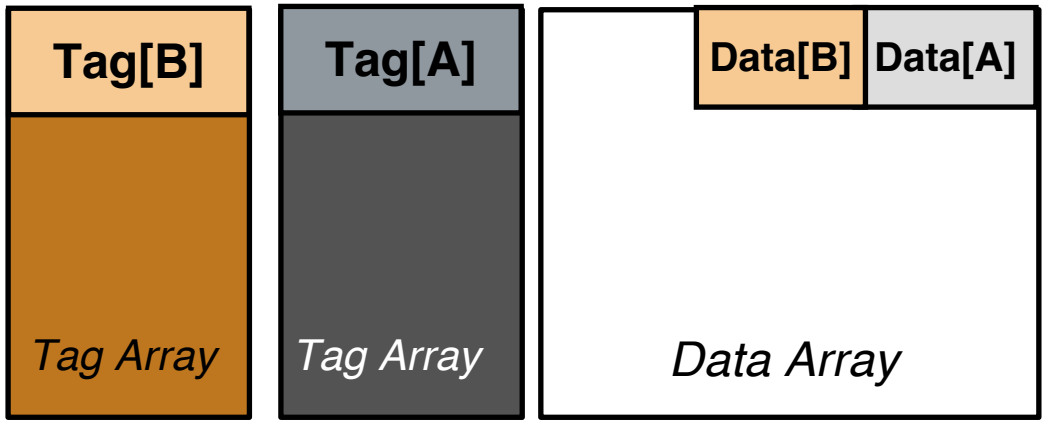

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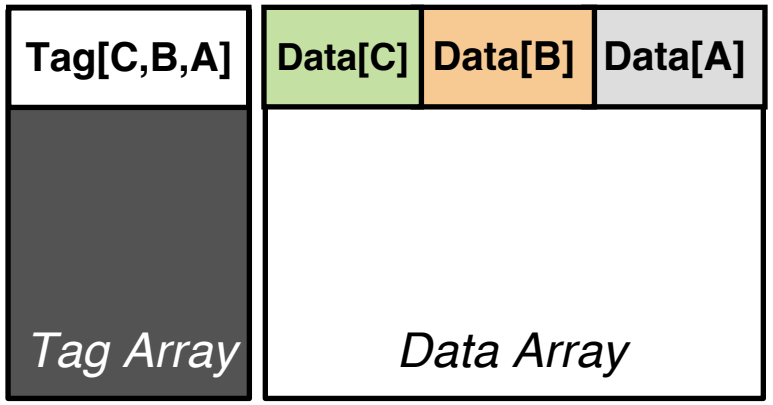

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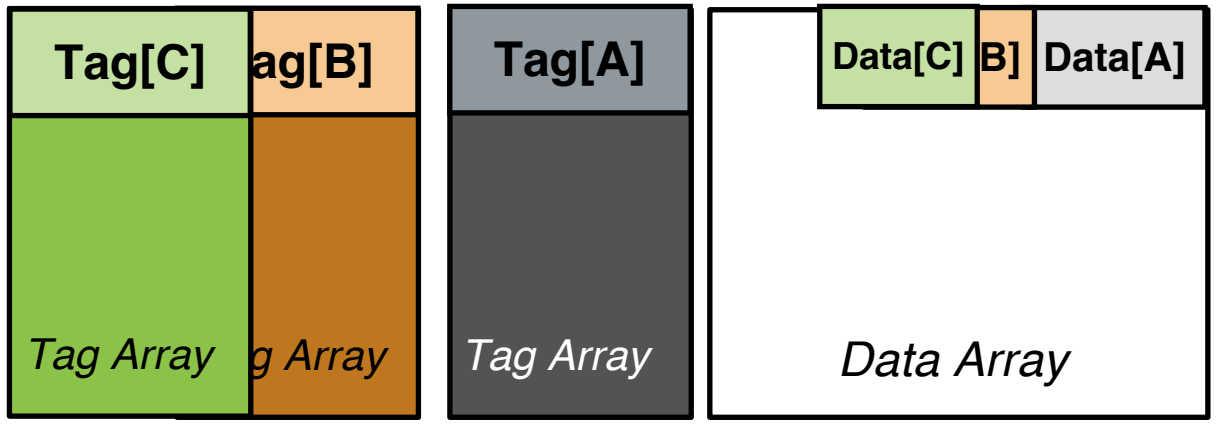

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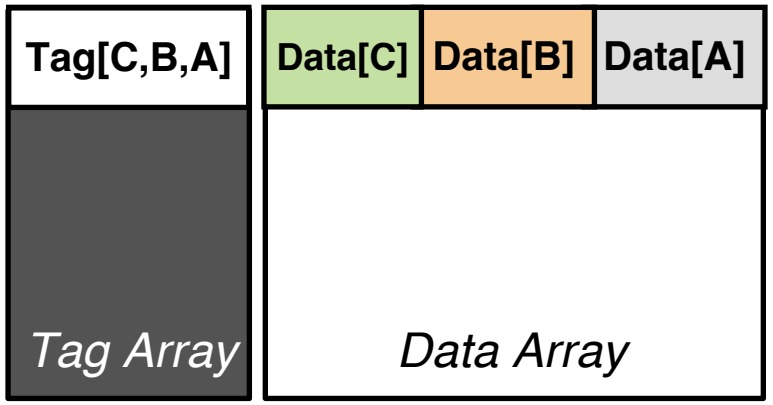

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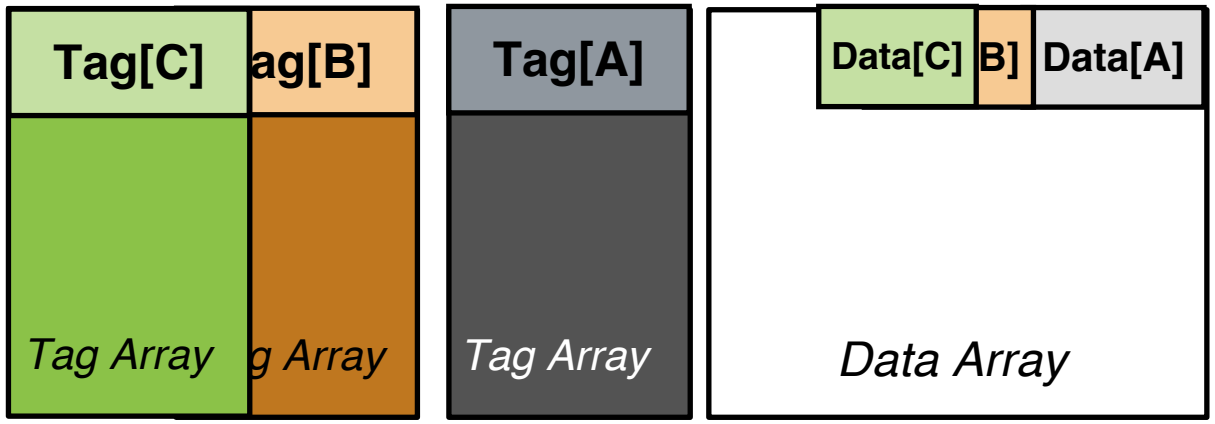

3x Tag Area

Cache Compression: Tradeoffs

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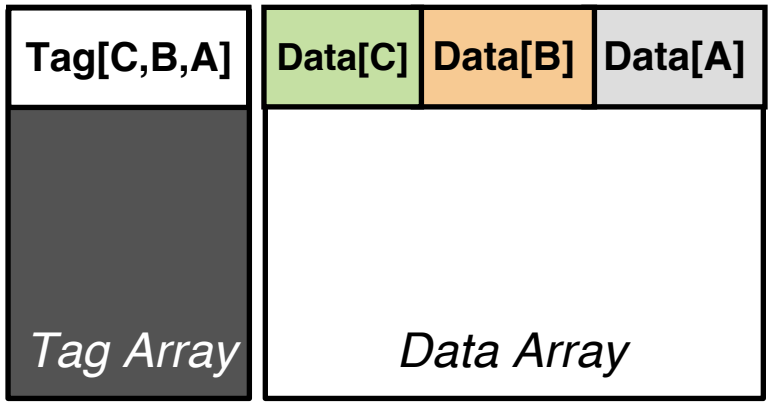

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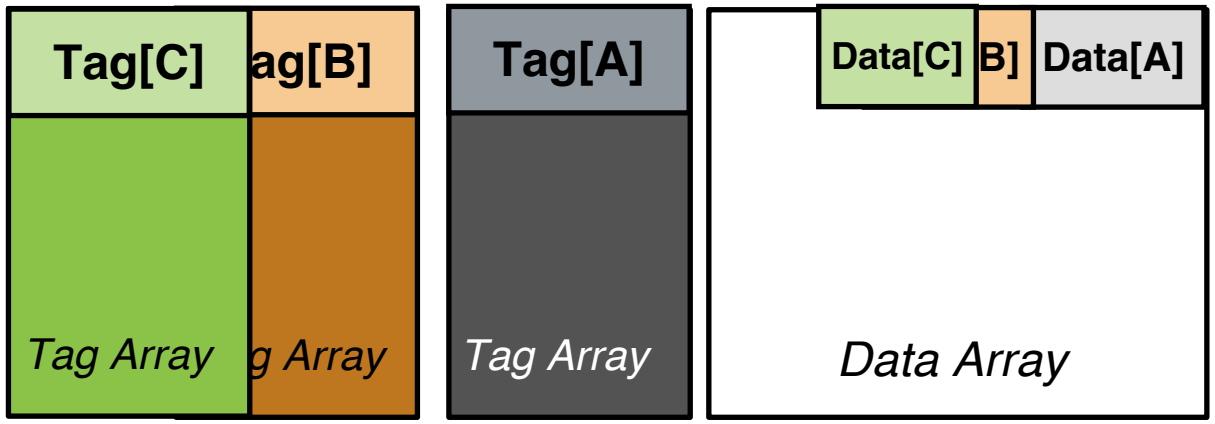

3x Tag Area

Difficult to decide the number of tag arrays at design time!

Cache Compression: Tradeoffs

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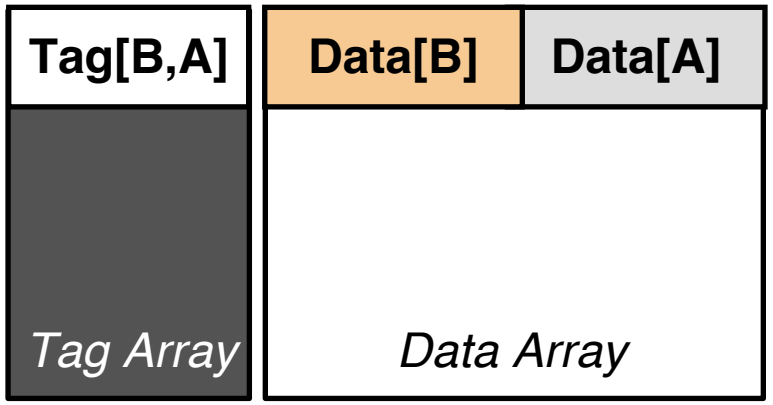

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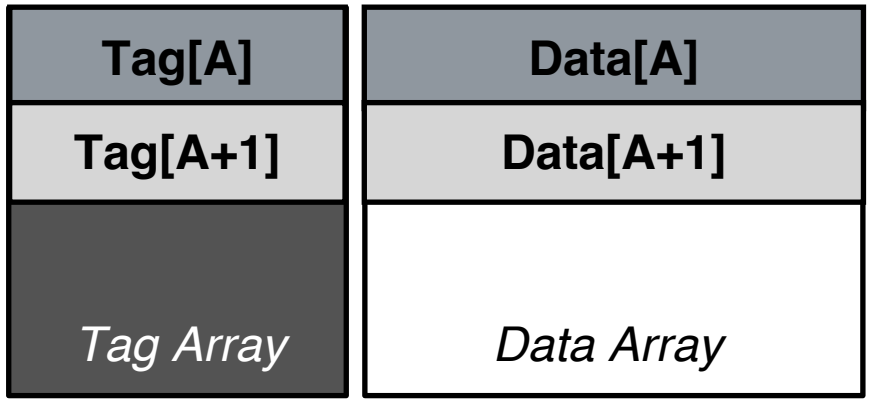

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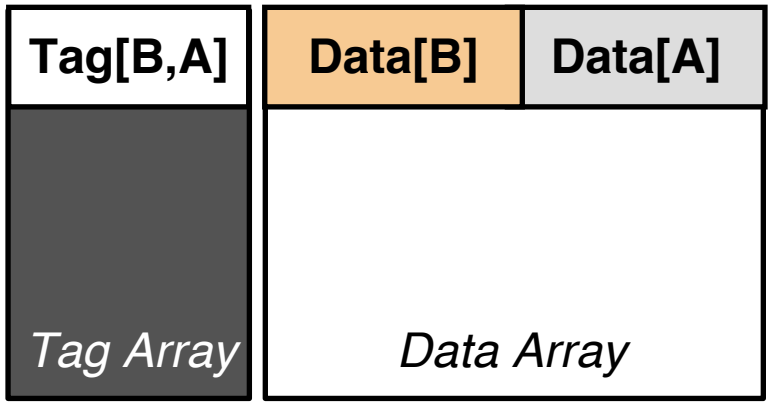

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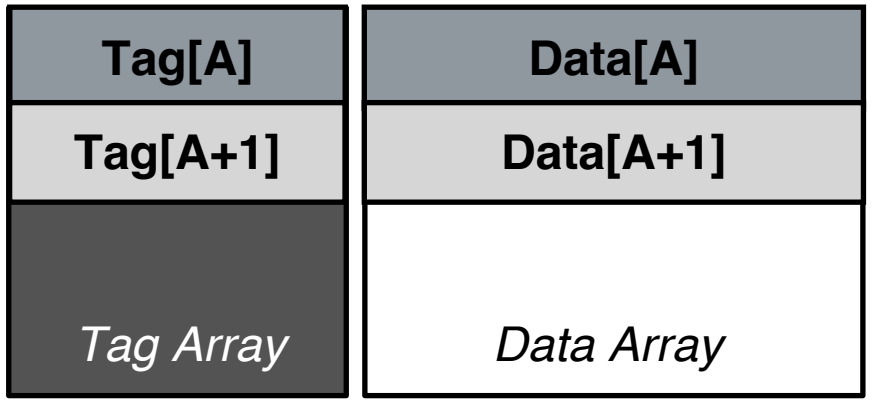
PRACTICAL COMPRESSION

Storing only adjacent blocks together



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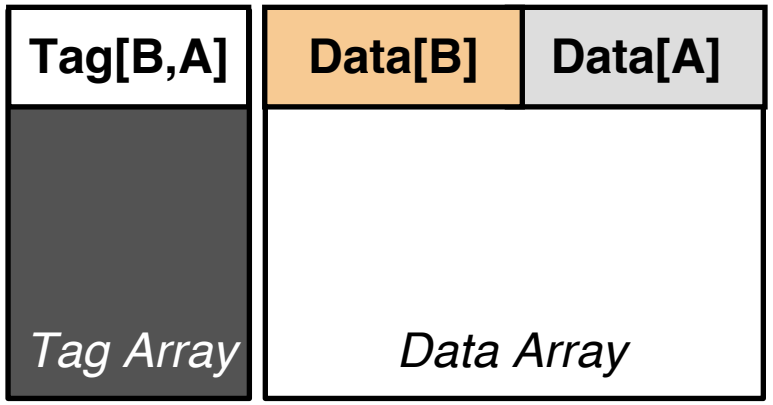

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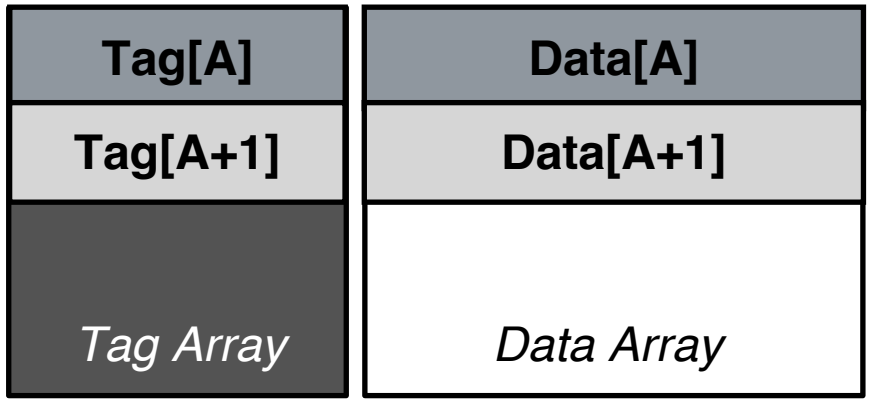

Tag[A] ≈ Tag[A+1]

Cache Compression: Tradeoffs

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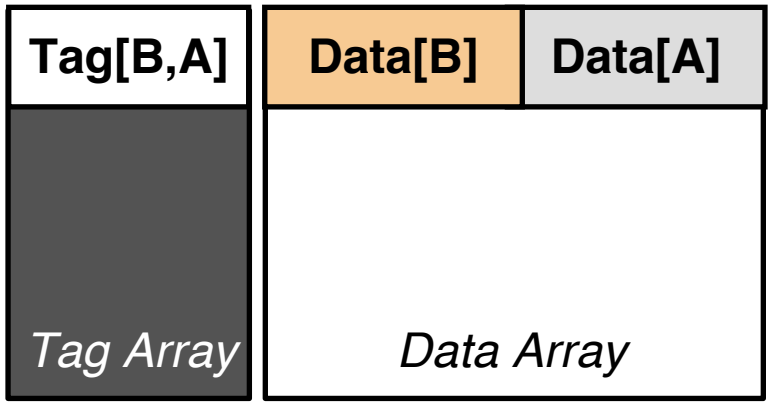

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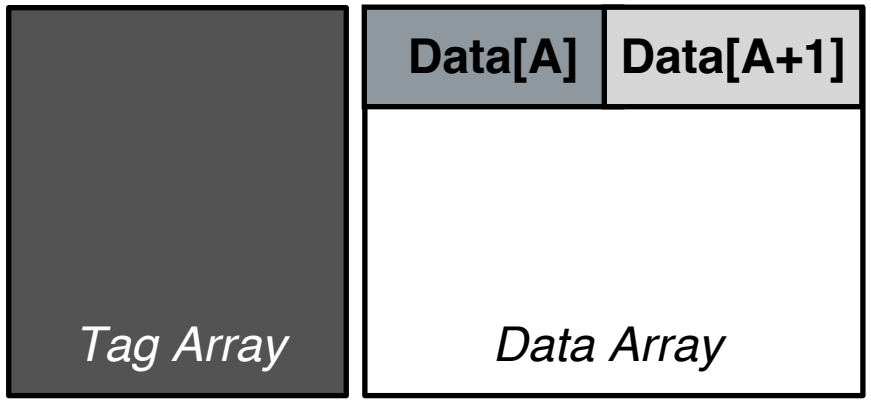

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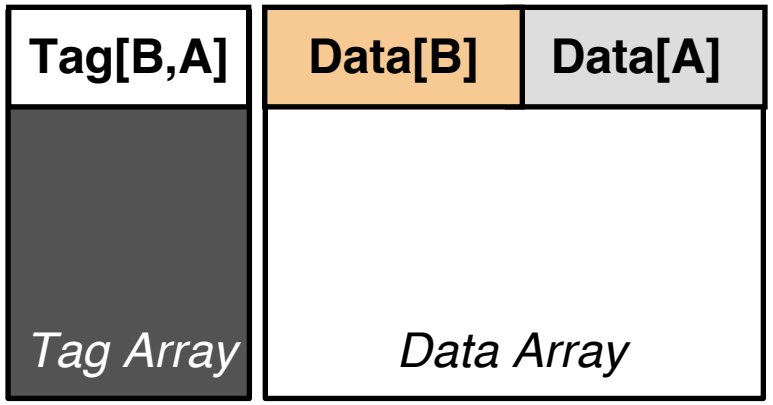

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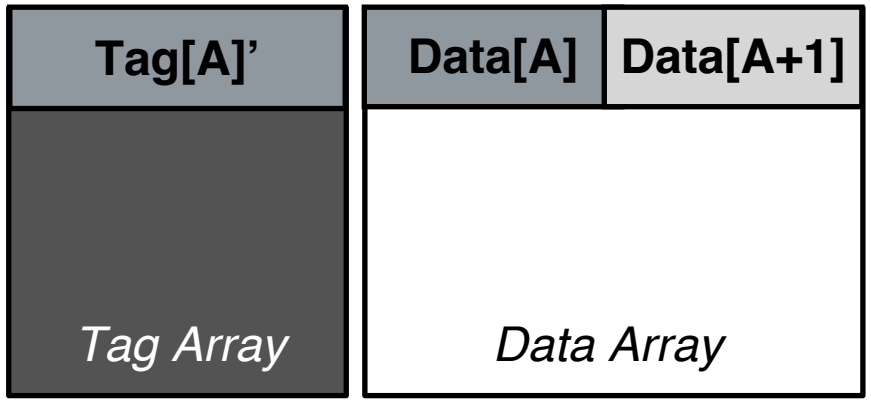

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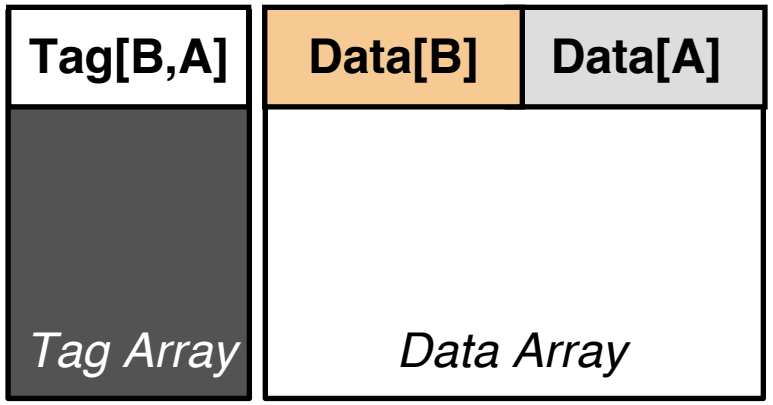

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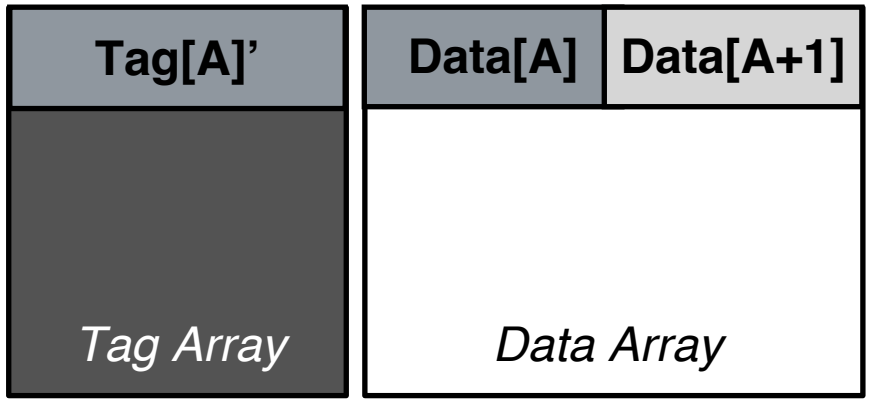
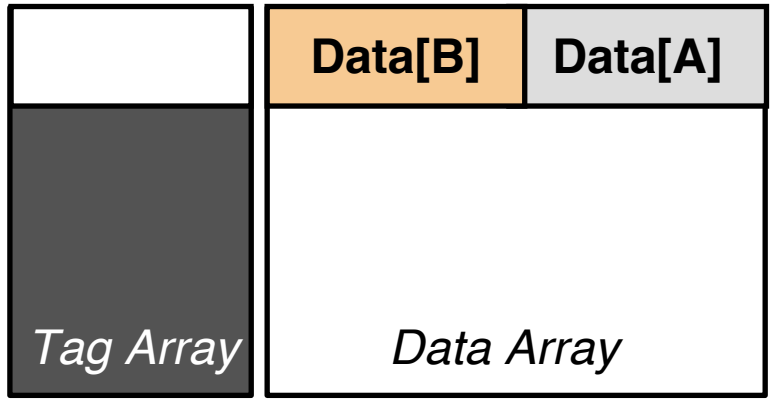


Restriction in Block placement!

Cache Compression: Our Work

Touché :

PRACTICAL TECHNIQUE FOR NEAR-IDEAL COMPRESSION



PRIOR WORK

2x Tag Area

Restriction in Block placement

Cache Compression: Our Work

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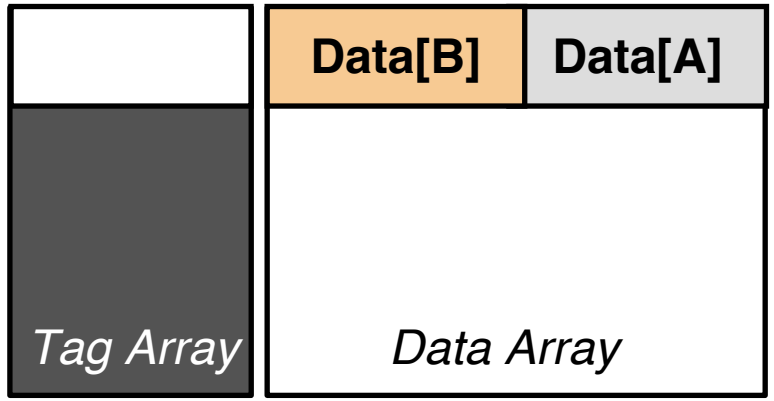

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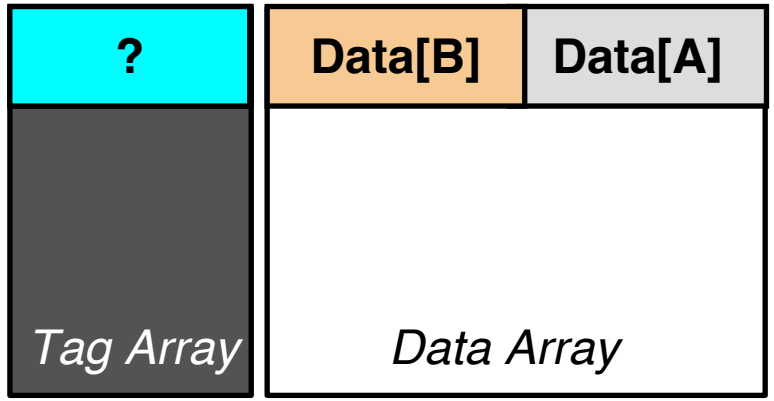

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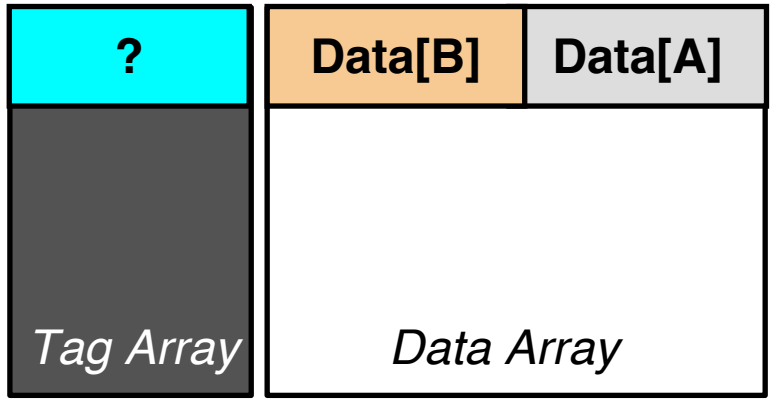

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Three Key Mechanisms

Cache Compression: Our Work

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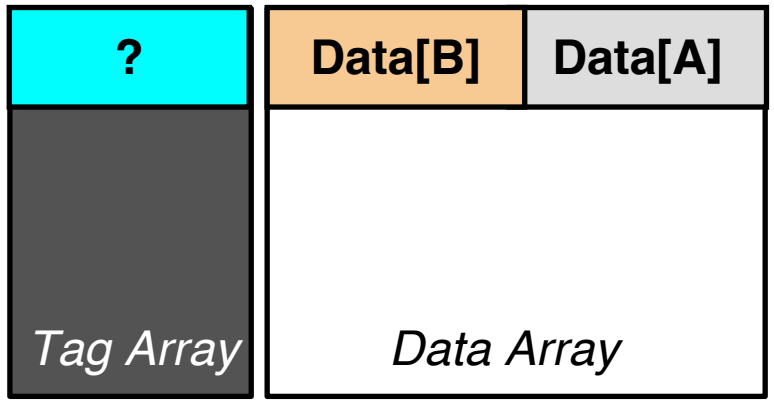


No Additional Area Overheads!

Three Key Mechanisms

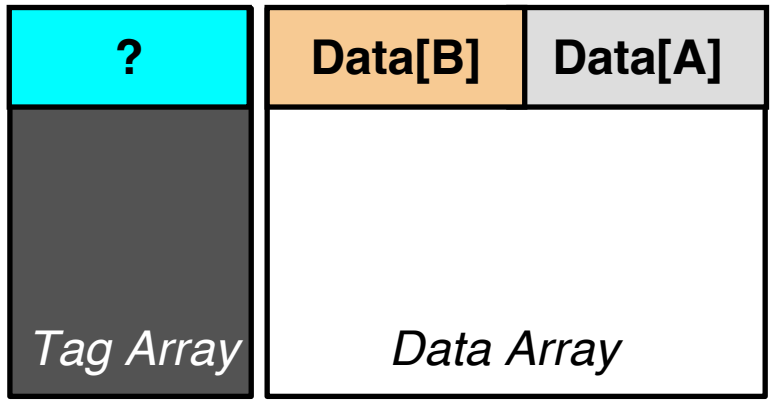
Signature (SIGN) Engine

+

Cache Compression: Our Work

Touché :

PRACTICAL TECHNIQUE FOR NEAR-IDEAL COMPRESSION



No Additional Area Overheads!

Three Key Mechanisms

Signature (SIGN) Engine

+

Tag Appended Data (TADA)

+

Cache Compression: Our Work

Touché :

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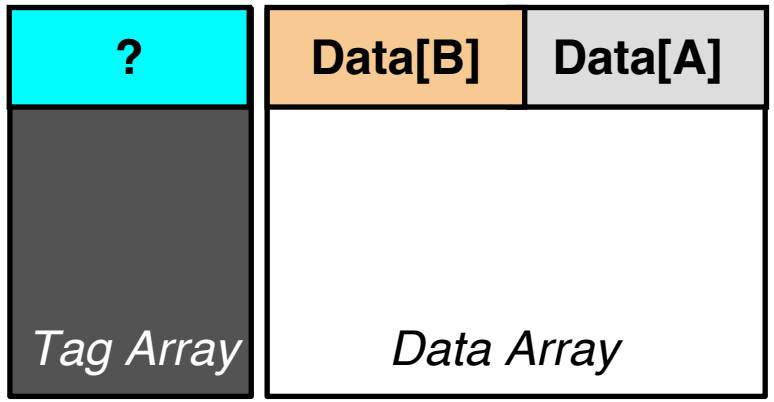

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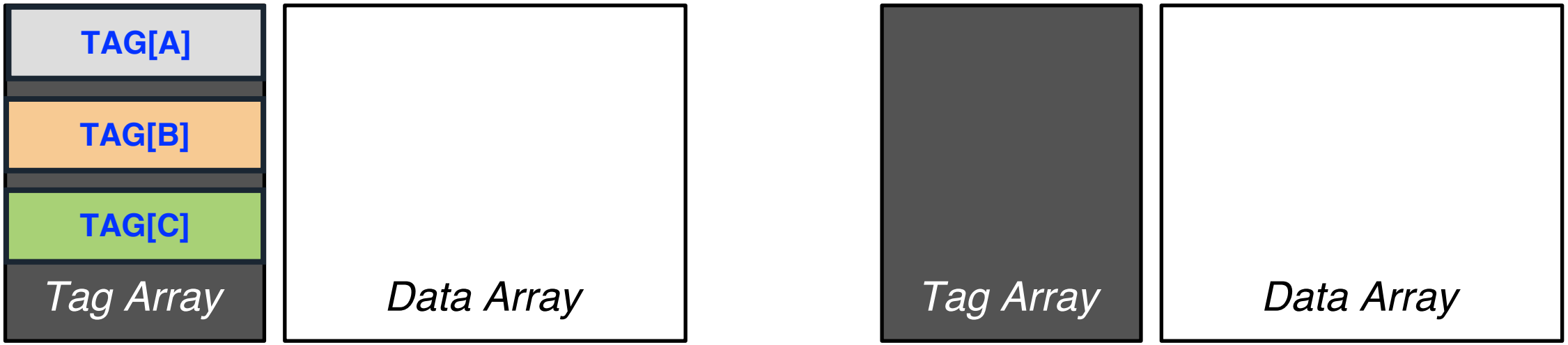
Superblock Marker (SMARK)

Signature (SIGN) Engine

Key Idea



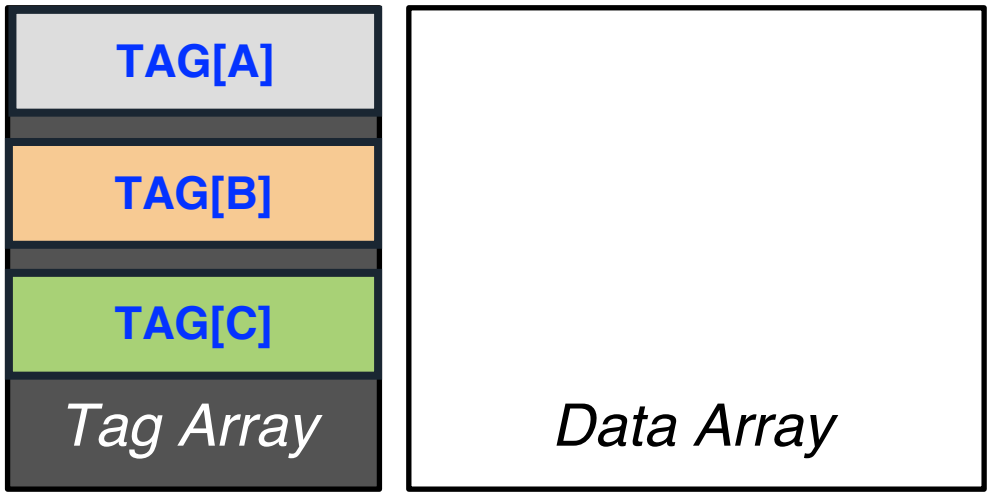
Uncompressed Cache

Touché

Signature (SIGN) Engine

Key Idea

✓ Using **shortened signatures**



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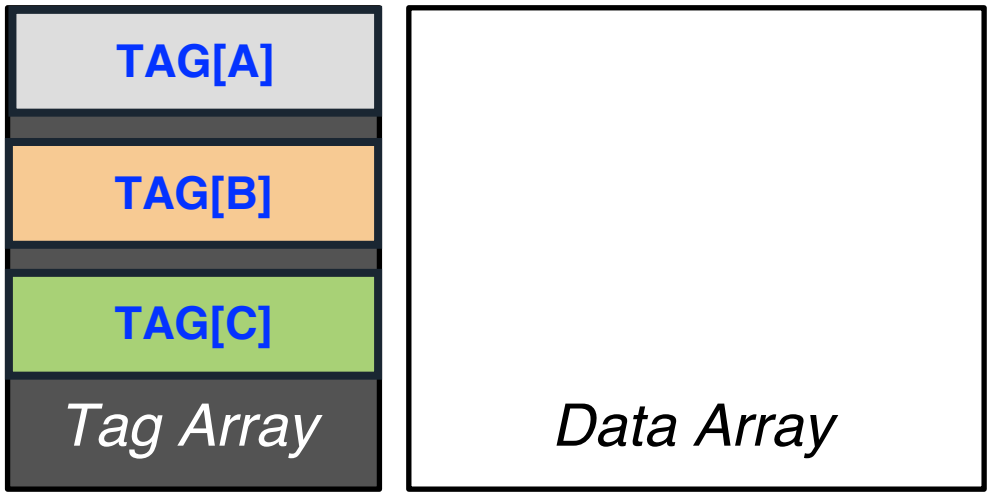

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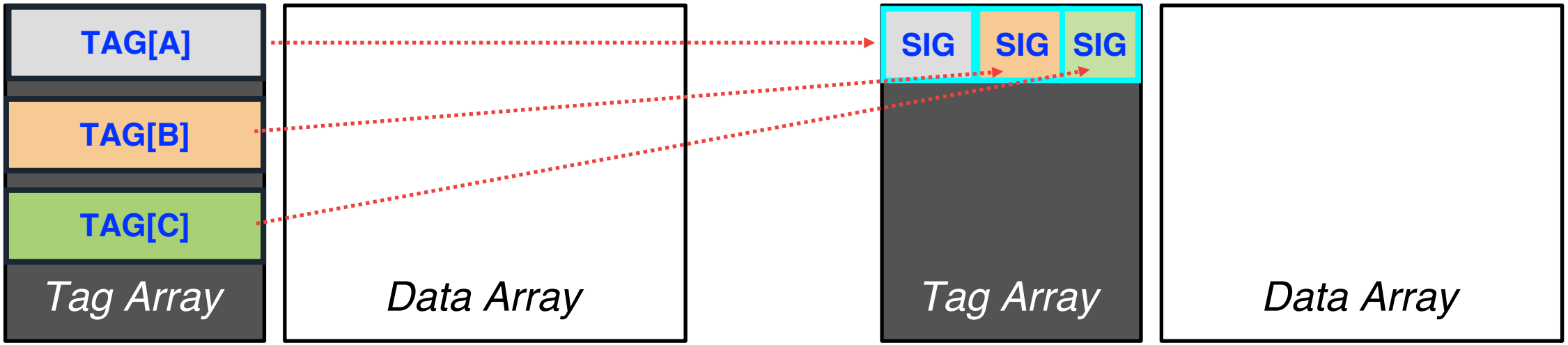

Uncompressed Cache

Touché

Signature (SIGN) Engine

How to generate Signature?

TAG[A]

Touché

Signature (SIGN) Engine

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✓ Generates shortened signatures (9 bits) from the full tag addresses (29 bits)

Touché

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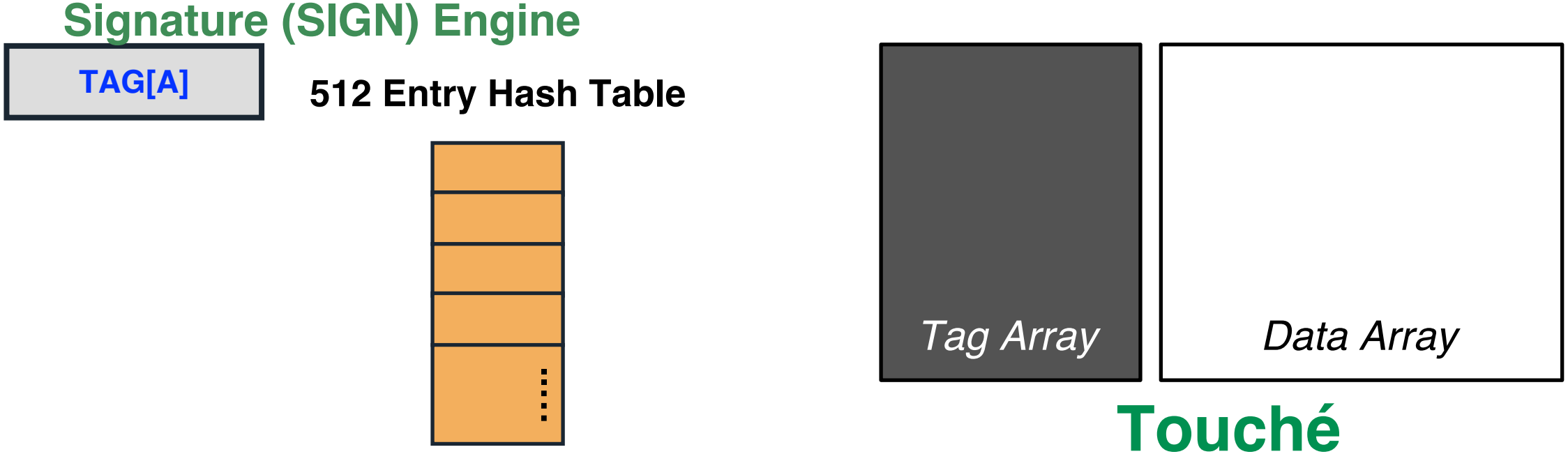

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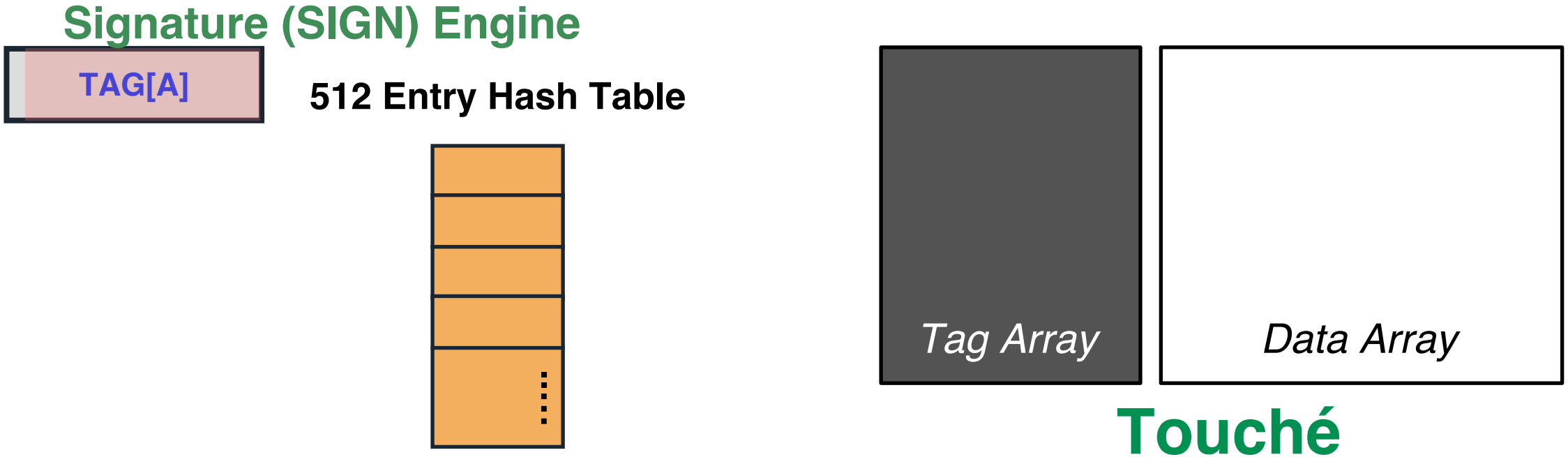

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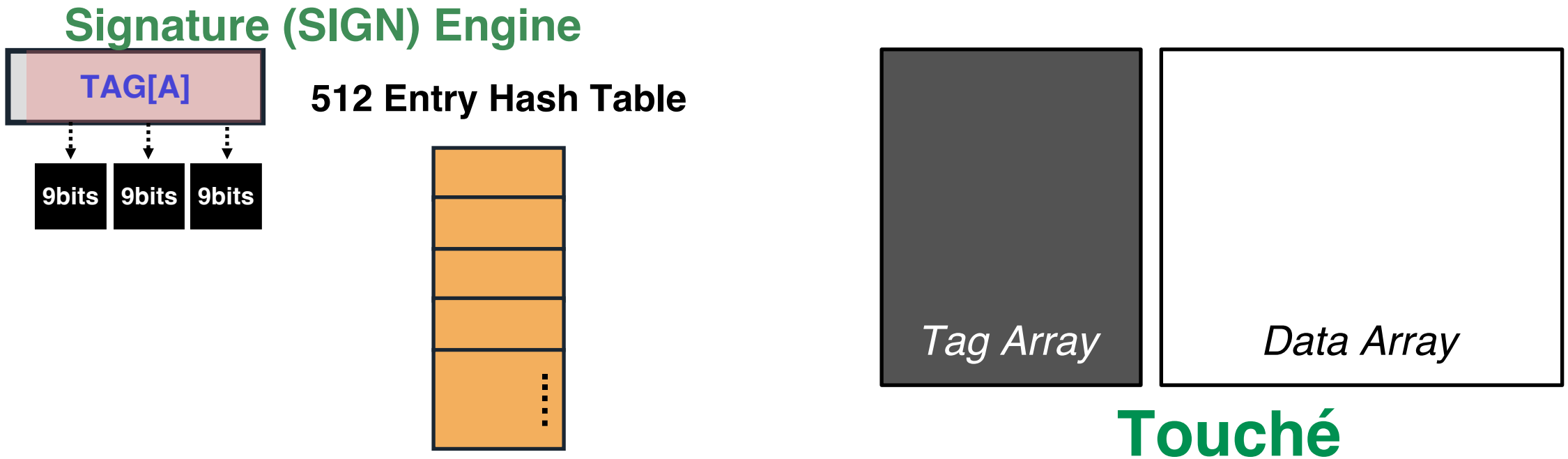

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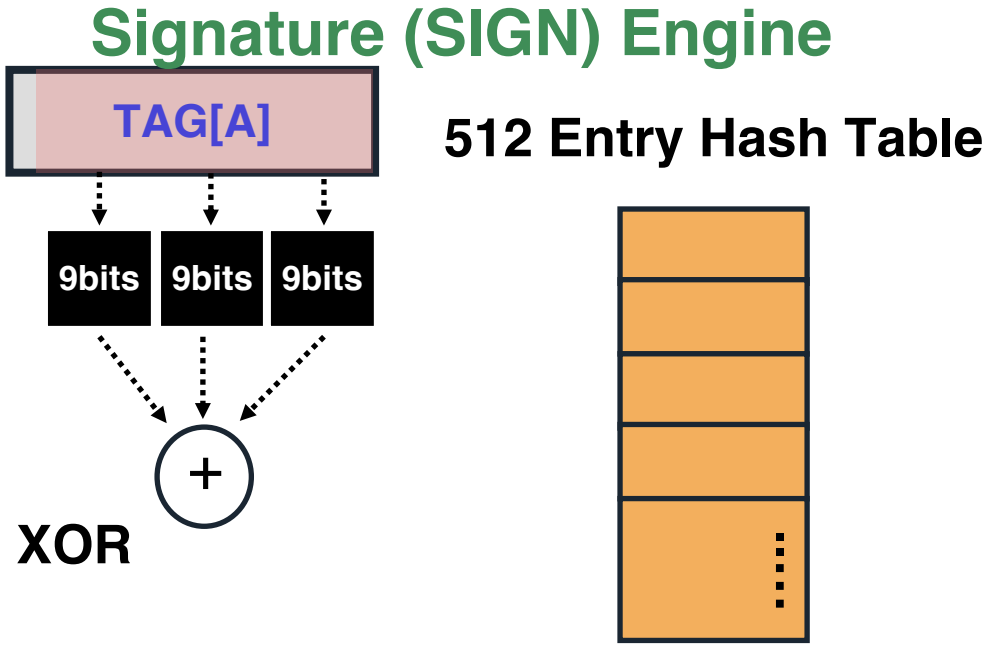

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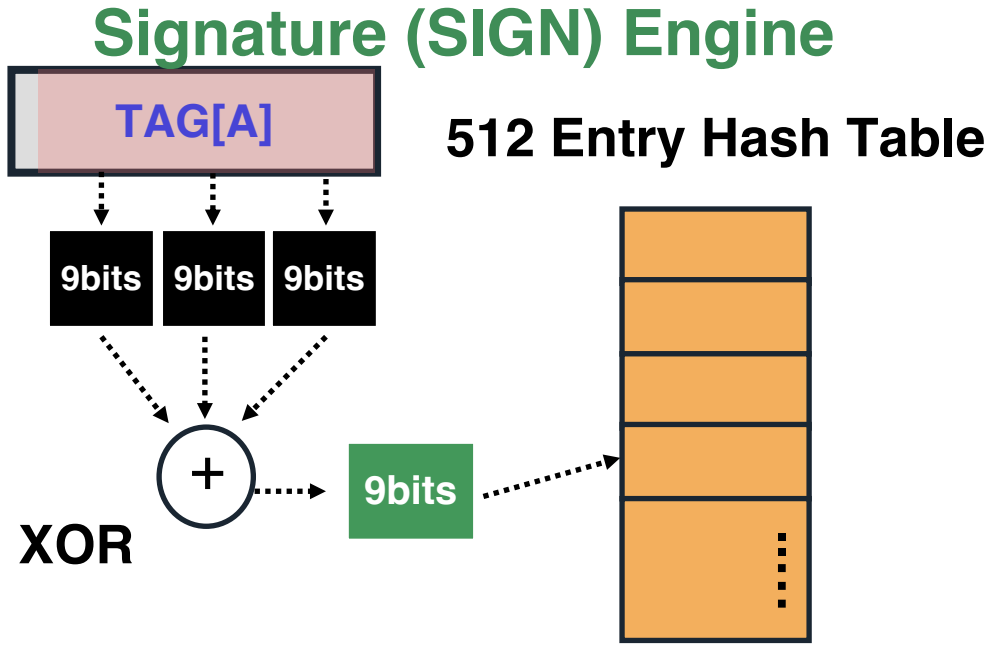

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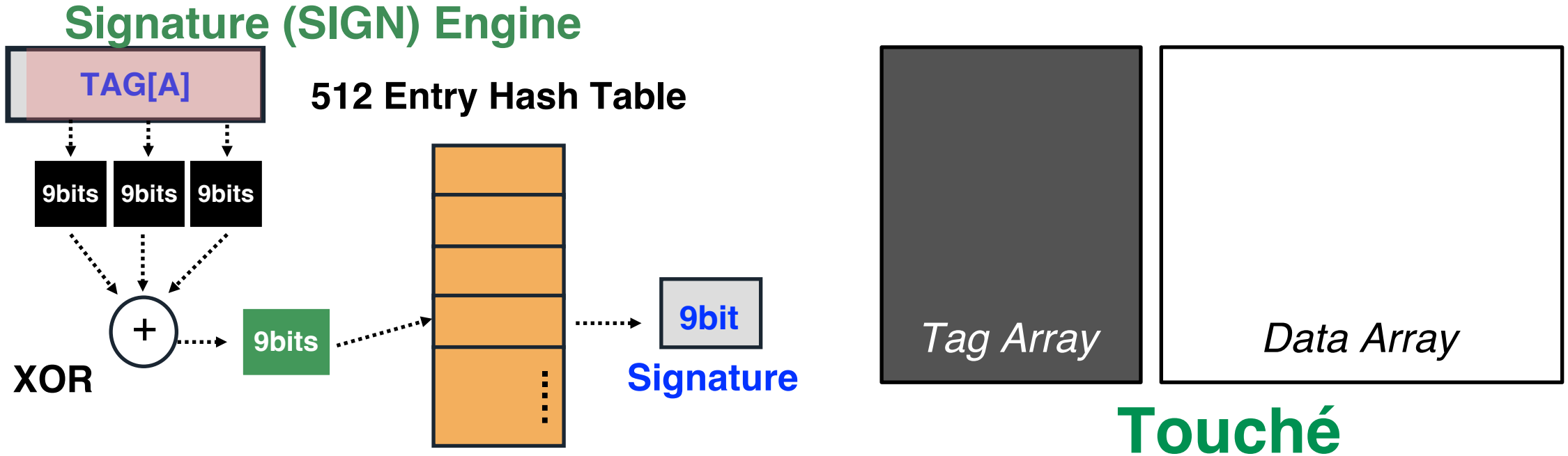

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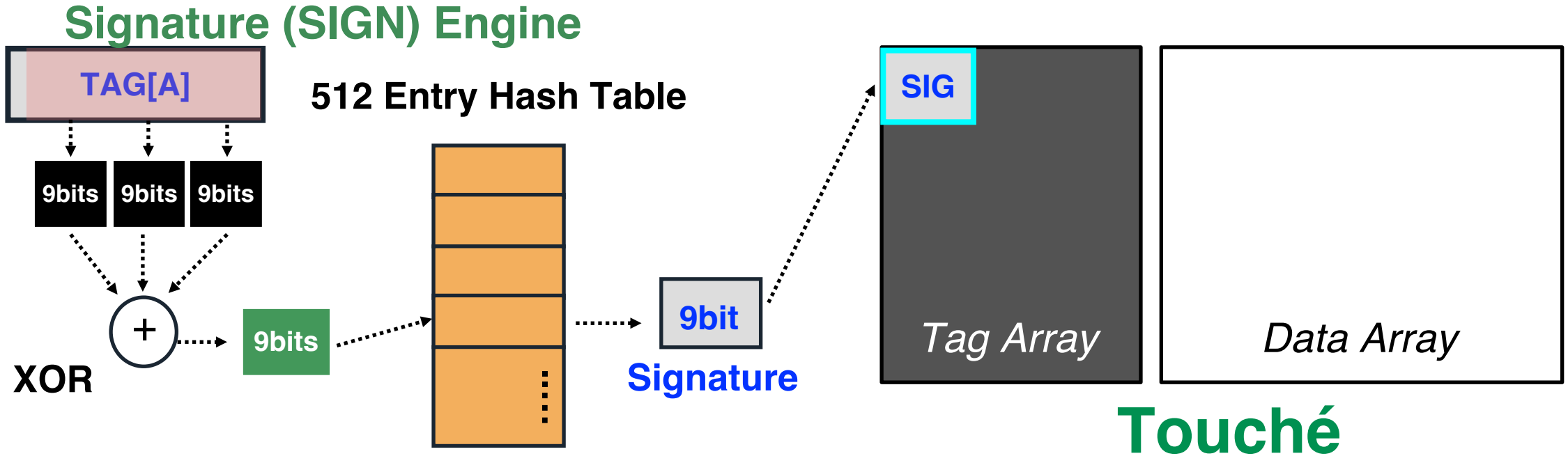


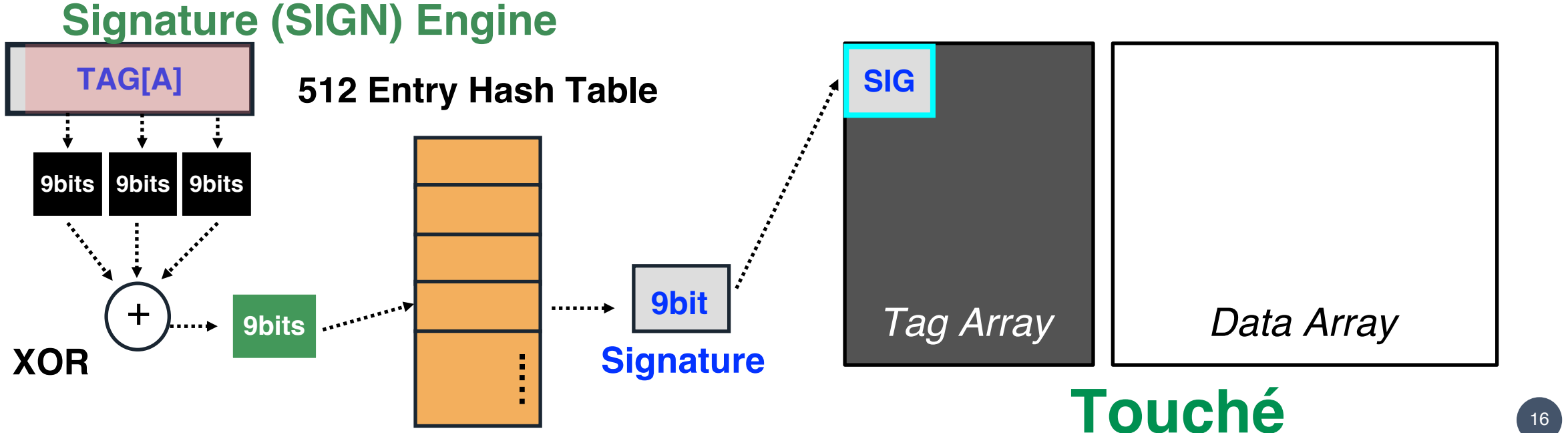
Touché

Signature (SIGN) Engine

How to generate Signature?

✓ Generates shortened signatures (9 bits) from the full tag addresses (29 bits)

✓ Only requires one XOR operation and a hash table lookup



Touché

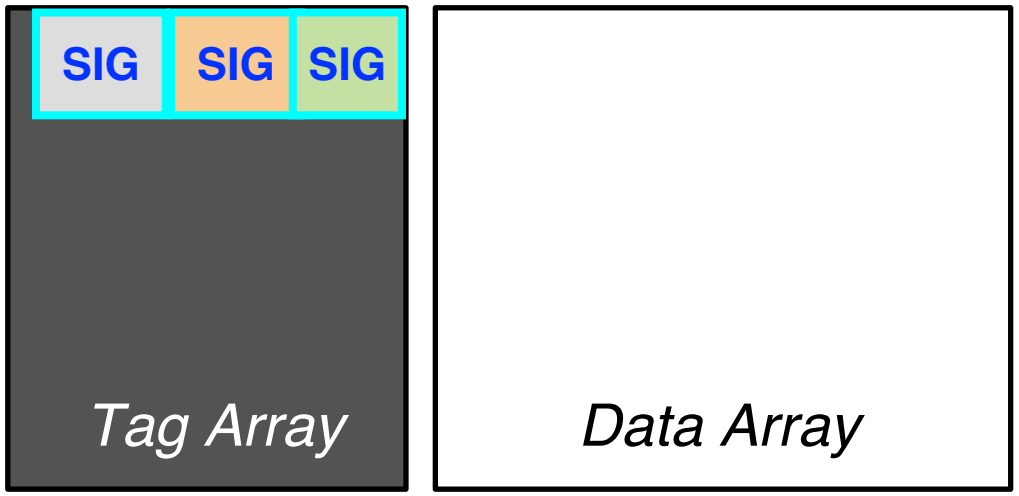
Signature (SIGN) Engine

Key Idea

✓ Using Shortened Signatures

✓ Store the shortened signatures in a tag entry

✓ **Identifying compressed lines** by **using the valid and dirty bits**



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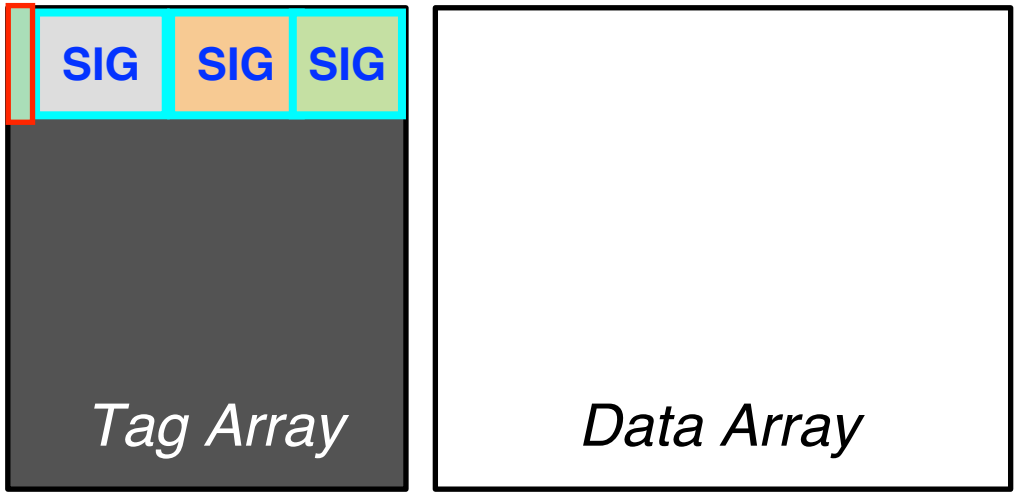

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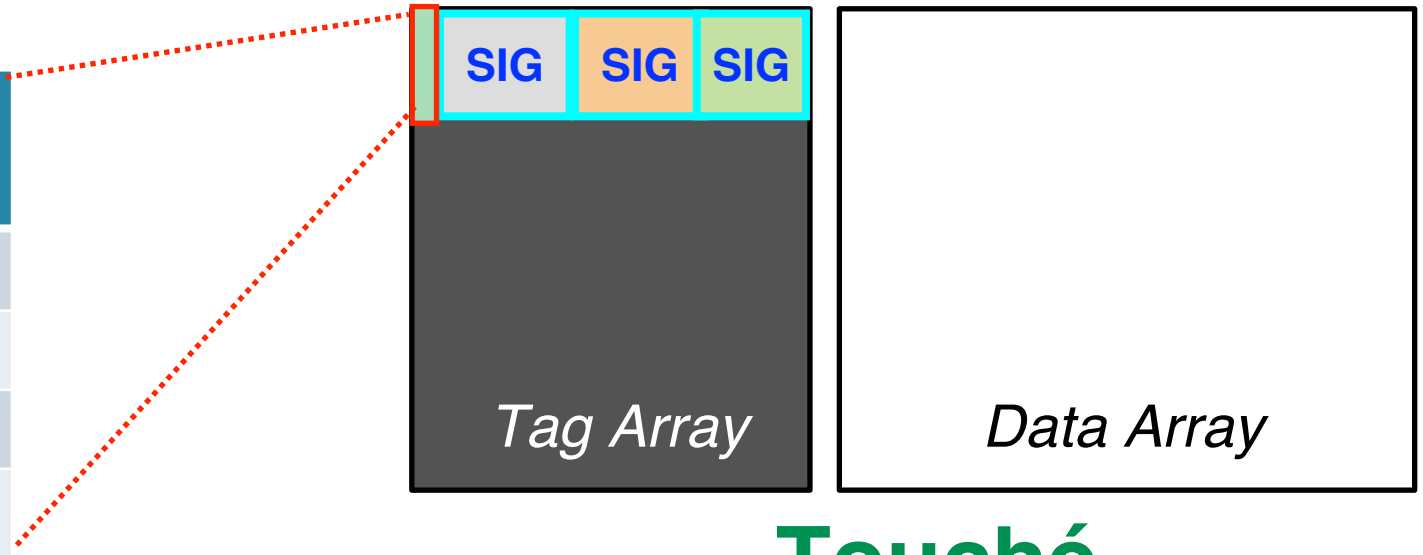

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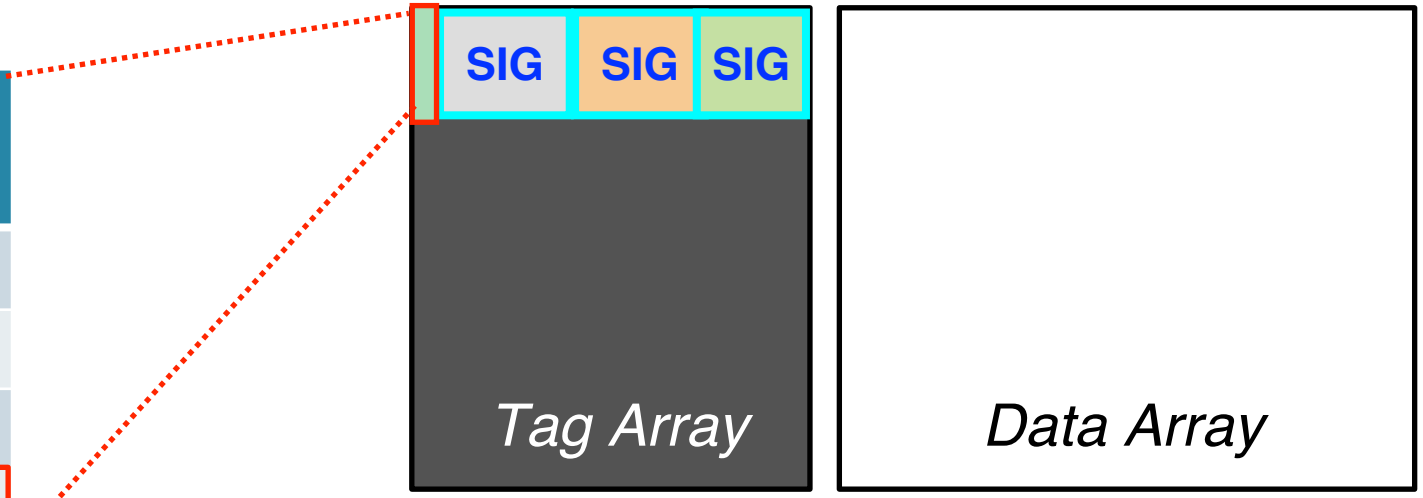

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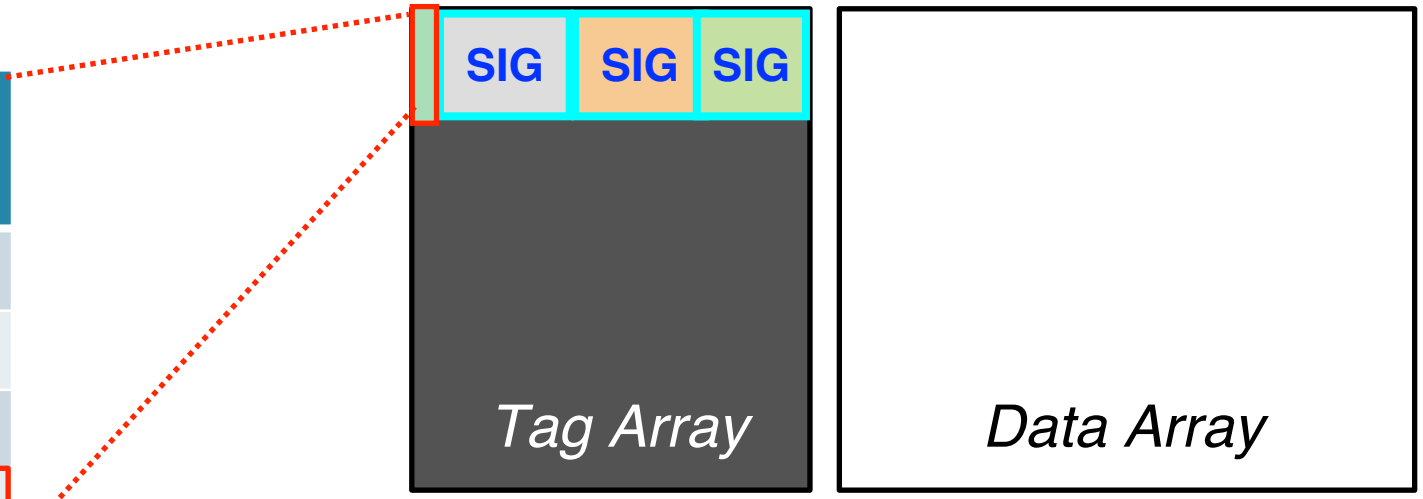

Touché

Signature (SIGN) Engine

An Issue

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✓ Signatures are shorter than full tags

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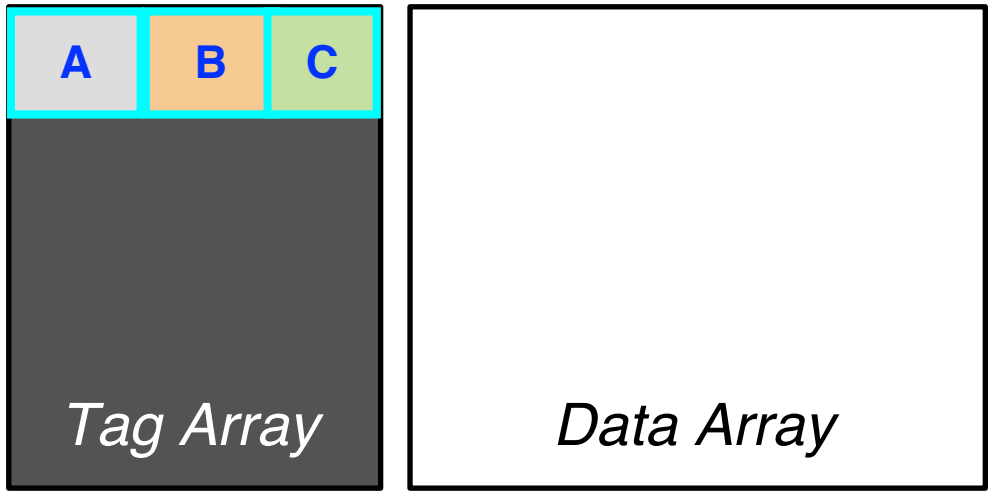

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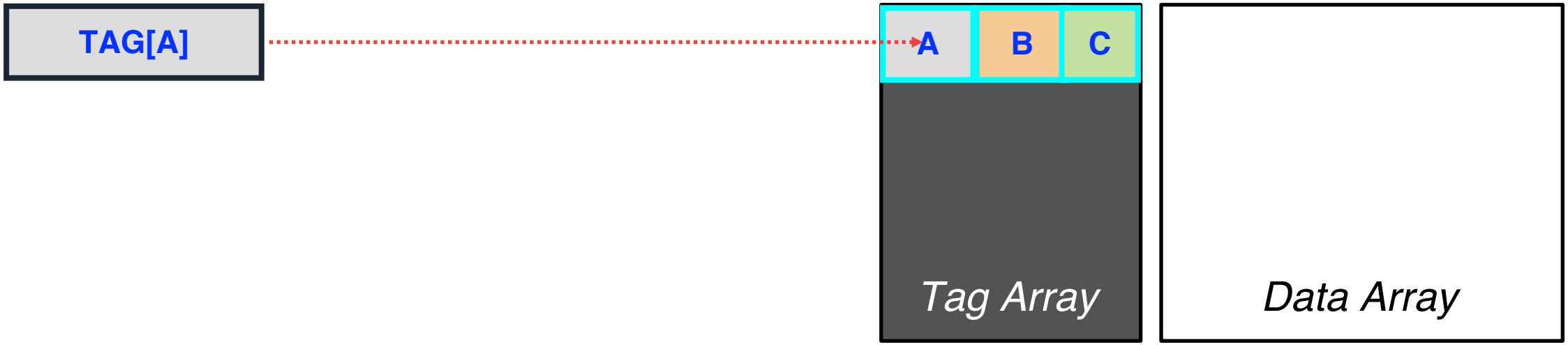

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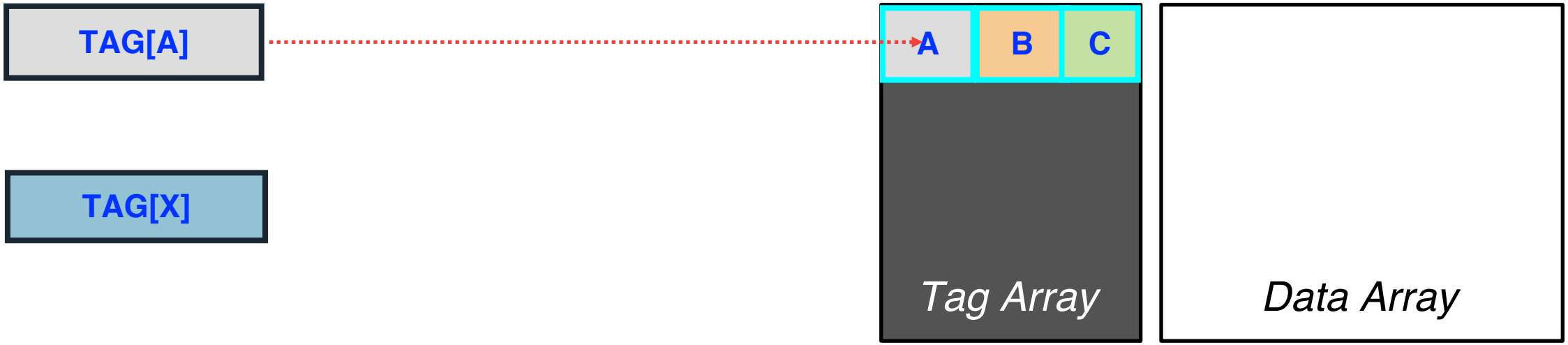

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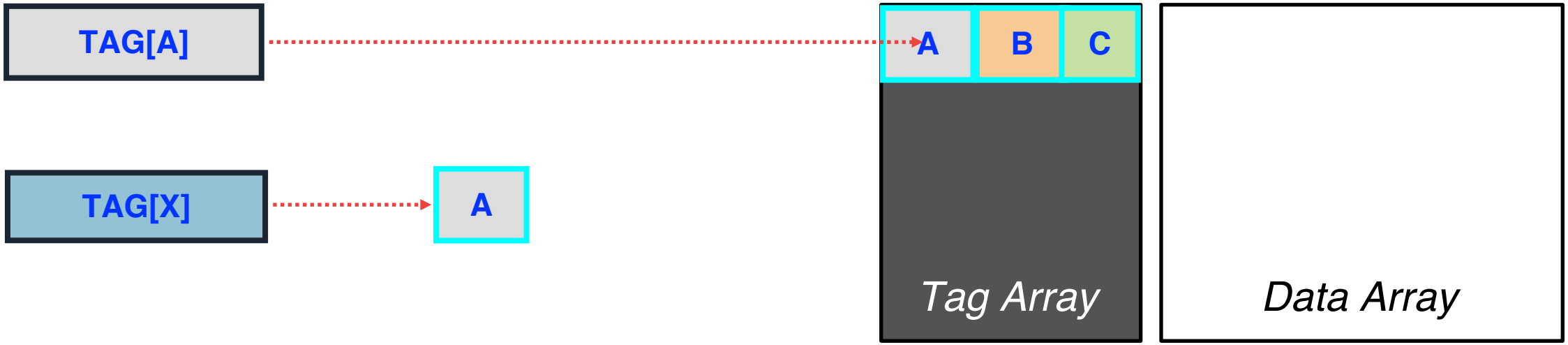

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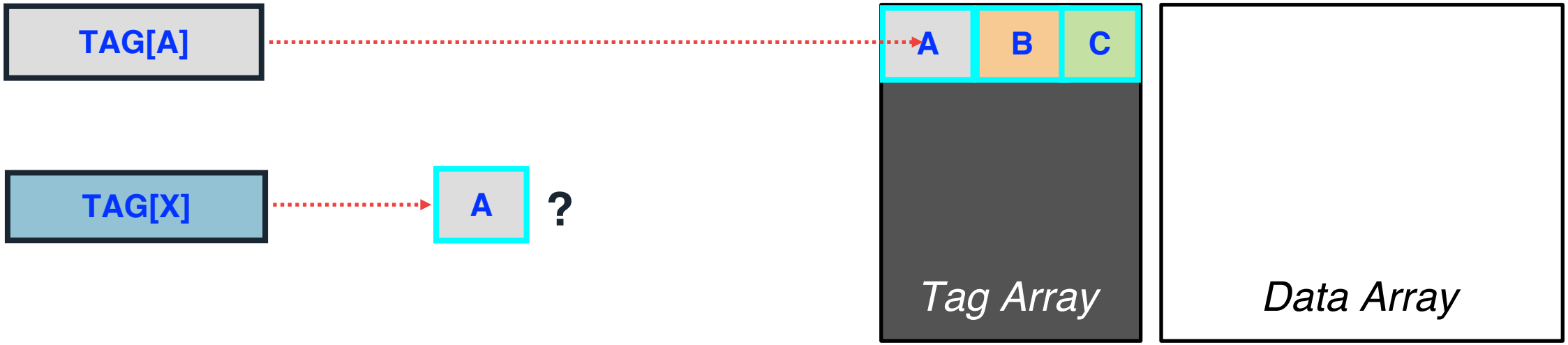

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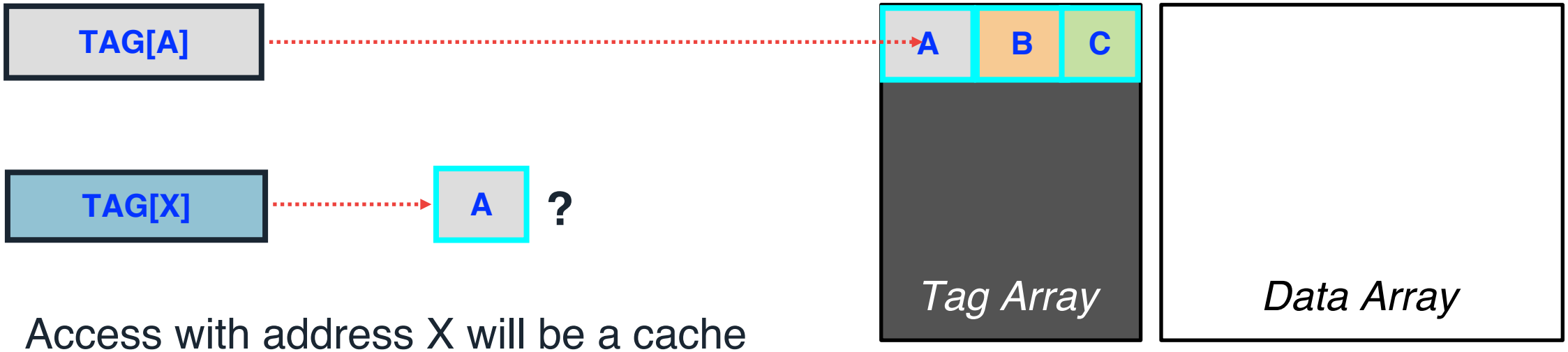


Access with address X will be a cache

hit, but it should be a cache miss!!

Touché

Signature (SIGN) Engine

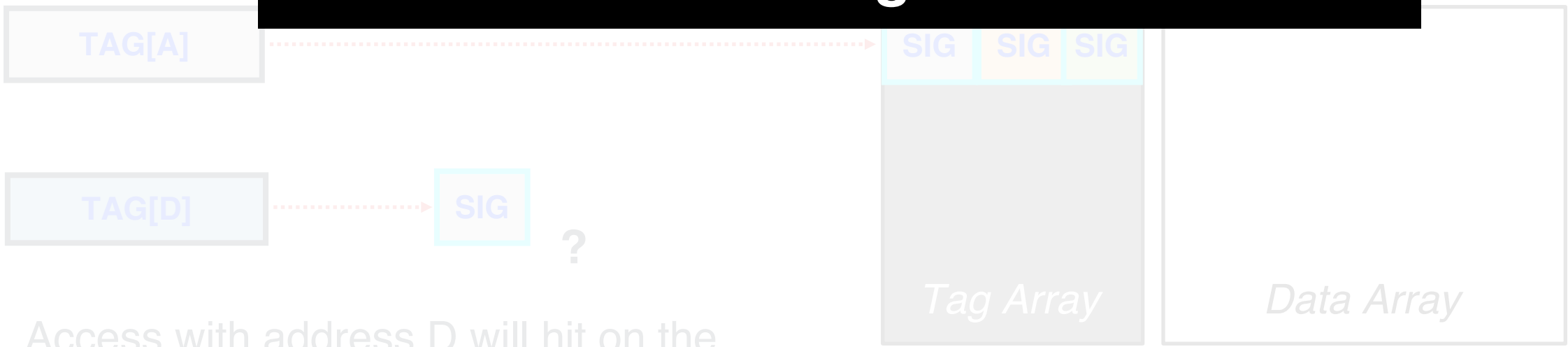
An Issue with SIGN

✓ Signatures are shorter than full tags

Sever

How to resolve the Signature Collision?

Collision



Access with address D will hit on the

cache, but it should be miss!!

Touché

Signature (SIGN) Engine

How to resolve the Signature Collision?

→ Tag Appended Data (TADA)

Tag Appended Data (TADA)

Key Idea

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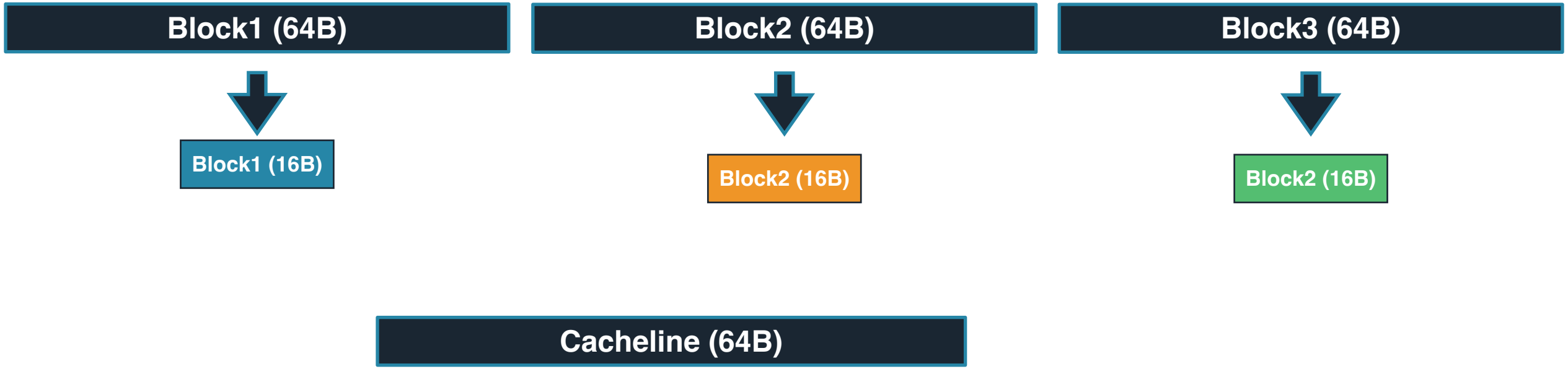

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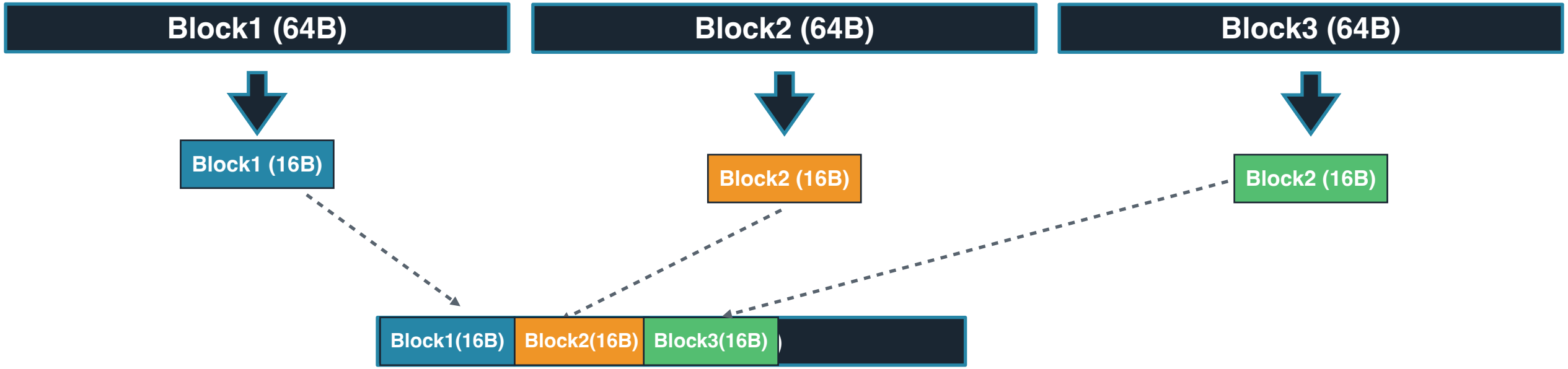

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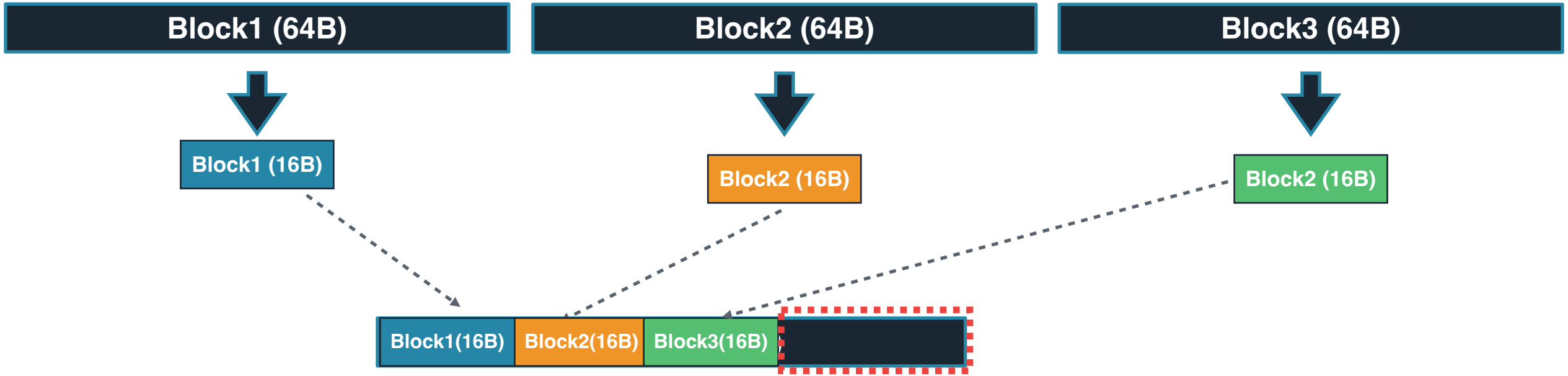

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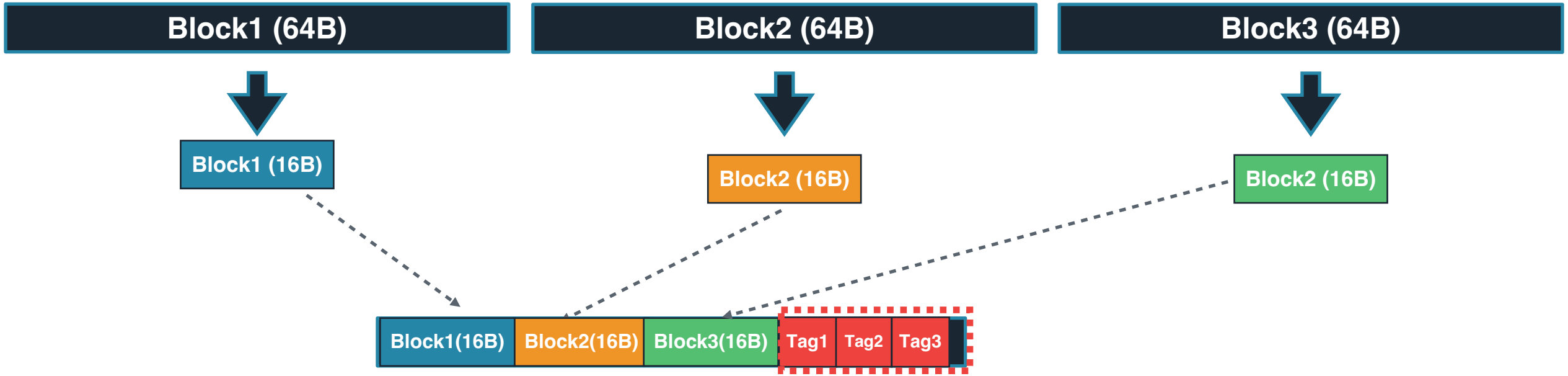

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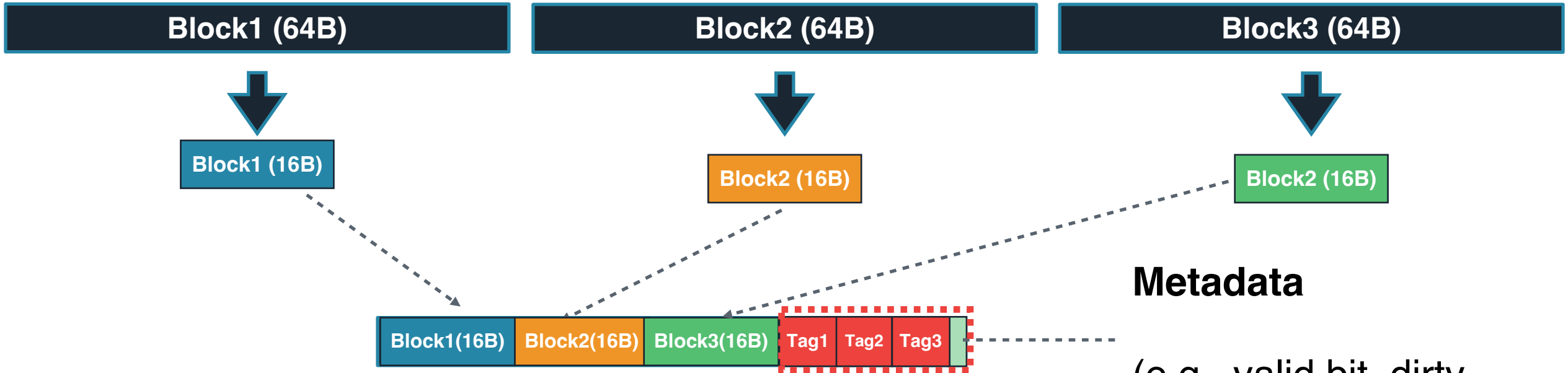

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(e.g., valid bit, dirty bit, compressibility)

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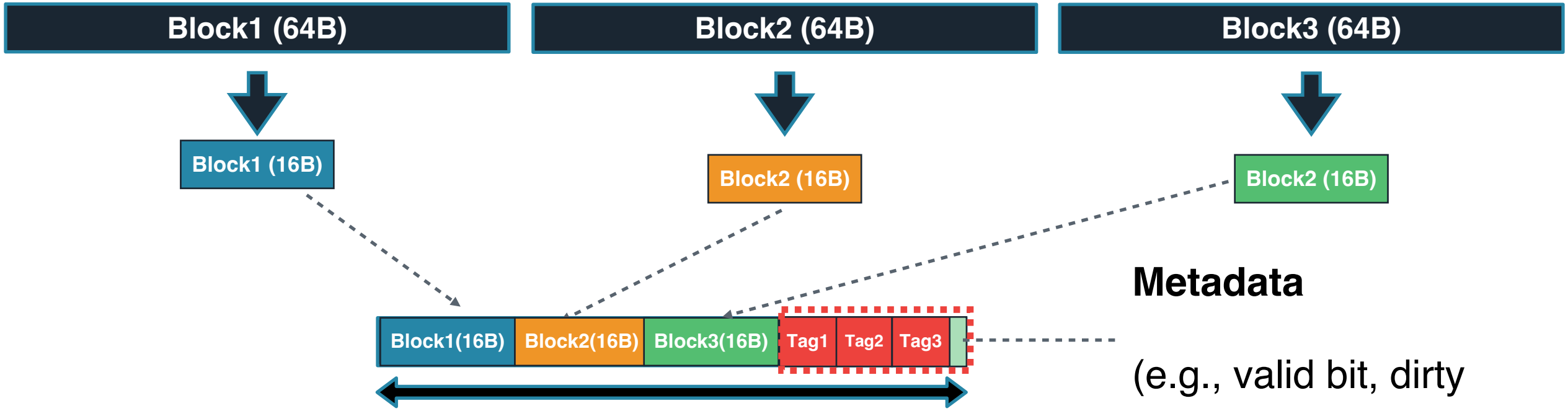

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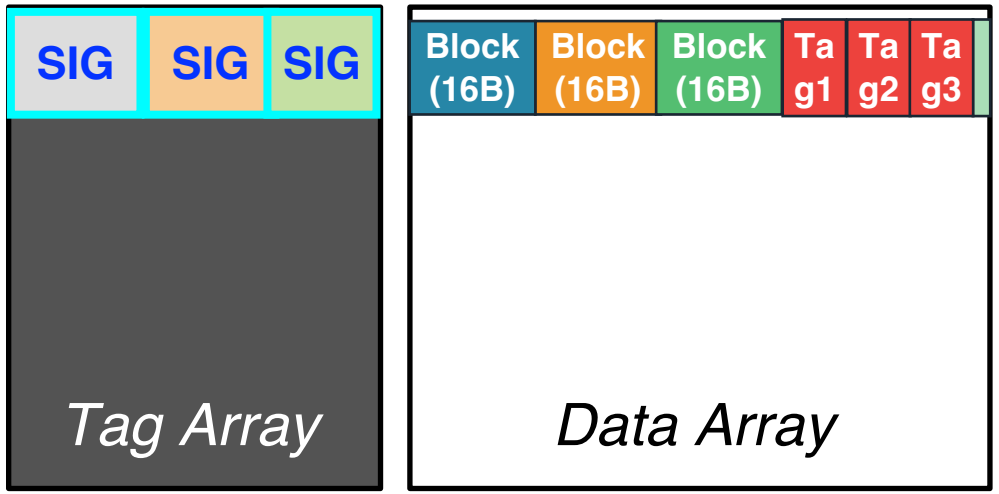
SIGN + TADA

“SIGN+TADA” enable to store **three compressed blocks** in a



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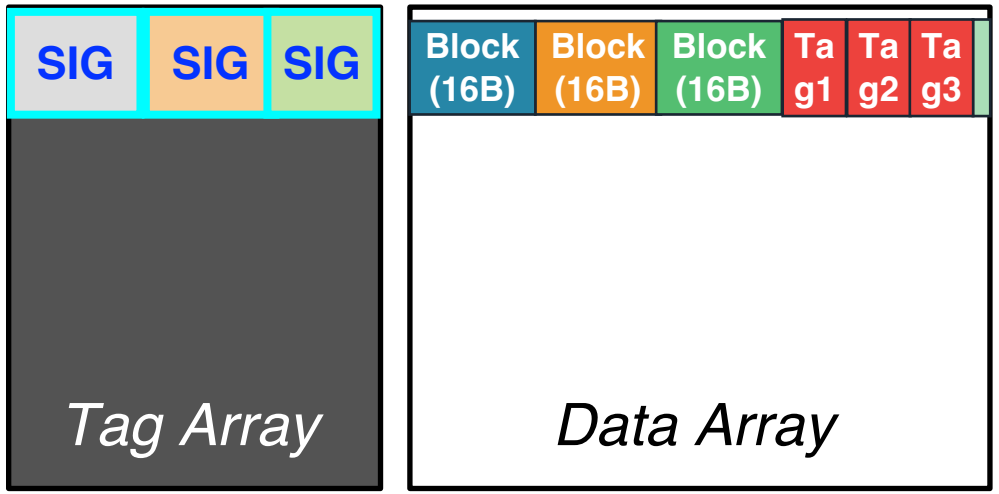

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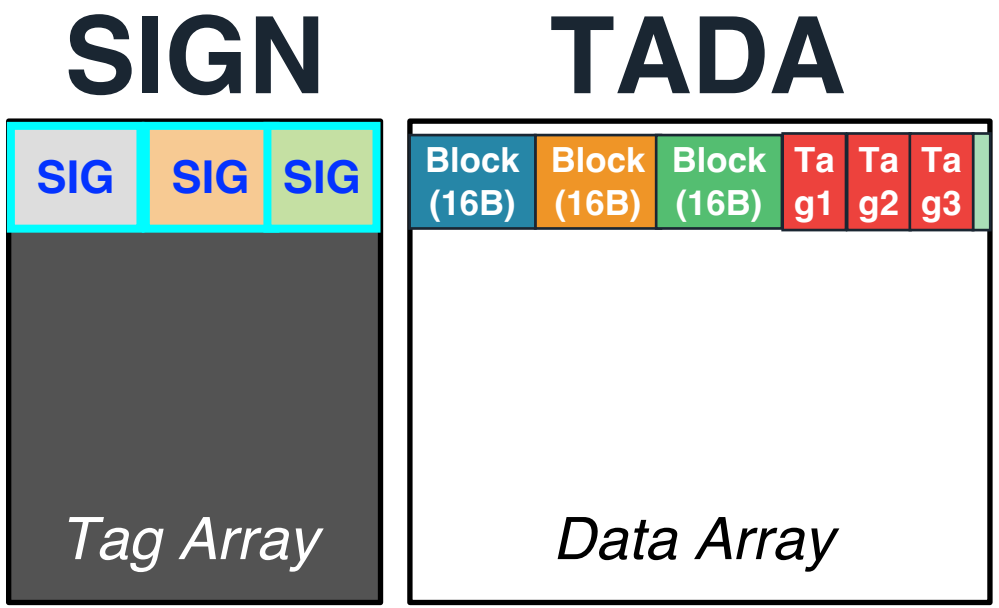

Touché

Superblock Marker (SMARK)

To improve the effective cache capacity **further**,

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Uncompressed Cache

Superblock Marker (SMARK)

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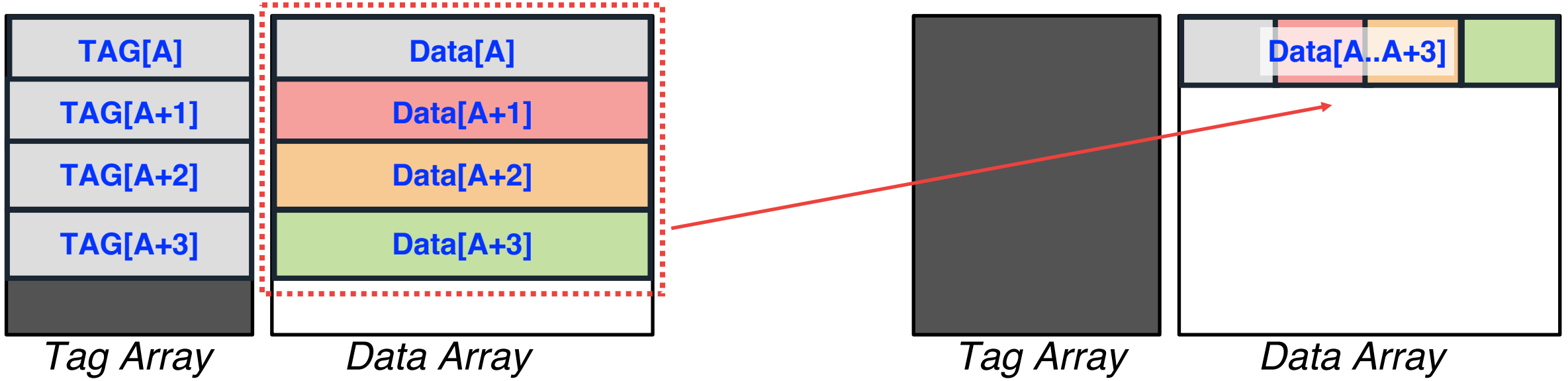

Uncompressed Cache

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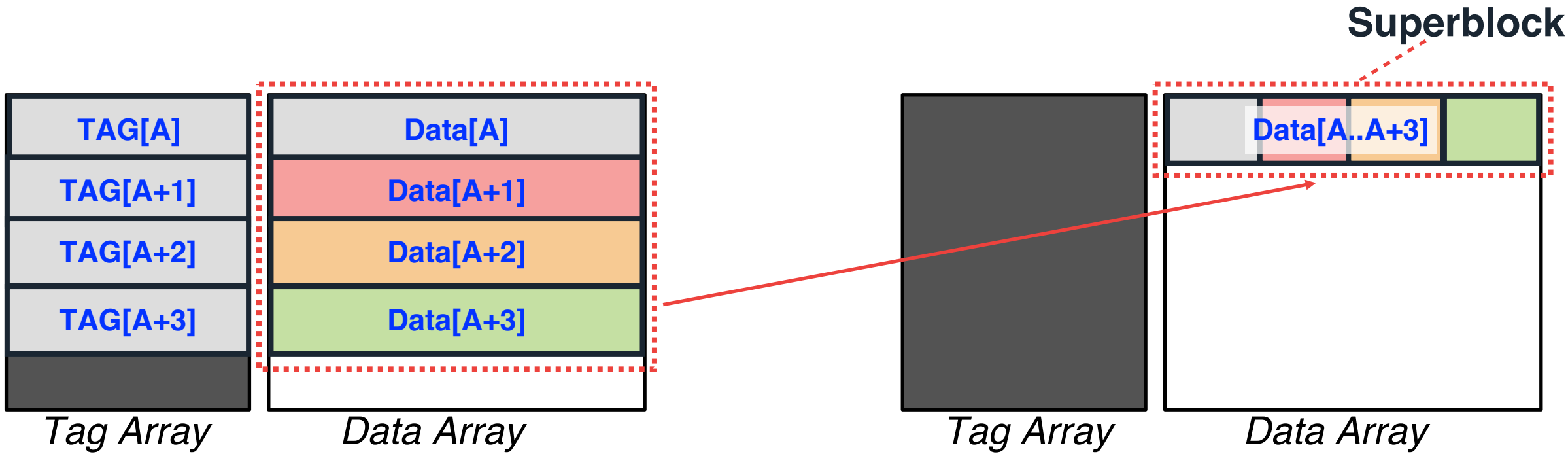


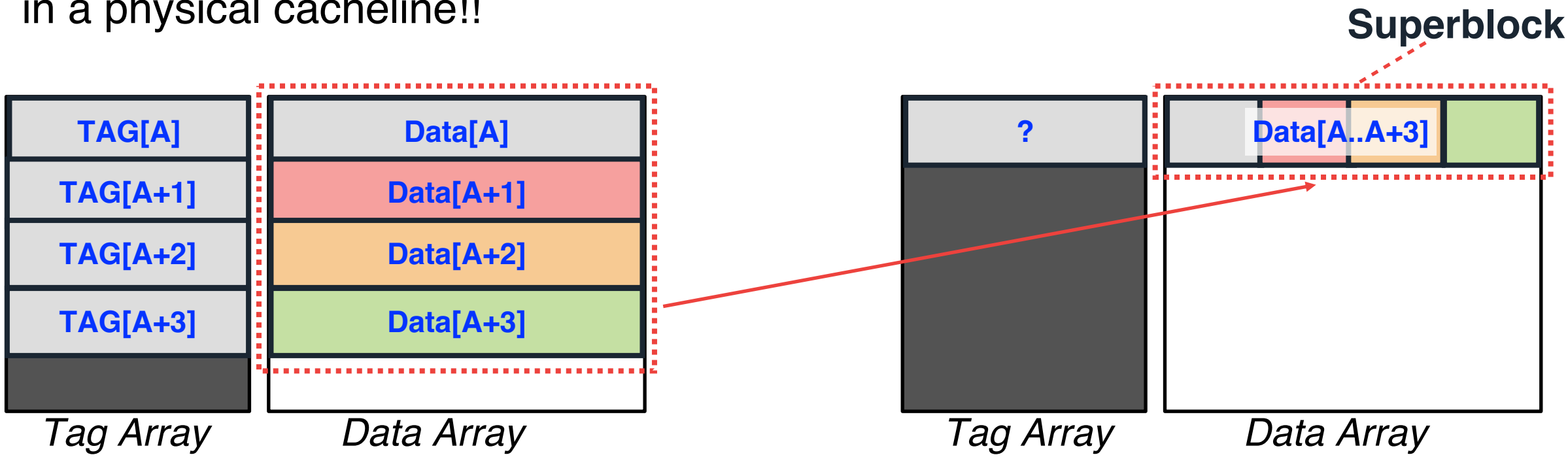
Uncompressed Cache

Touché

Superblock Marker (SMARK)

To improve the effective cache capacity **further**,

SMARK enables to store **four neighboring compressed blocks** (Superblock) in a physical cacheline!!



Uncompressed Cache

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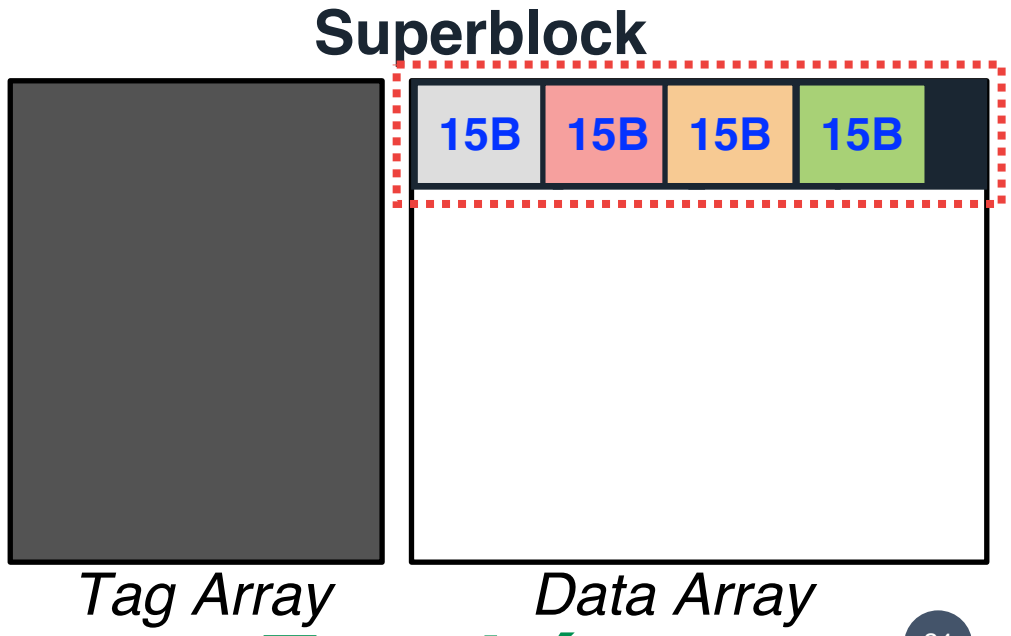

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Superblock Marker (SMARK)

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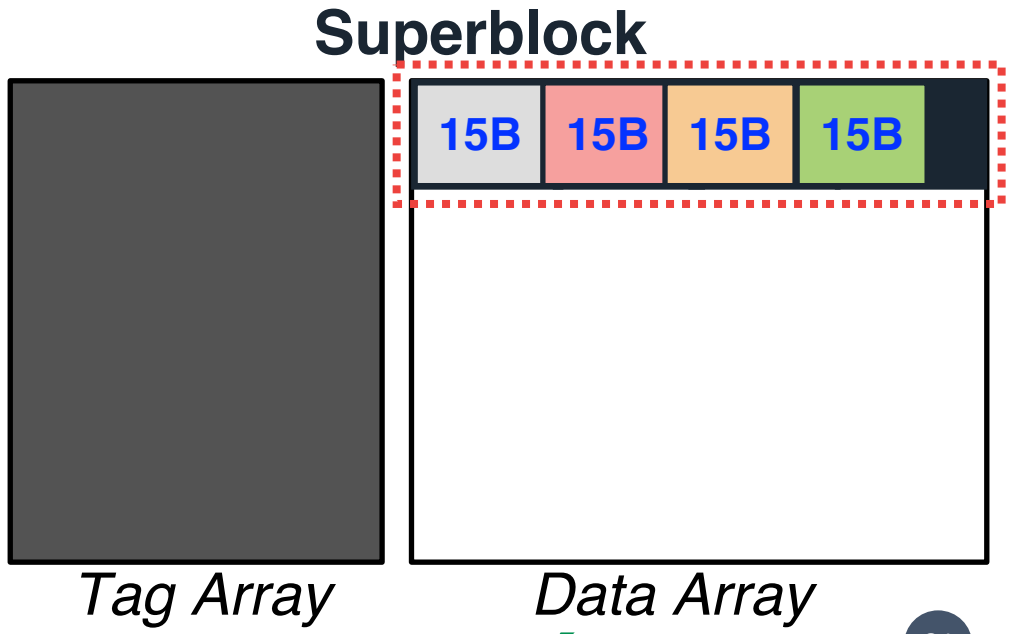
✓ To indicate the superblock, stores a random 16-bit marker (SMARK) in a tag entry



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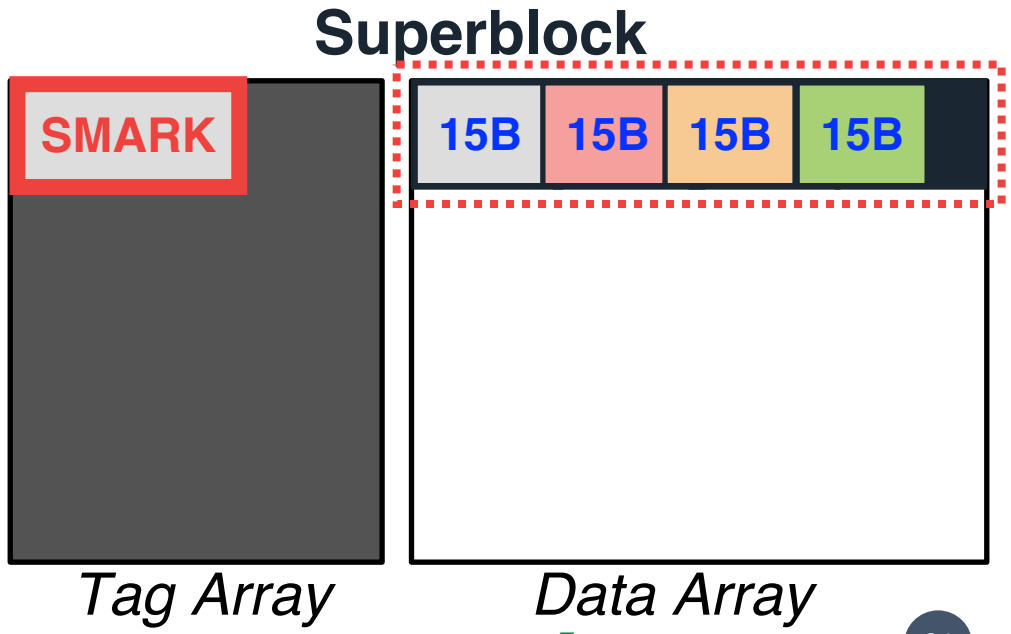

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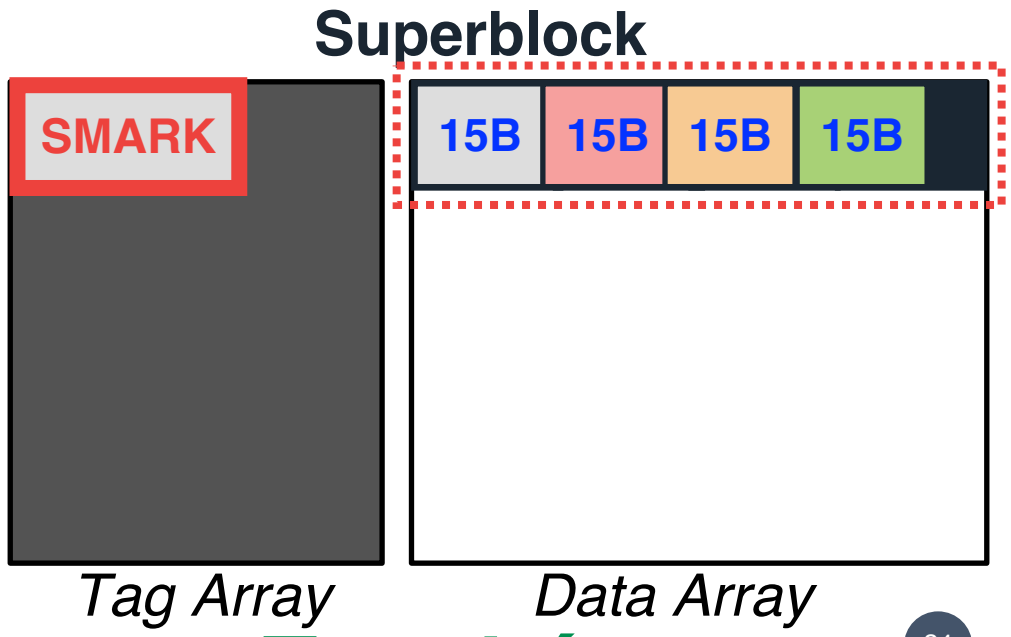
✓ To indicate the superblock, stores a random 16-bit marker (SMARK) in a tag entry

✓ Appends the signature to the marker



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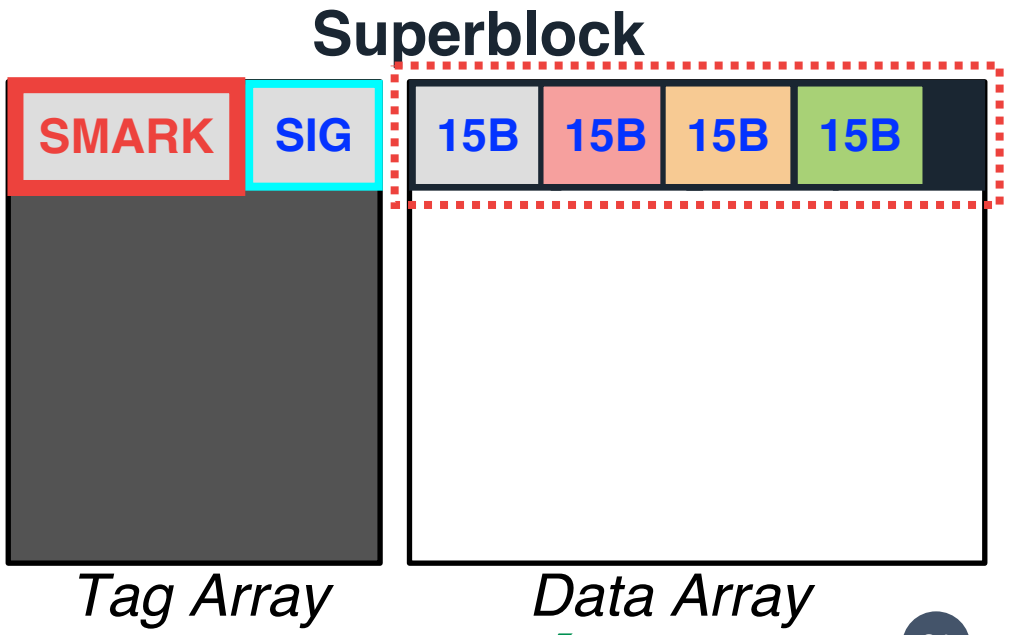

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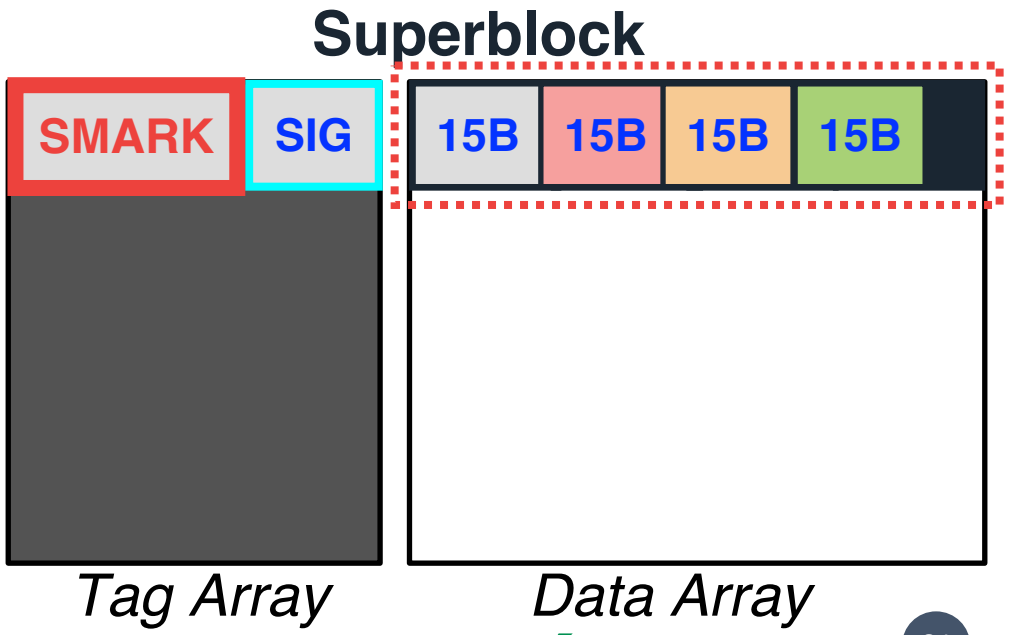
✓ The full tag is stored at the end of the cacheline



Touché

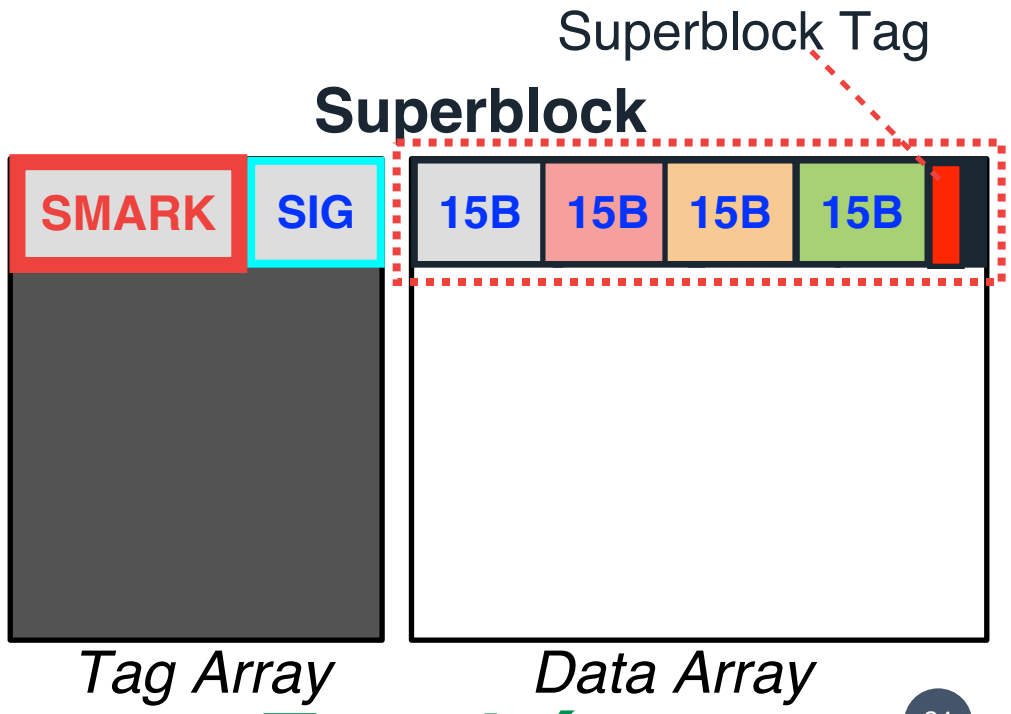
Superblock Marker (SMARK)

Key Idea

✓ To indicate the superblock, stores a random 16-bit marker (SMARK) in a tag entry

✓ Appends the signature to the marker

✓ The full tag is stored at the end of the cacheline



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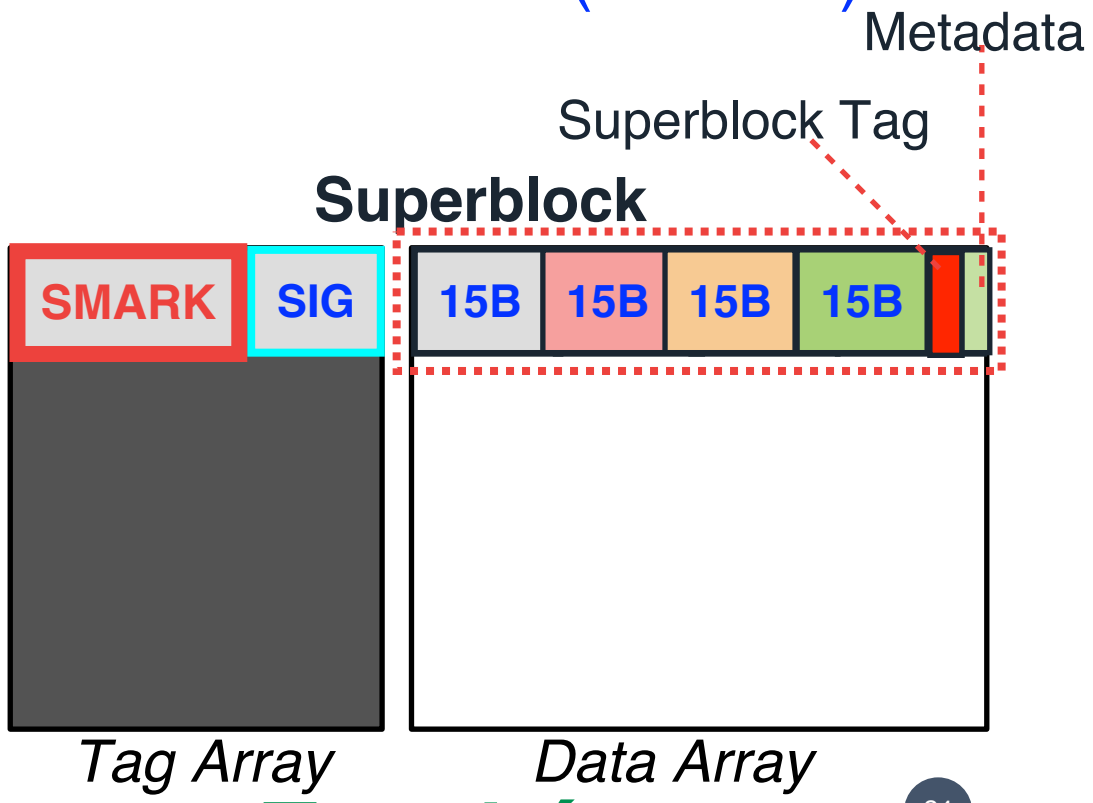
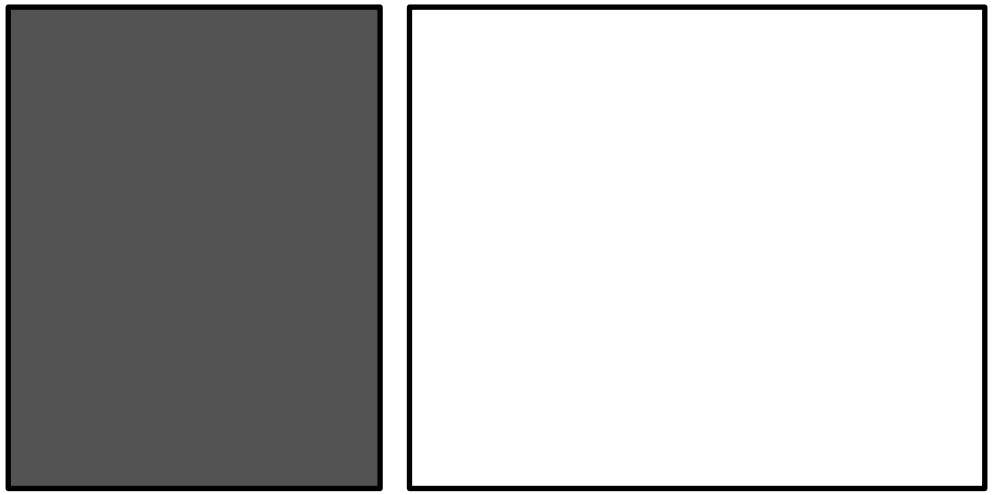


Touché

Touché = SIGN + TADA + SMARK

Using **“SIGN+TADA+SMARK”,** Touché enables to store



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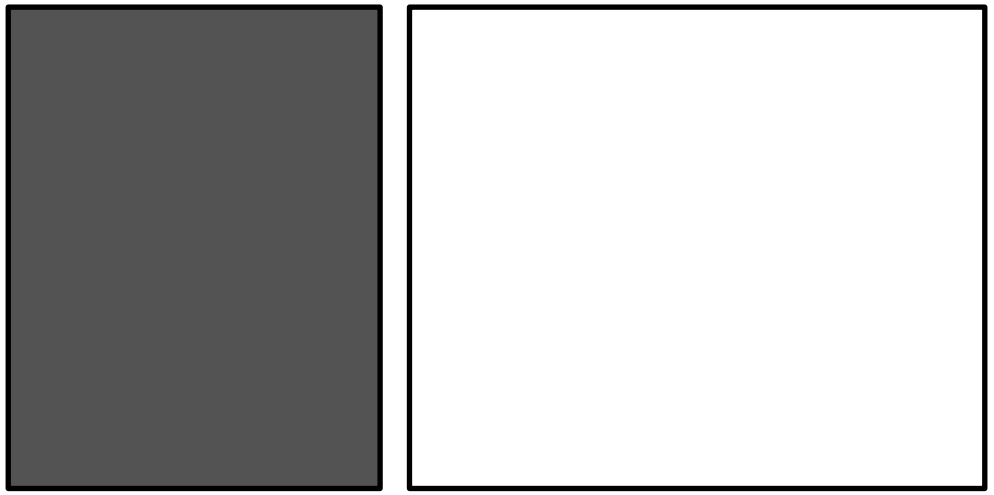

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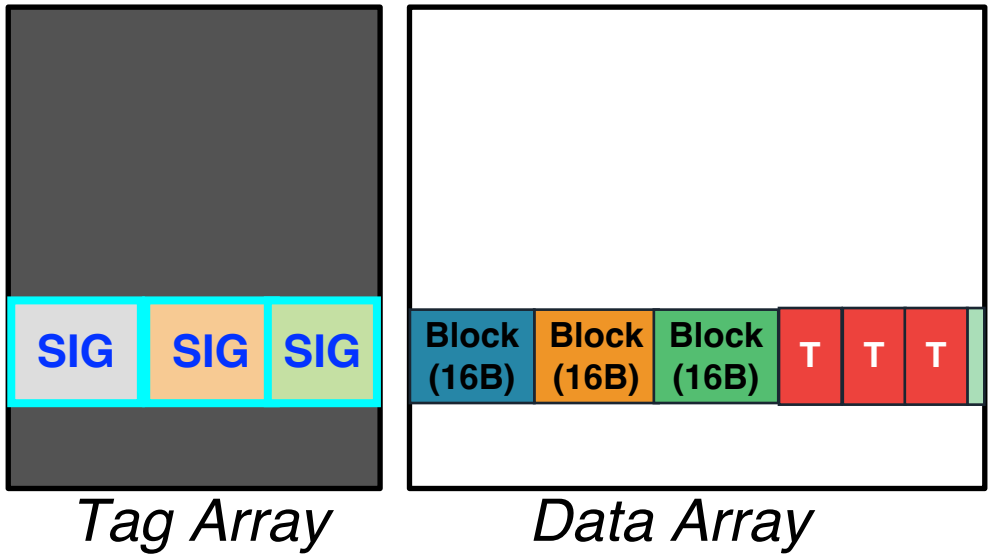

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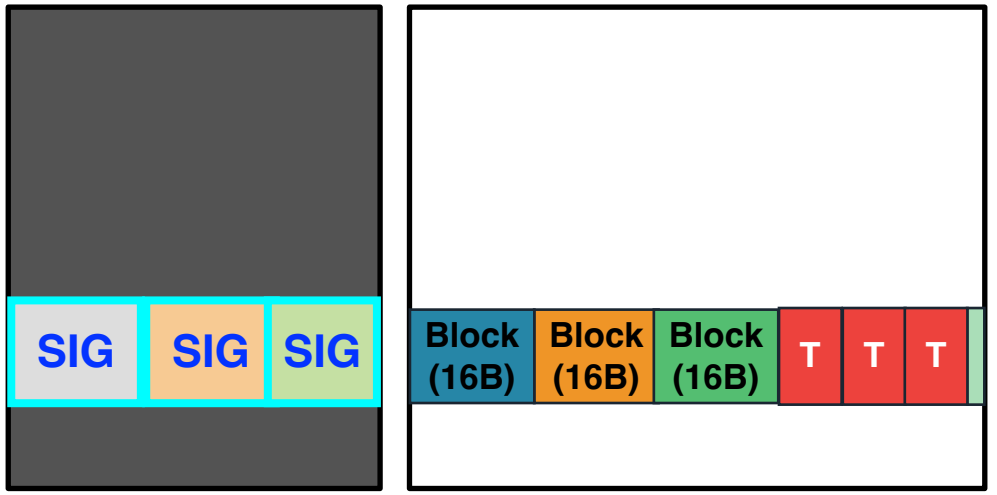

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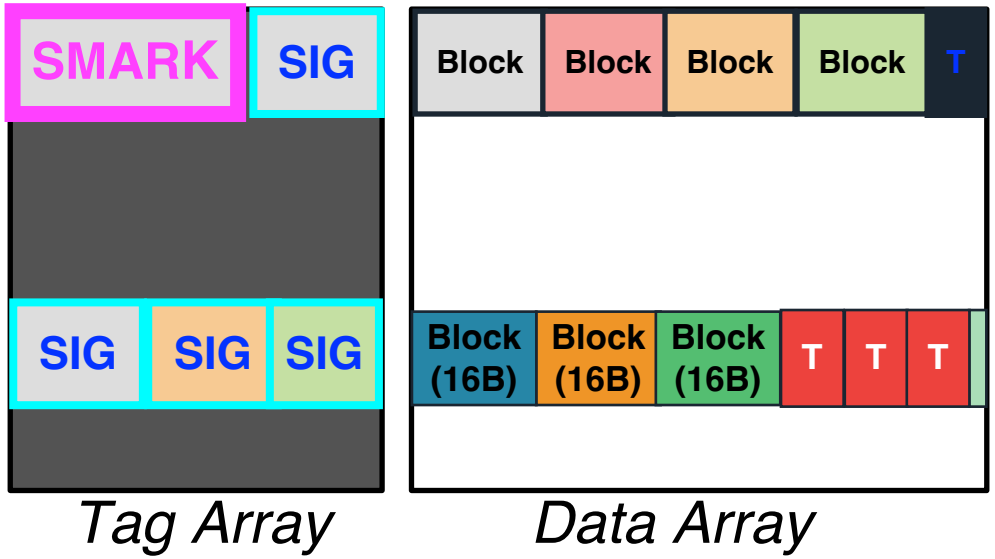

Touché

Touché = SIGN + TADA + SMARK

Using “**SIGN+TADA+SMARK**”, Touché enables to store
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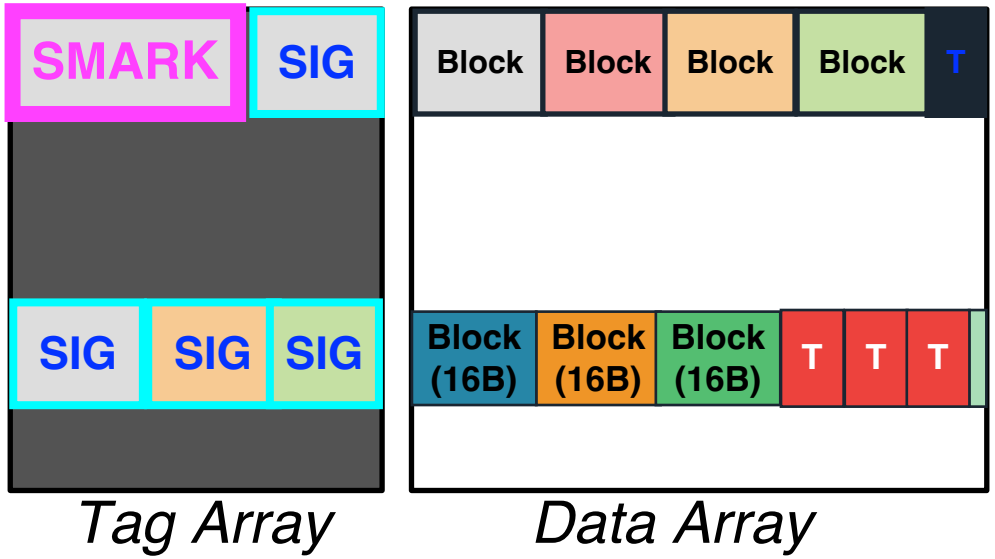
without any tag overheads!



Touché

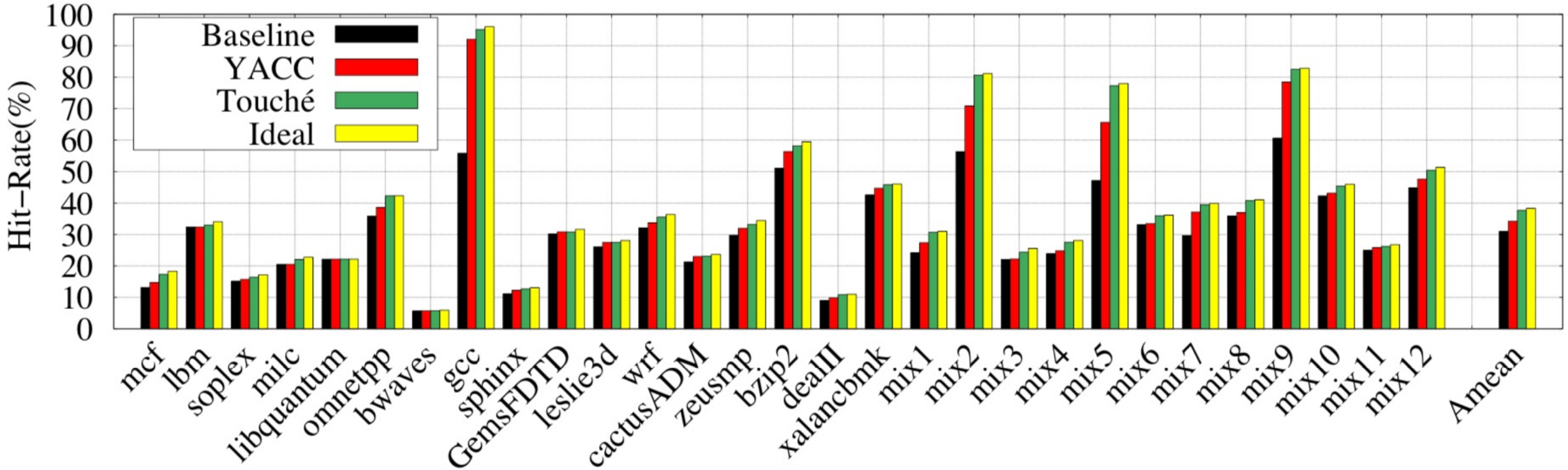
Experimental Methodology

✓ **Trace-based in-house cache simulator based on the USIMM**
- Detailed cache hierarchy
- Processor core models

✓ **Compression algorithms**
- BDI [G. Pekhimenko et al]
- FPC [Alaa R Alameldeen et al]

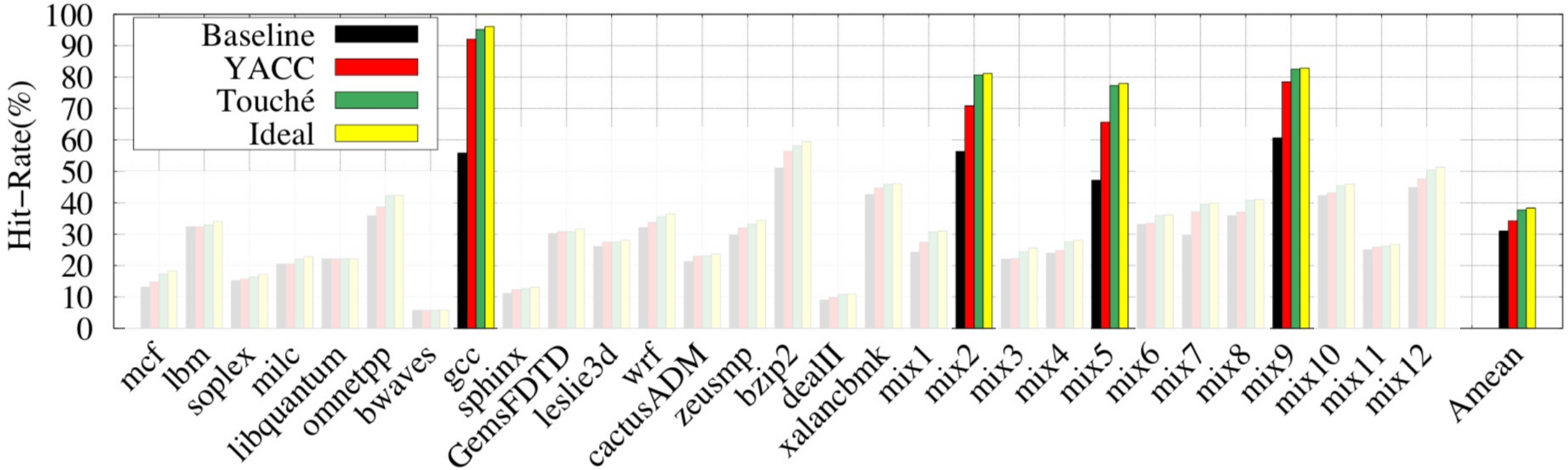
Number of Core **Processor Clock Frequency** **Issue Width**	4 3.2 GHz 8
L1 Cache (Private) **L2 Cache (Private)**	32KB, 8-way, 64B, 4 cycles 256KB, 8-way, 64B, 12 cycles
Last-level Cache **LLC Tag Access** **LLC Data Access**	4MB, 8-way, 64B 5 cycles 30 cycles
Memory Bus Frequency **Memory Channels** **Rank per Channel** **Bank Groups** **Banks per Bank Group** **Rows per Bank** **Columns per Row**	1600MHz (DDR 3200MHz) 2 1 4 4 64K 128
DRAM Access Timings: RCD-RP-CAS **DRAM Refresh Timing: RFC**	22-22-22 420ns

Effect on Last-level Cache Hit-Rate



Effect on Last-level Cache Hit-Rate

Touché achieves dramatic increase in the LLC Hit-Rate for the workloads extremely sensitive to the LLC capacity



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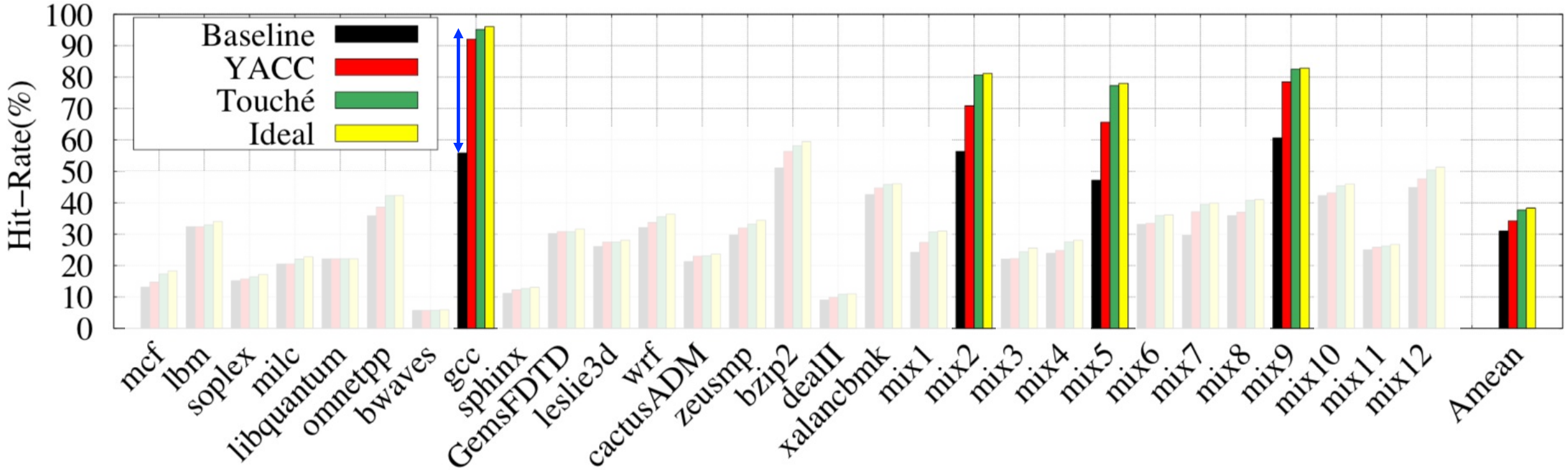
- The hit-rate of gcc increases from 55% to 95%!



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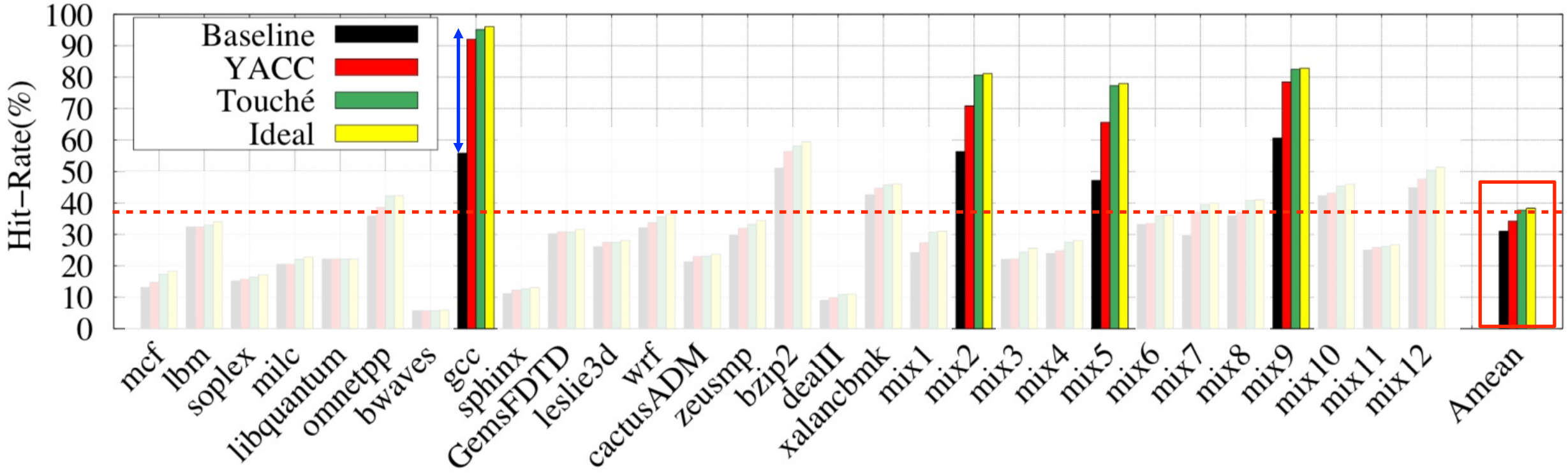
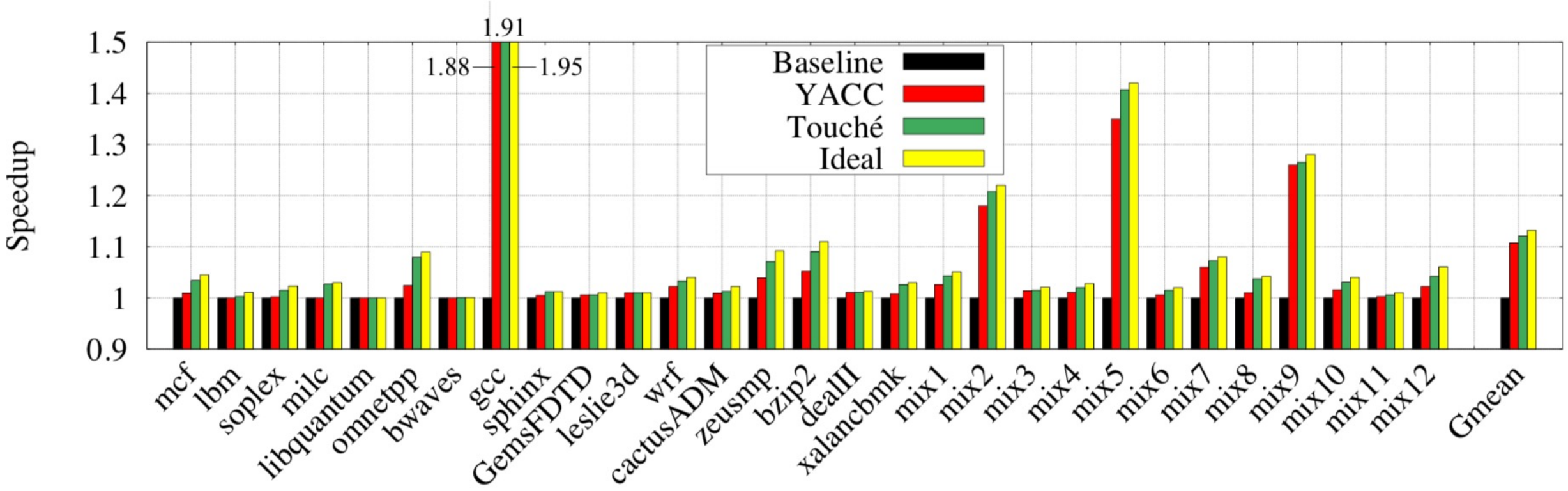


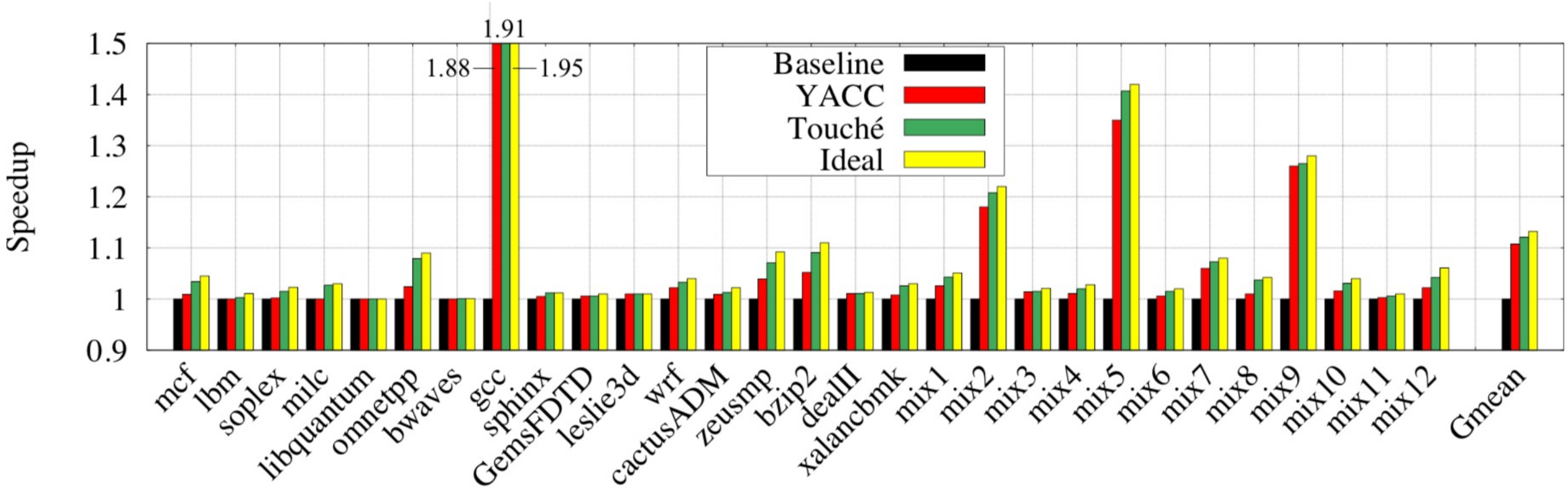
On average, Touché increases the hit rate by 6% (Ideal – 7%)

Performance Impact



Performance Impact

Touché improves the performance significantly for workloads that are sensitive to the LLC capacity!



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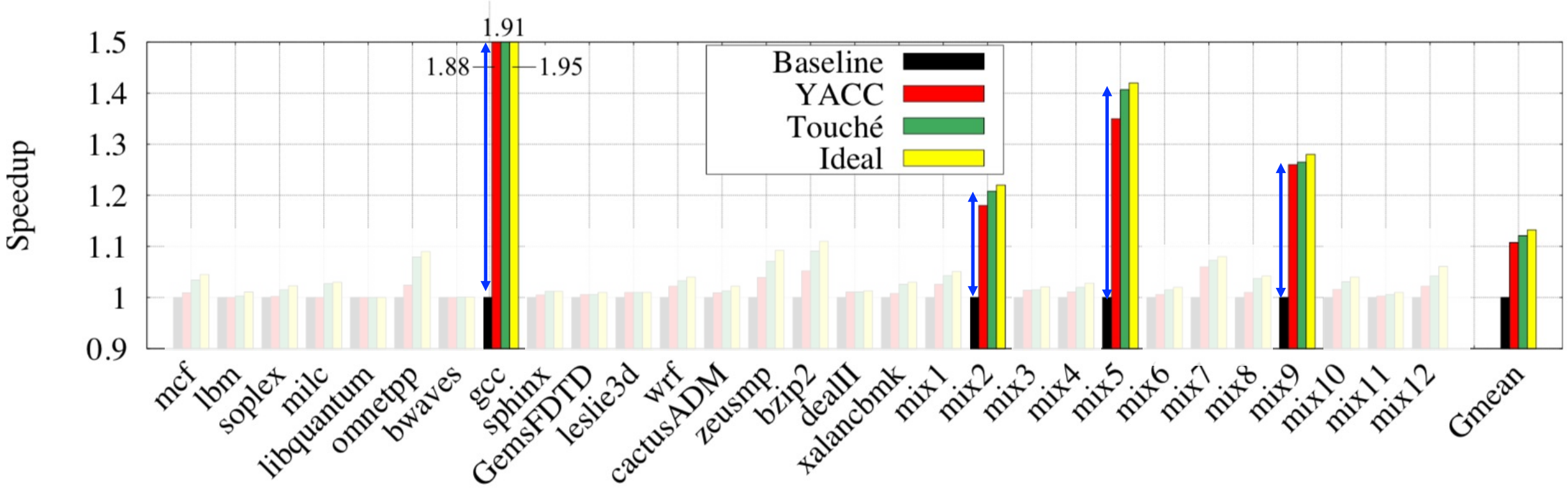

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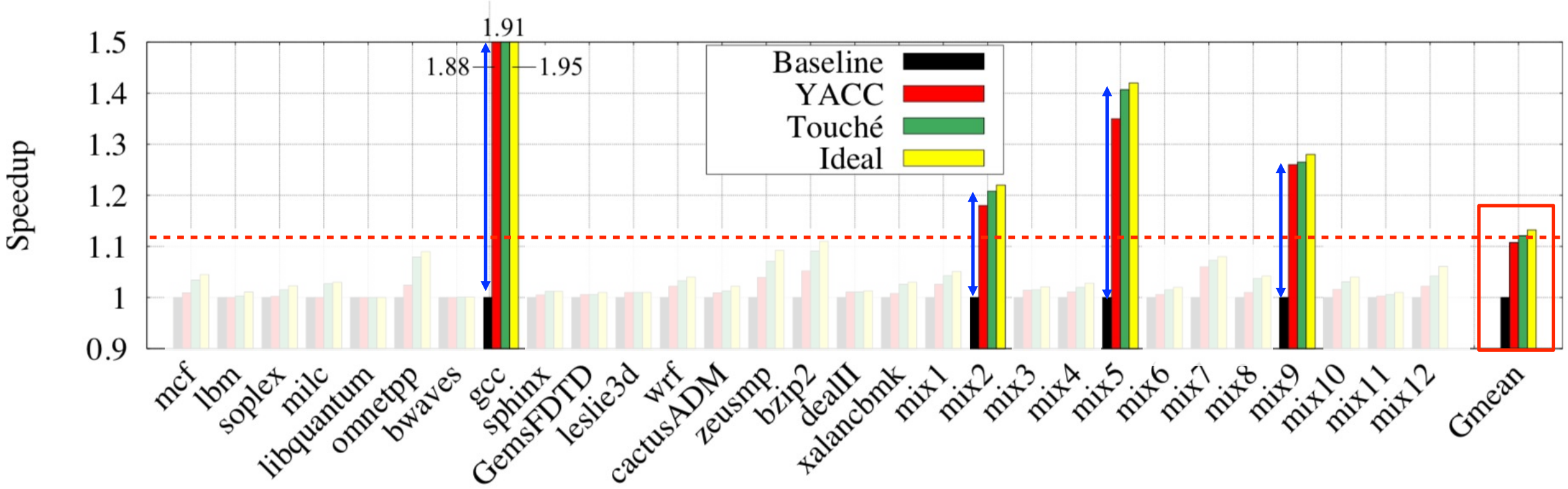

On average, Touché achieves a speedup of 12% (Ideal : 13%)

Summary

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Summary

- Last-Level Cache (LLC) capacity/core has stagnated over the past decade.
- Data compression is a promising technique to increase the effective capacity of LLC.
- However, compressed blocks require additional tag entries.
- **Touché** is a framework that enables LLC compression without any area overheads in the tag or data arrays.
- **Touché** is completely hardware based and achieves a near-ideal speedup of 12% without any area overheads.

Thanks!

"Eureka! Another breakthrough in compression technology!"