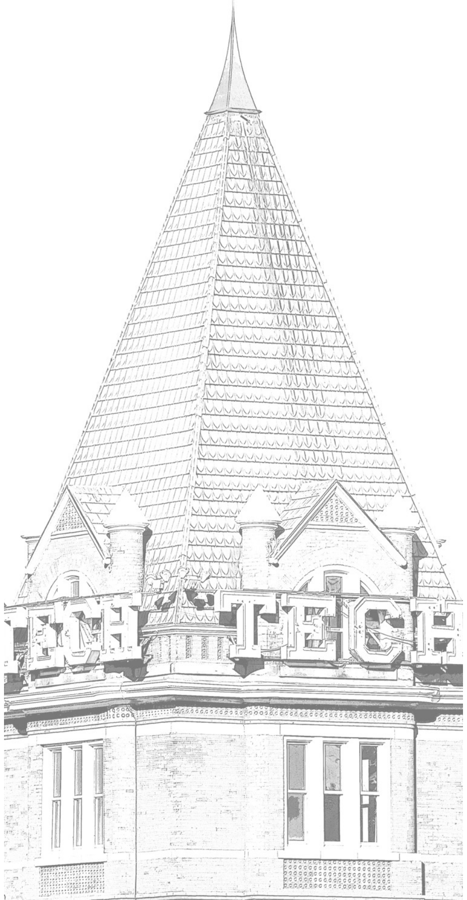
Citadel: Efficiently Protecting Stacked Memory From Large Granularity Failures



Dec 15th 2014

MICRO-47 Cambridge UK

Prashant Nair - Georgia Tech

David Roberts - AMD Research

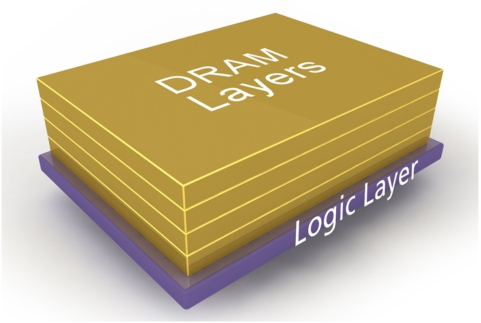
Moinuddin Qureshi - Georgia Tech

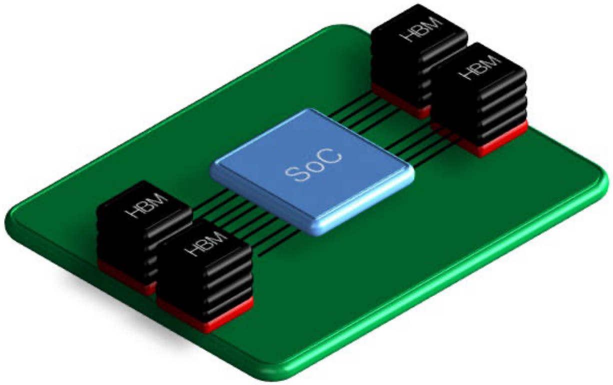
Georgia Institute of Technology

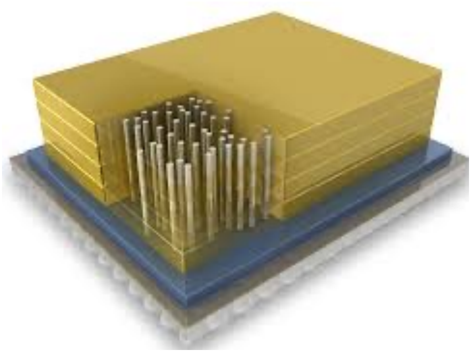
AMD

INTRODUCTION TO 3D DRAM

- DRAM systems face a bandwidth wall







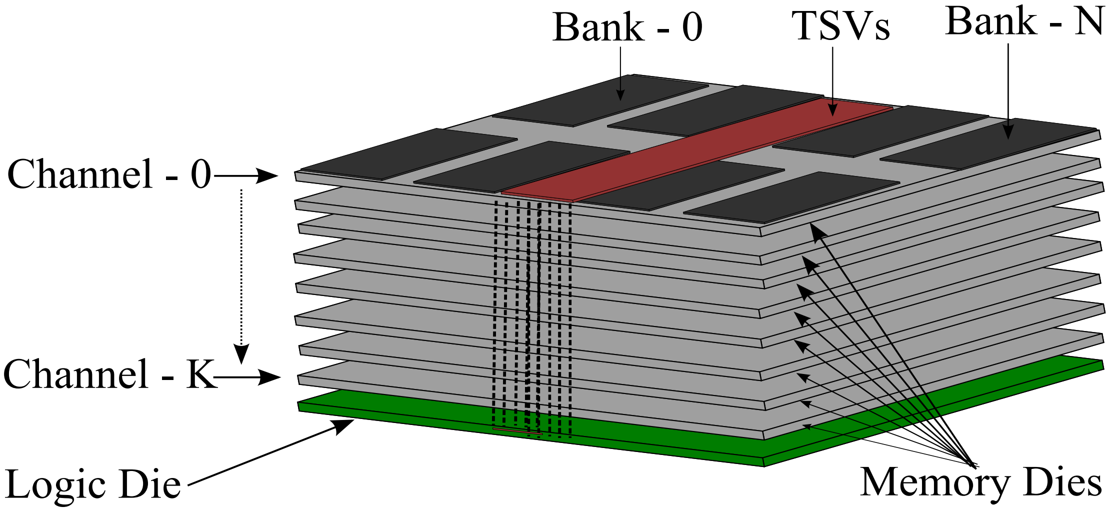
- Stack DRAM Dies over each other → 3D DRAM
- Use Through Silicon Vias (TSV) to connect Dies
- Higher density of TSV → Higher Bandwidth

Go 3D to Scale Bandwidth Wall

Courtesy MICRON, Extremetech

FAILURES IN 3D DRAM

- 3D DRAM ➡ Communicate using TSVs

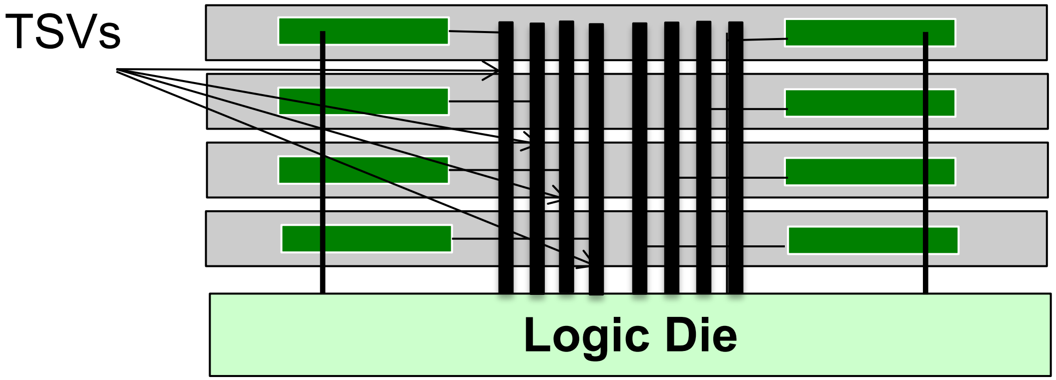


- A New Failure Mode: TSV Failures
- TSV Failures ➡ Large Granularity Failures

TSVs Present New Kind of Large Granularity Failures

A NEW FAILURE MODE FROM TSVs

TSVs conduit for Address and Data



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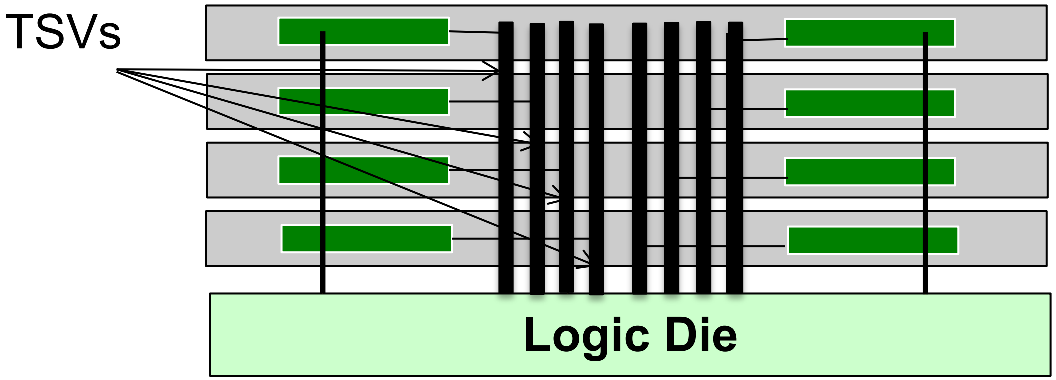

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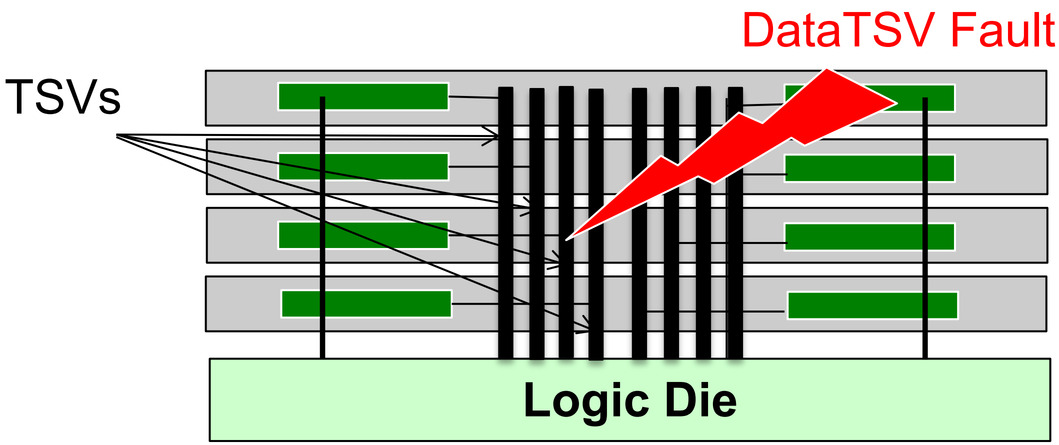

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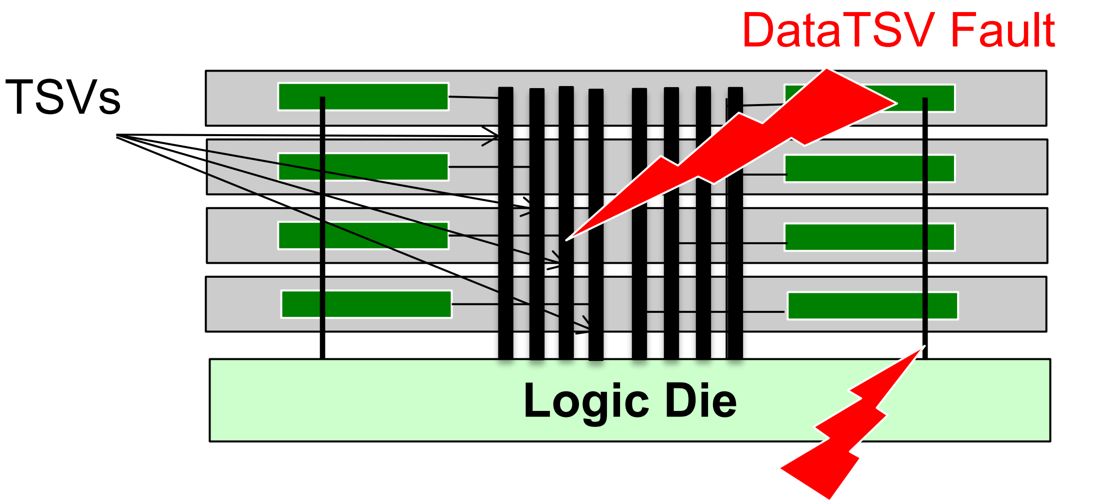

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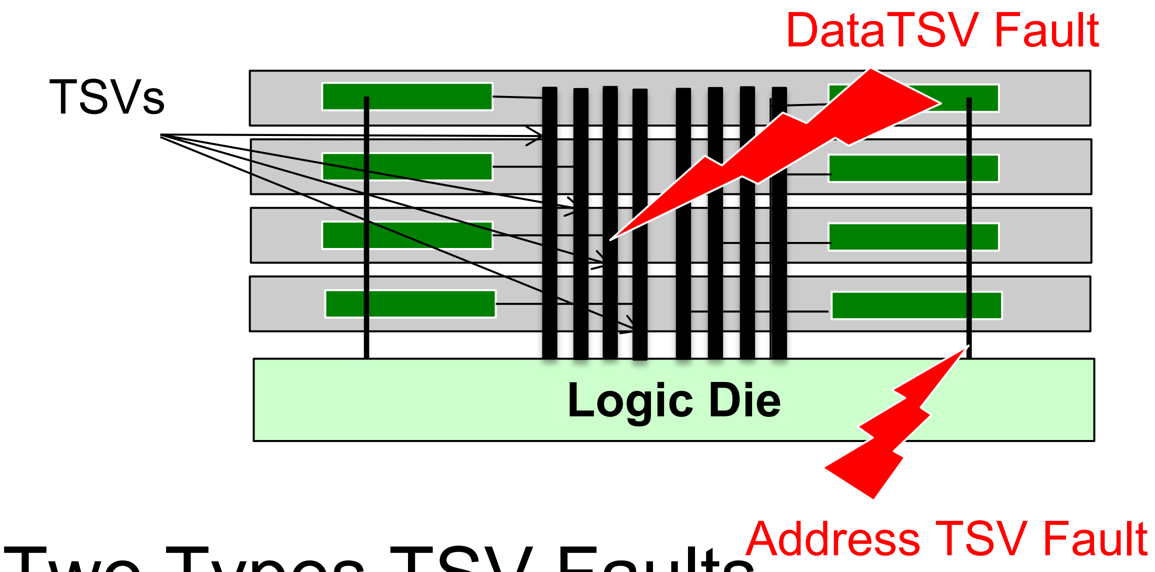


- Mainly Two Types TSV Faults

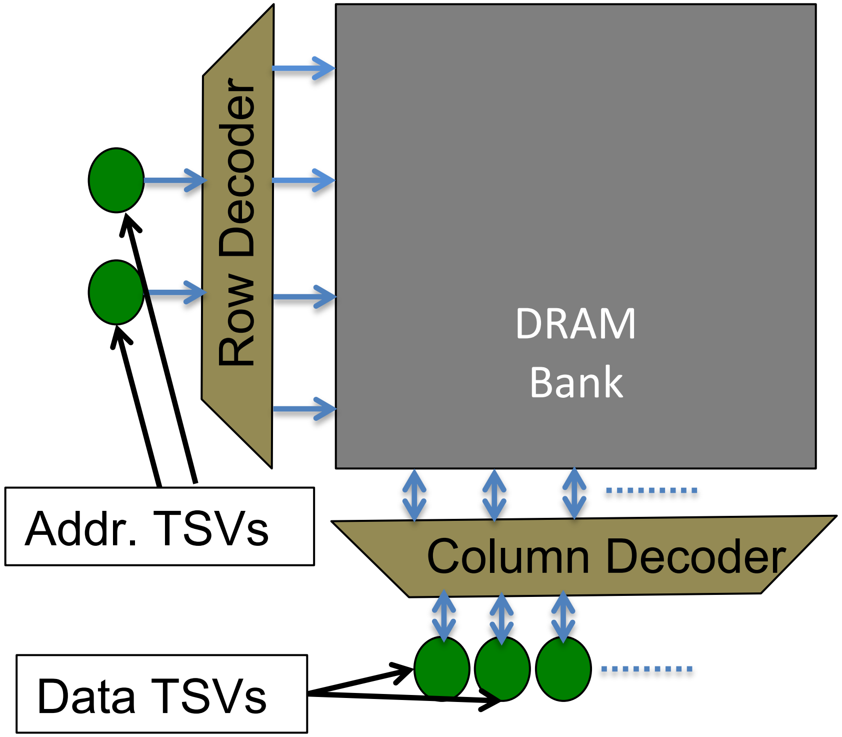
– Data (Incorrect Data fetched from DRAM Die)

– Address (Incorrect address presented to DRAM Die)

TSV Faults cause unavailability of Data and Addresses

EFFECT OF TSV FAULTS

- Data TSV Fault ➡ Few Columns Faulty



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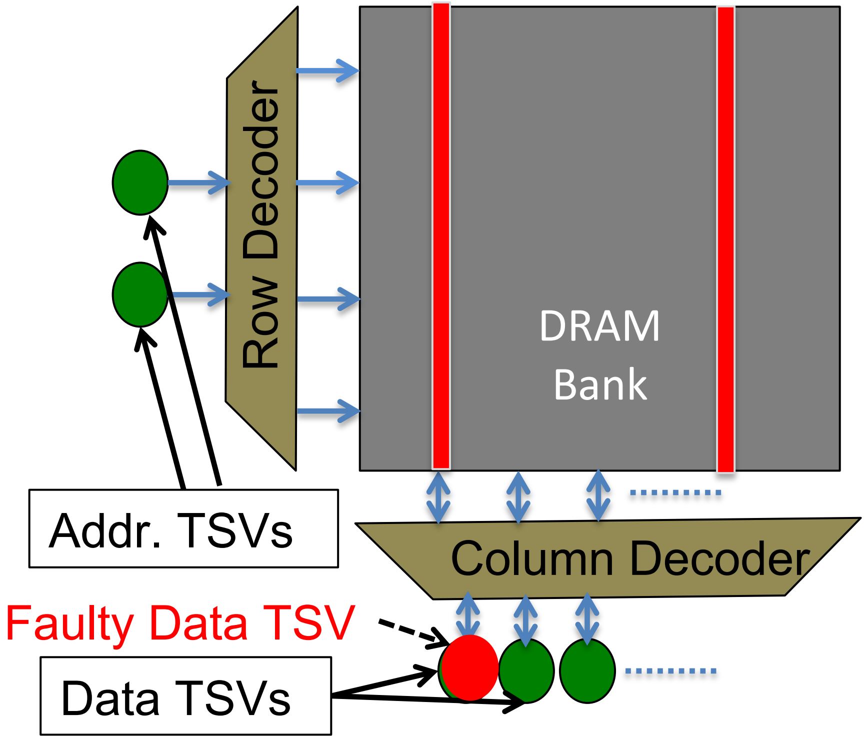

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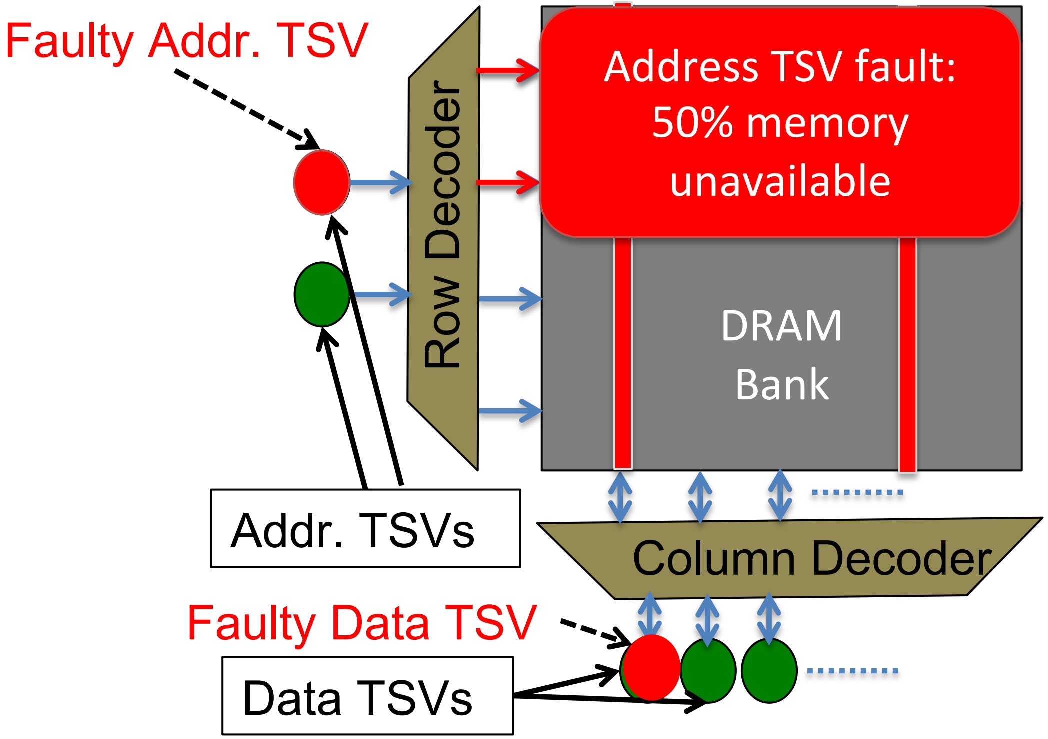
- Address TSV Fault ➡ 50% Memory Loss



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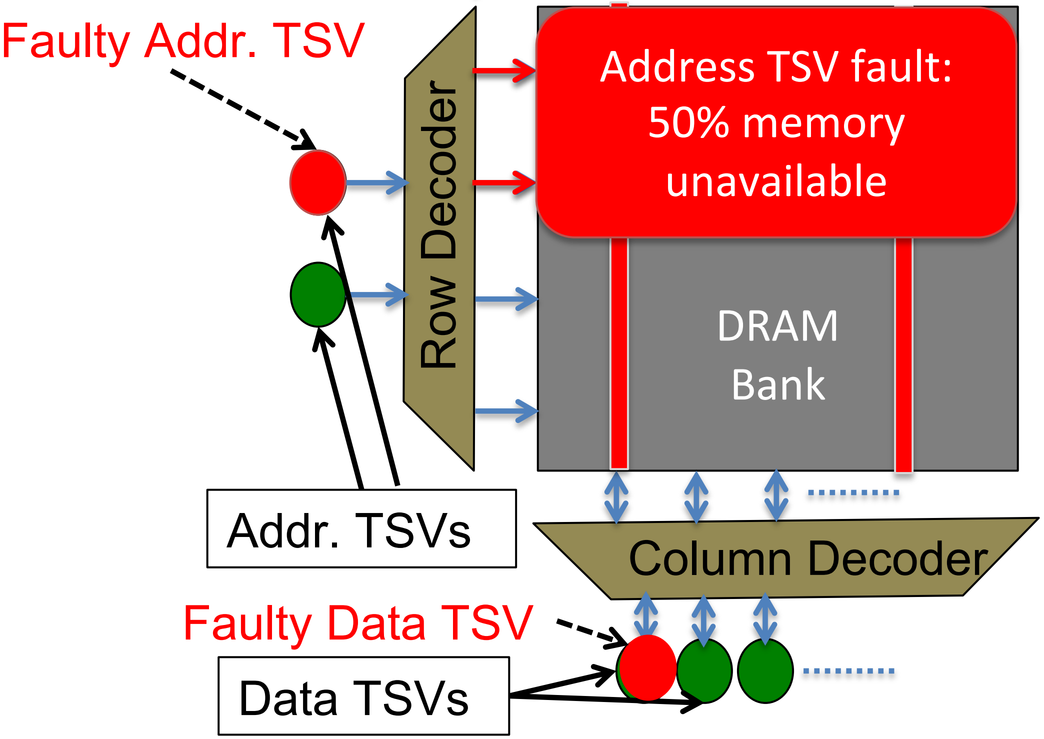
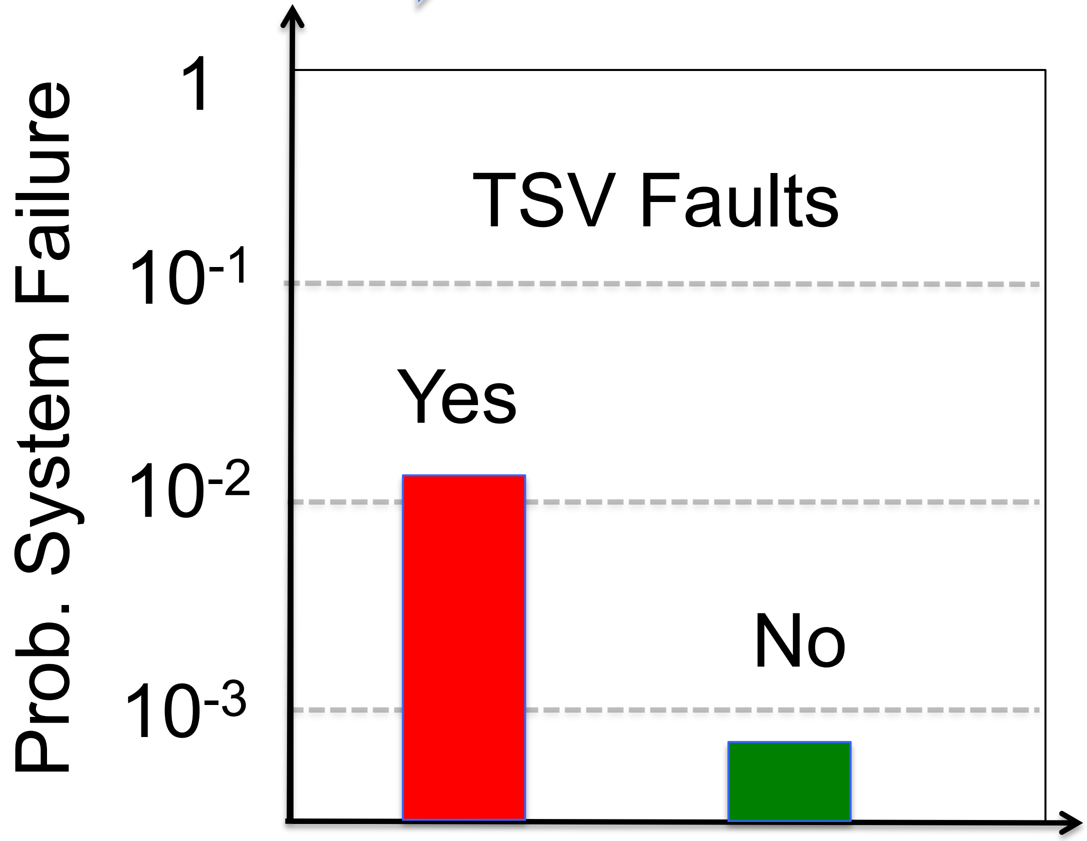


TSVs can cause failures at multiple granularities

IMPACT OF TSV FAULTS

System: 8GB Stacked Memory (HBM)

Prob. System Failure ➡ Prob(Uncorrectable Error)



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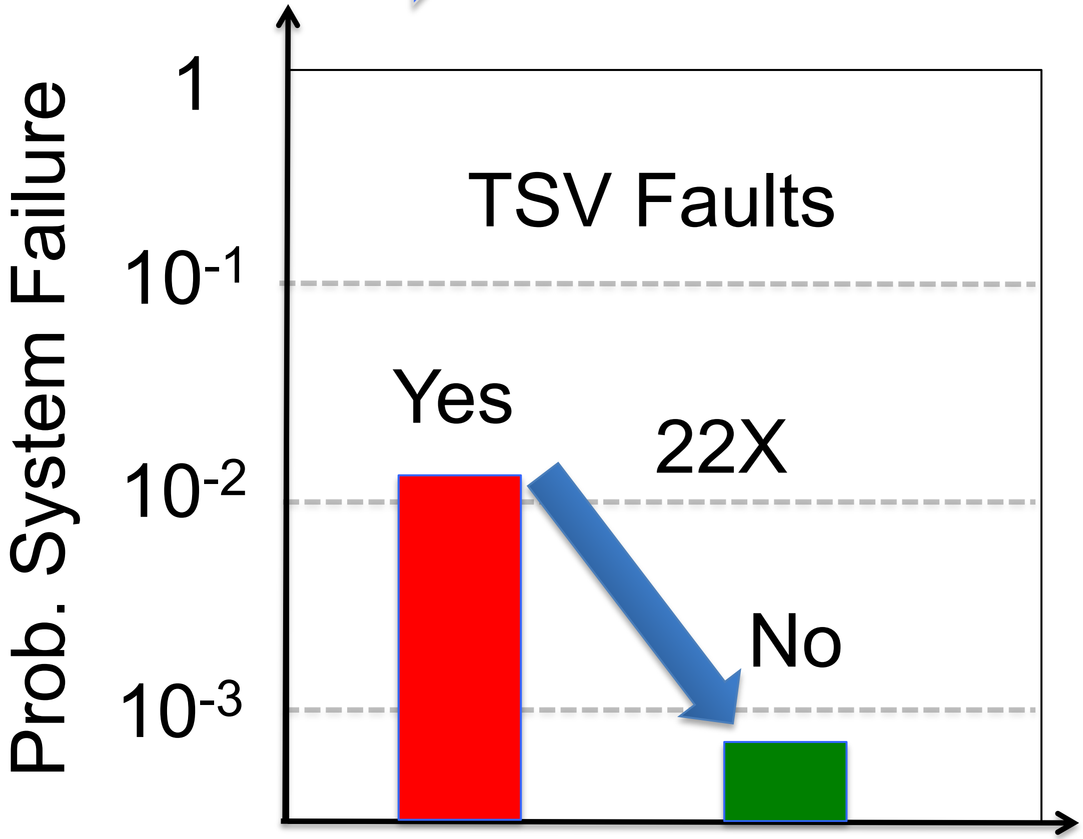
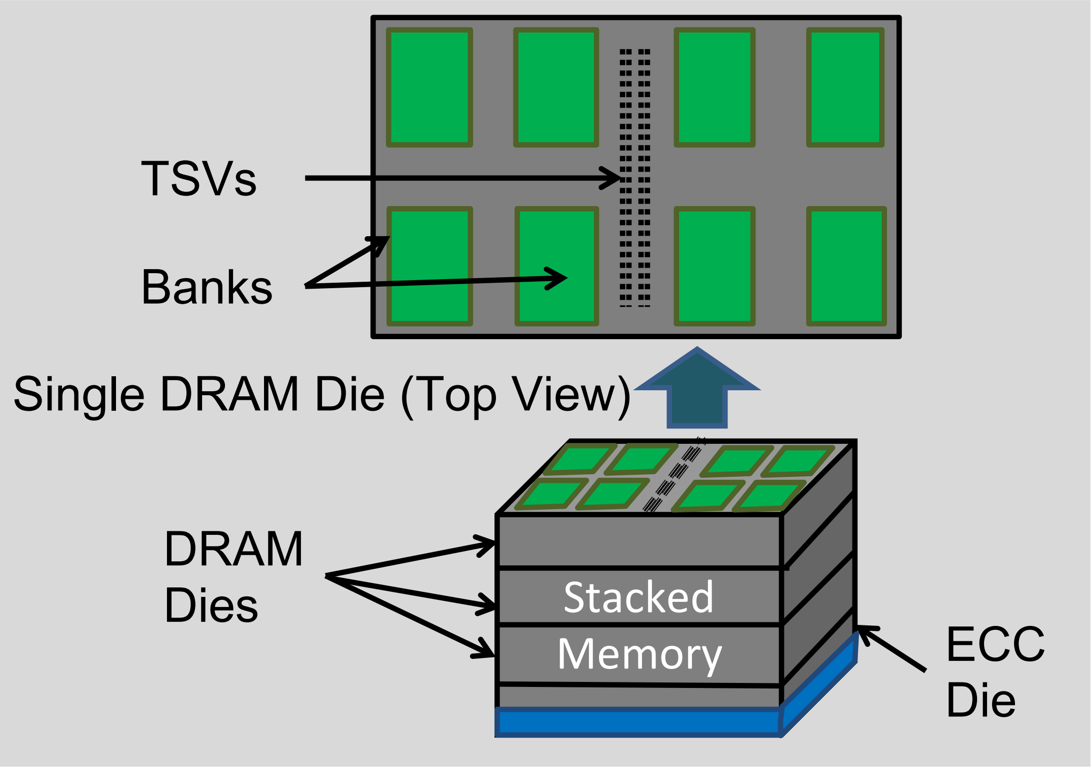


Efficient Techniques to Mitigate TSV Faults

OTHER FAILURES STILL PRESENT



TSVs

Banks

Single DRAM Die (Top View)

DRAM Dies

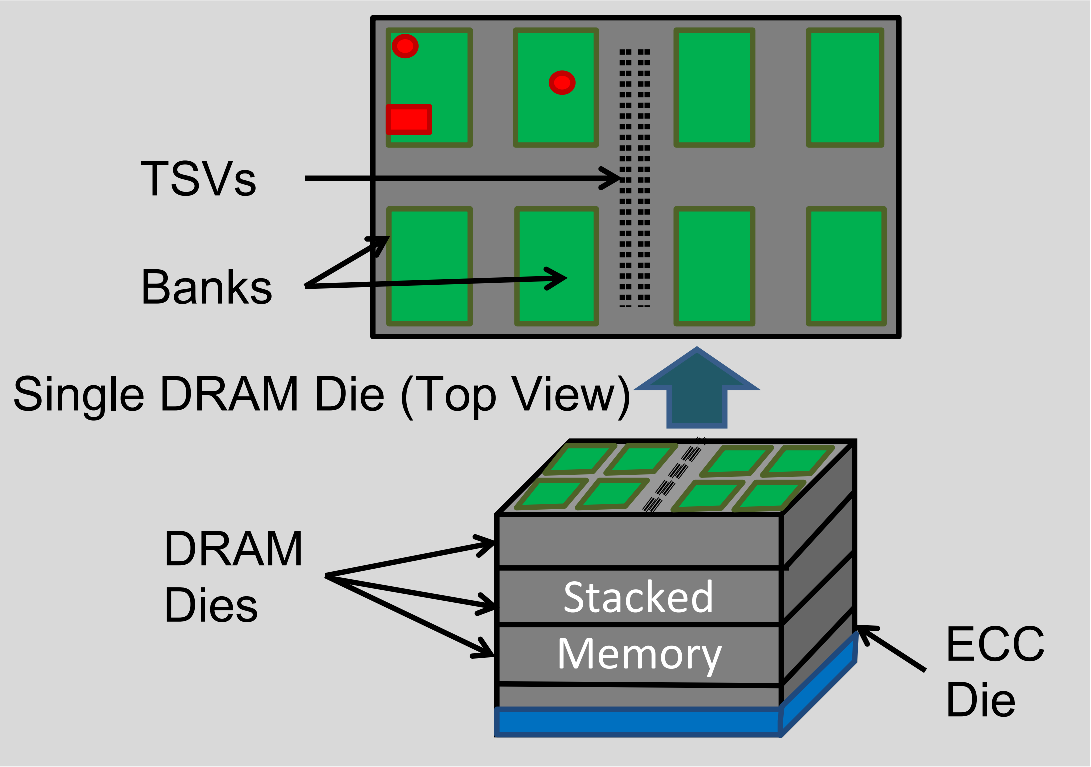
Stacked Memory

ECC Die

Apart from TSV Faults, 3D DRAM will also continue to have other multi-granularity failures

OTHER FAILURES STILL PRESENT

- Bit
- Word



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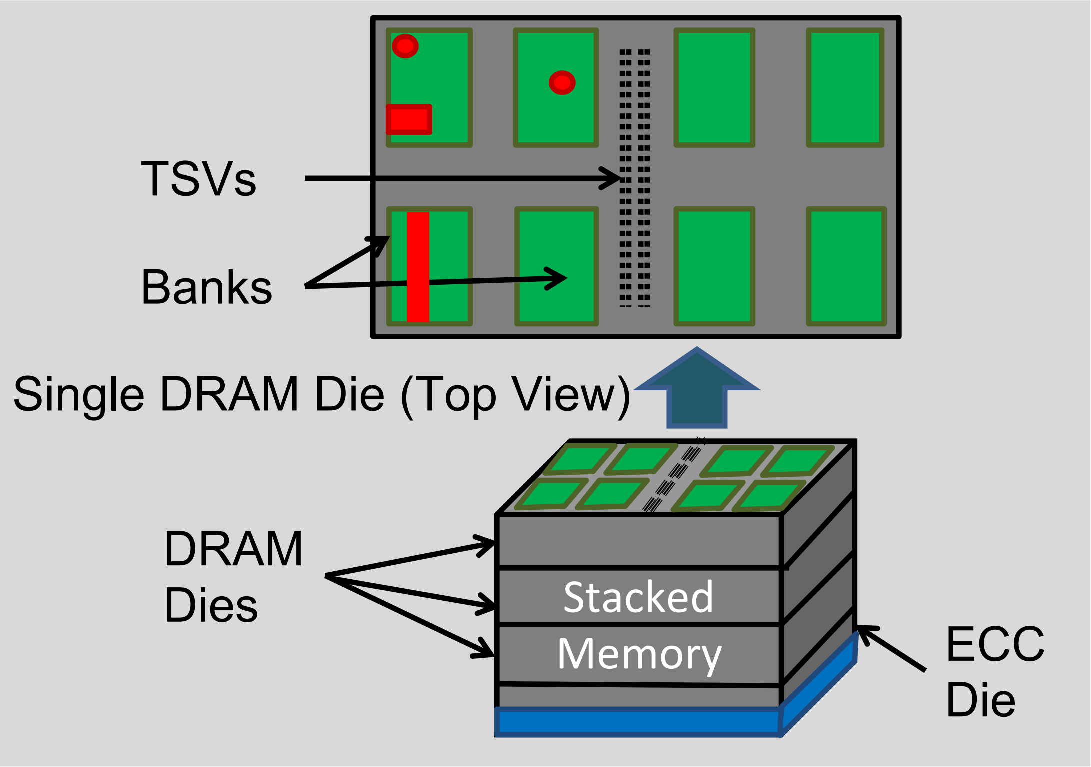

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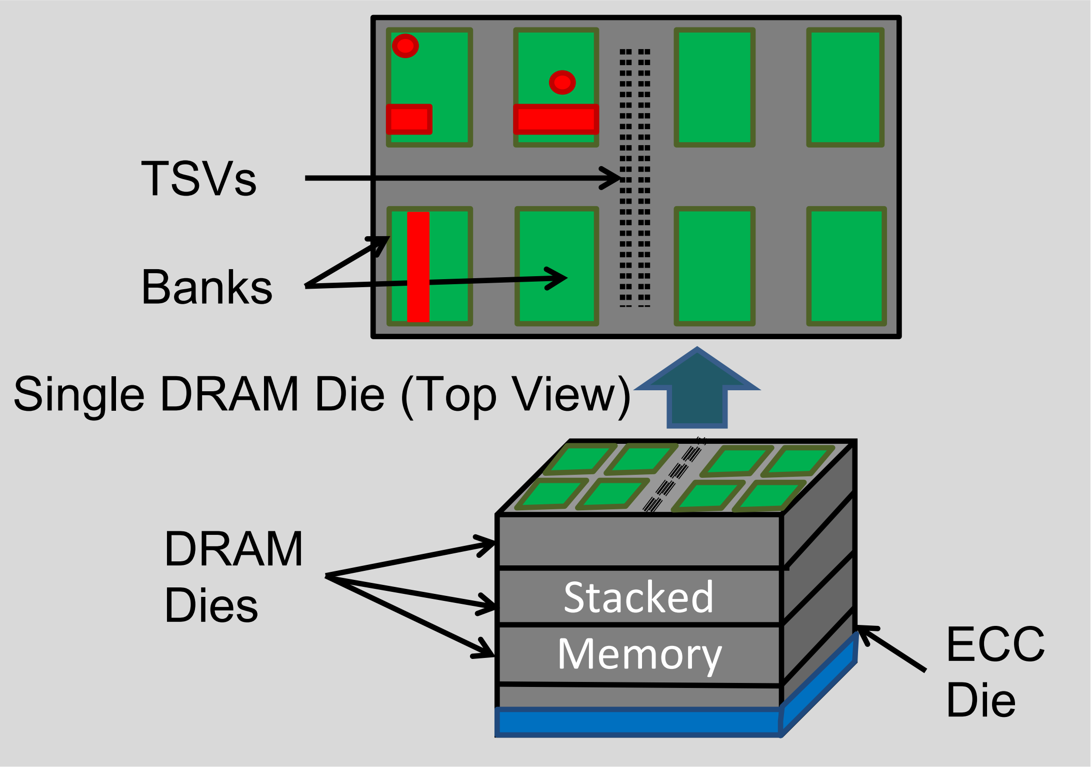

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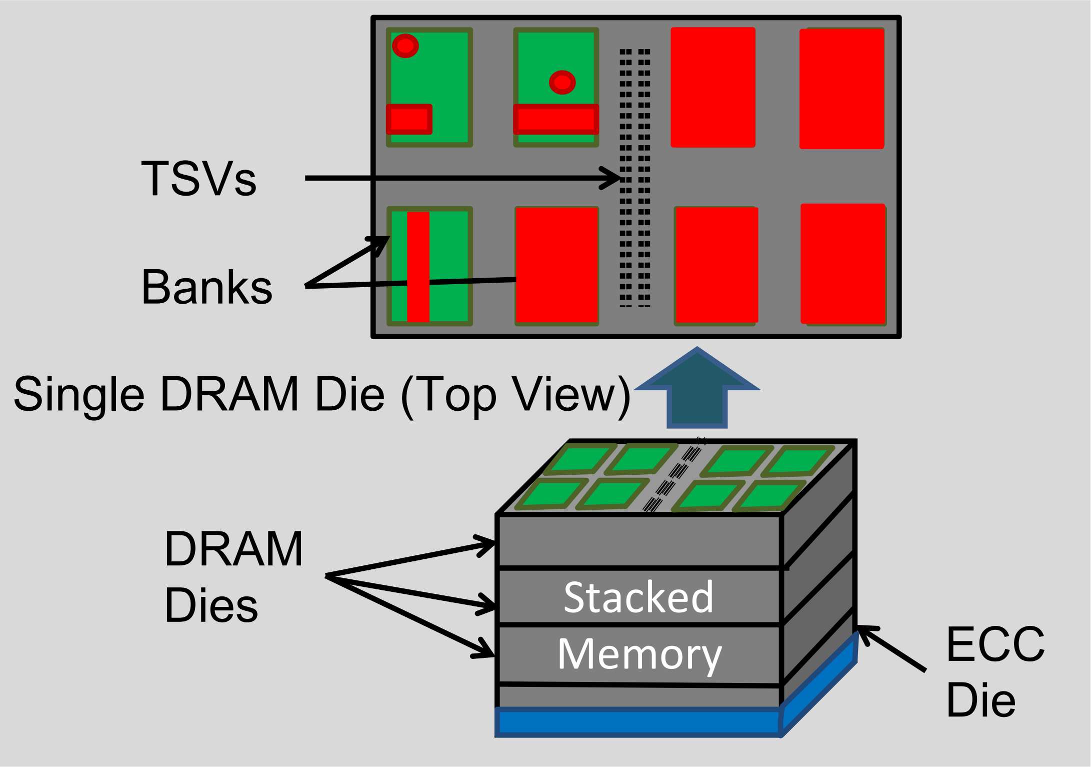

Apart from TSV Faults, 3D DRAM will also continue to have other multi-granularity failures

3D DRAM: FAILURE RATE

Die Failure Mode	*Permanent Fault Rate (FIT)
Bit	148.8
Word	2.4
Column	10.5
Row	32.8
Bank	80

*Projected from Sridharan et. al. : DRAM Field Study

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148.8 ✓ *SECDED*

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Bit 148.8: ✓ SECDED

Word + Column + Row + Bank = 125.7: ✗ SECDED

1. Large Granularity Faults are as likely as Bit Faults
2. Low Cost Solutions Required For Large Faults

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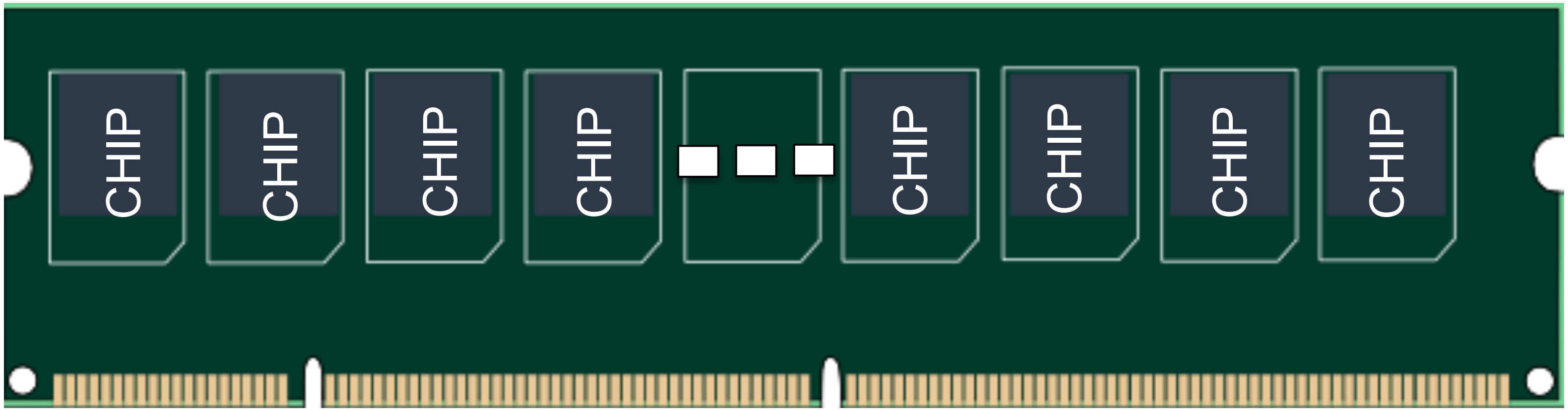
CONVENTIONAL SCHEMES

Current Systems Naturally Stripe Data Across Chips



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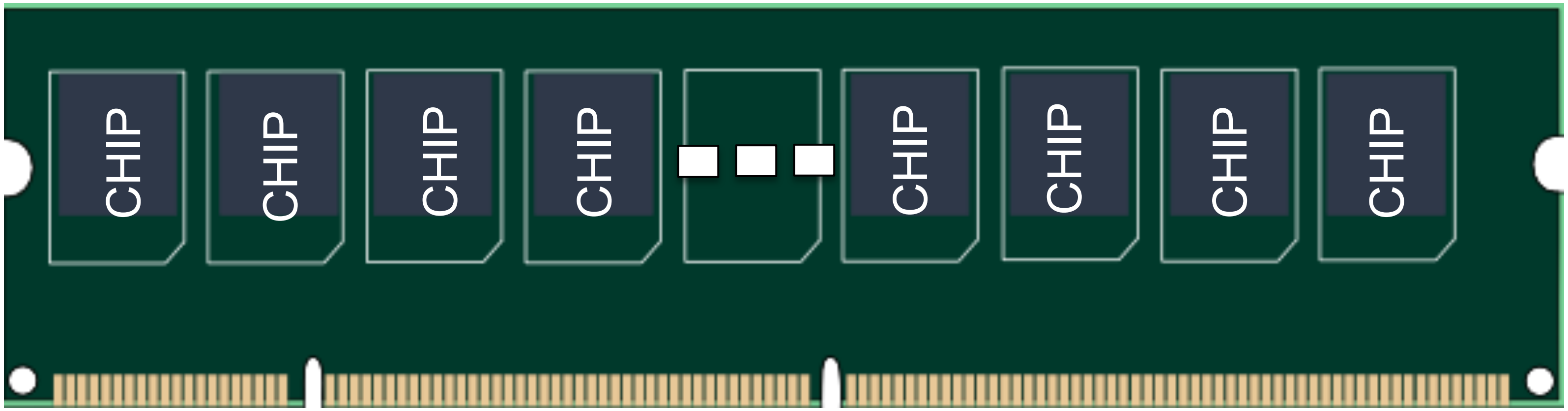

Cache Line = 64 Bytes

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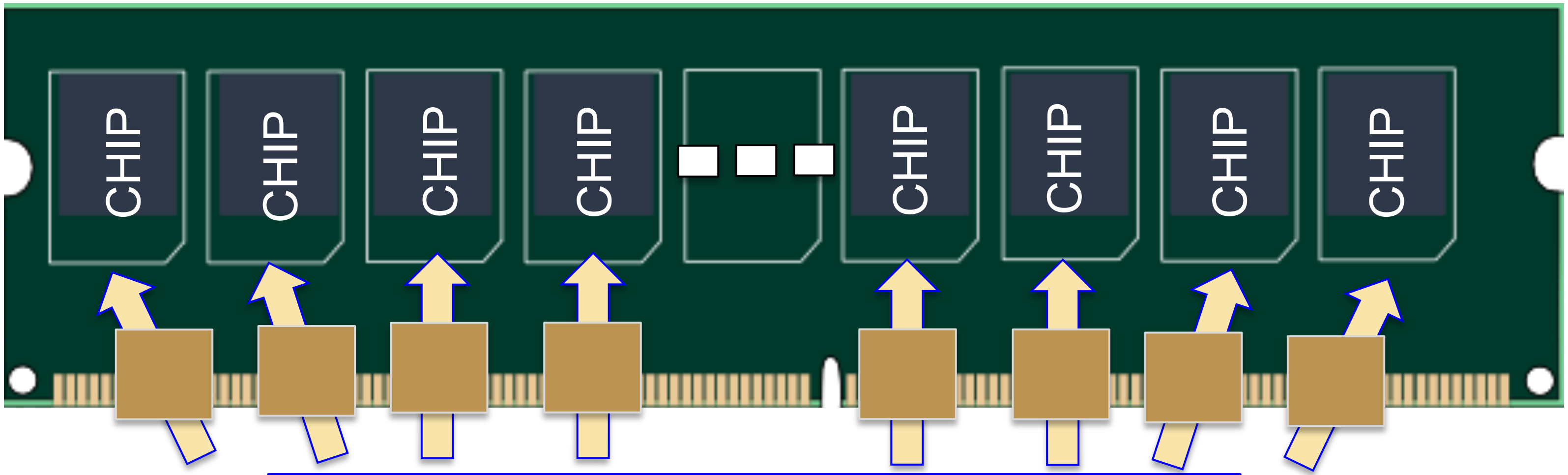

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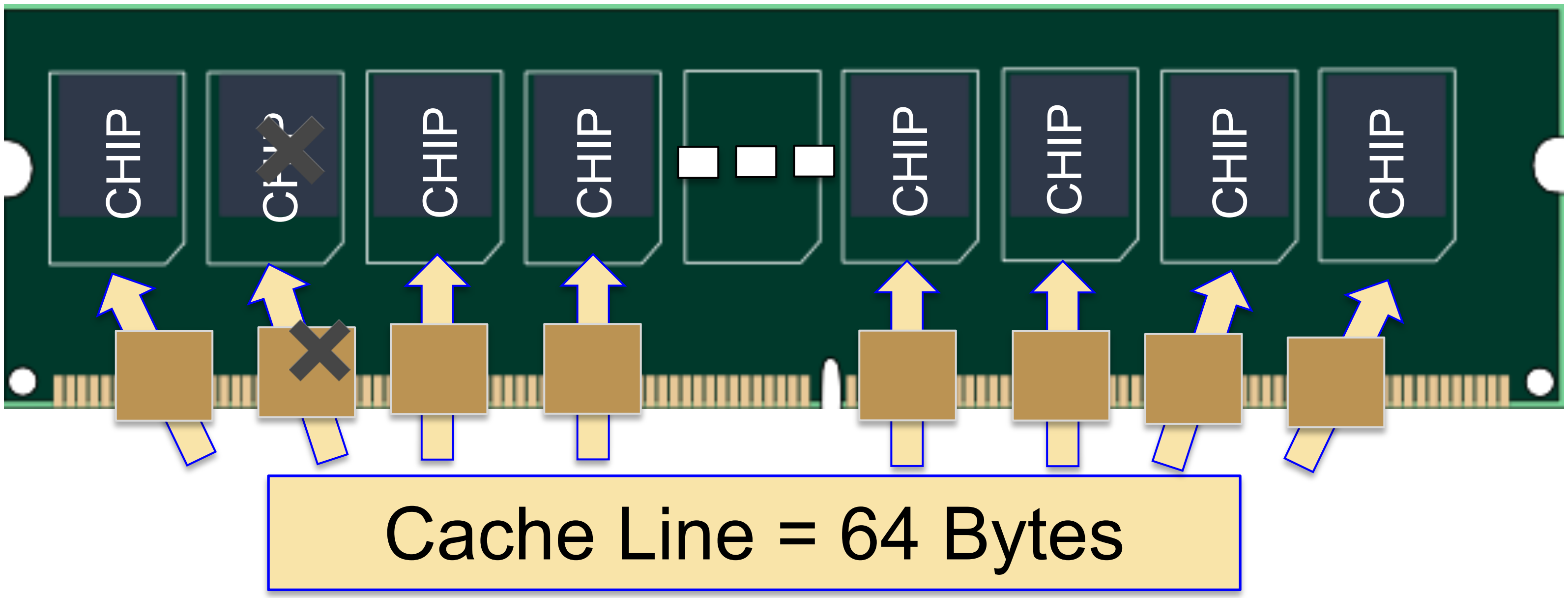

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- ChipKill : Mitigate Large Failures (Whole Chip)

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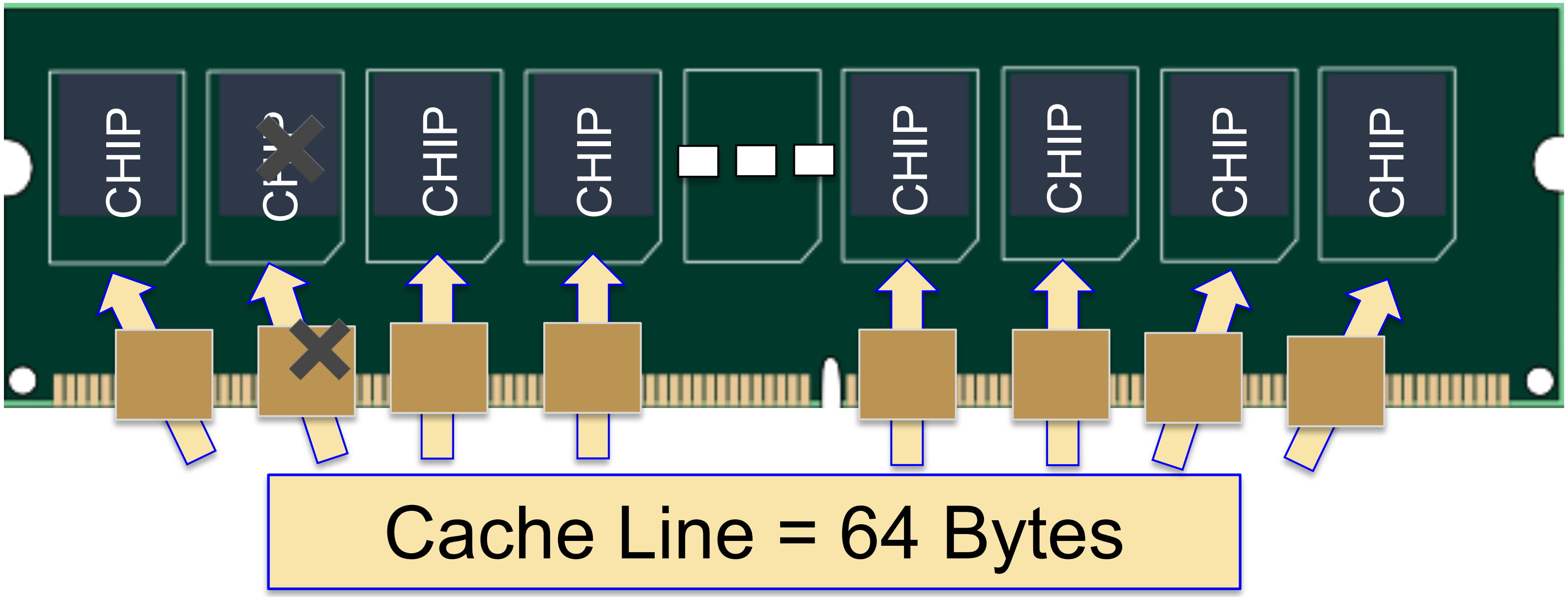
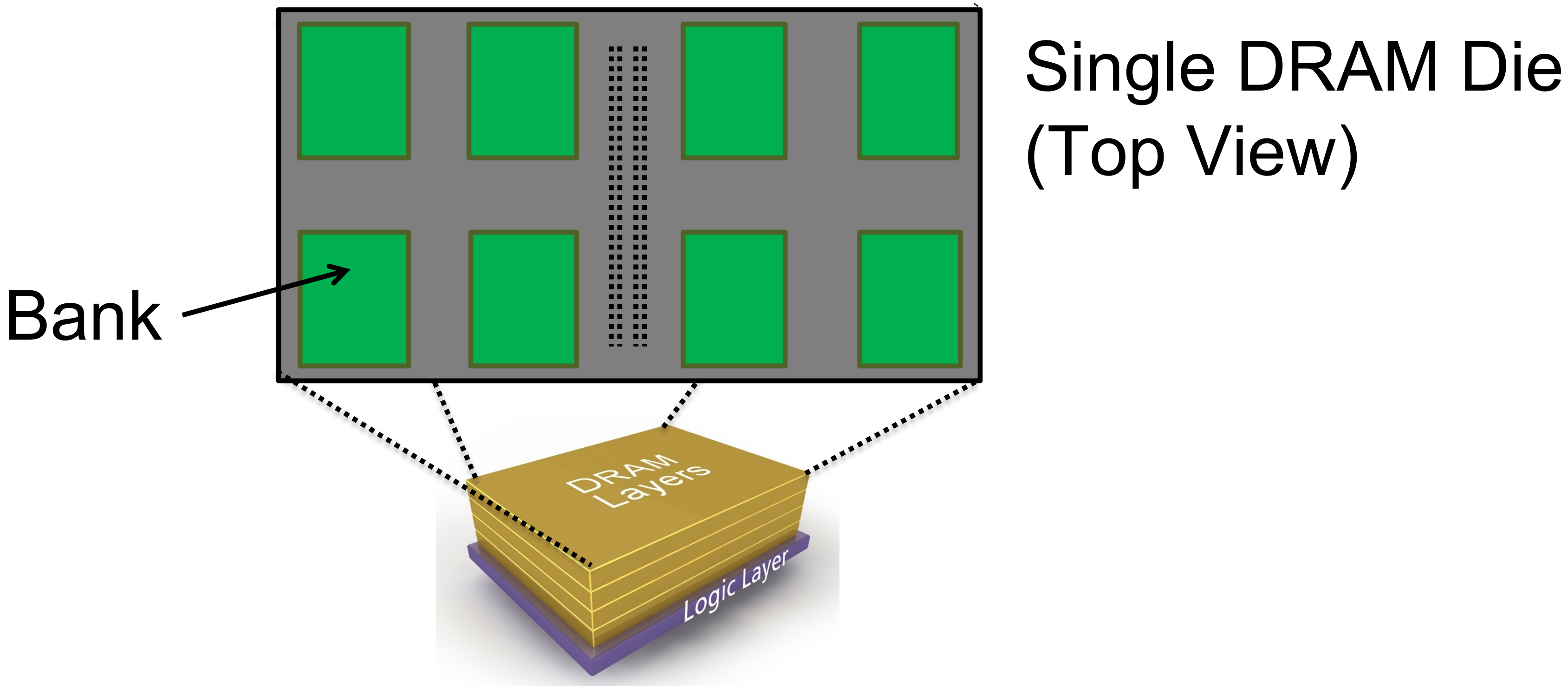


- ChipKill : Mitigate Large Failures (Whole Chip)

ChipKill relies on data striping to tolerate large granularity failures

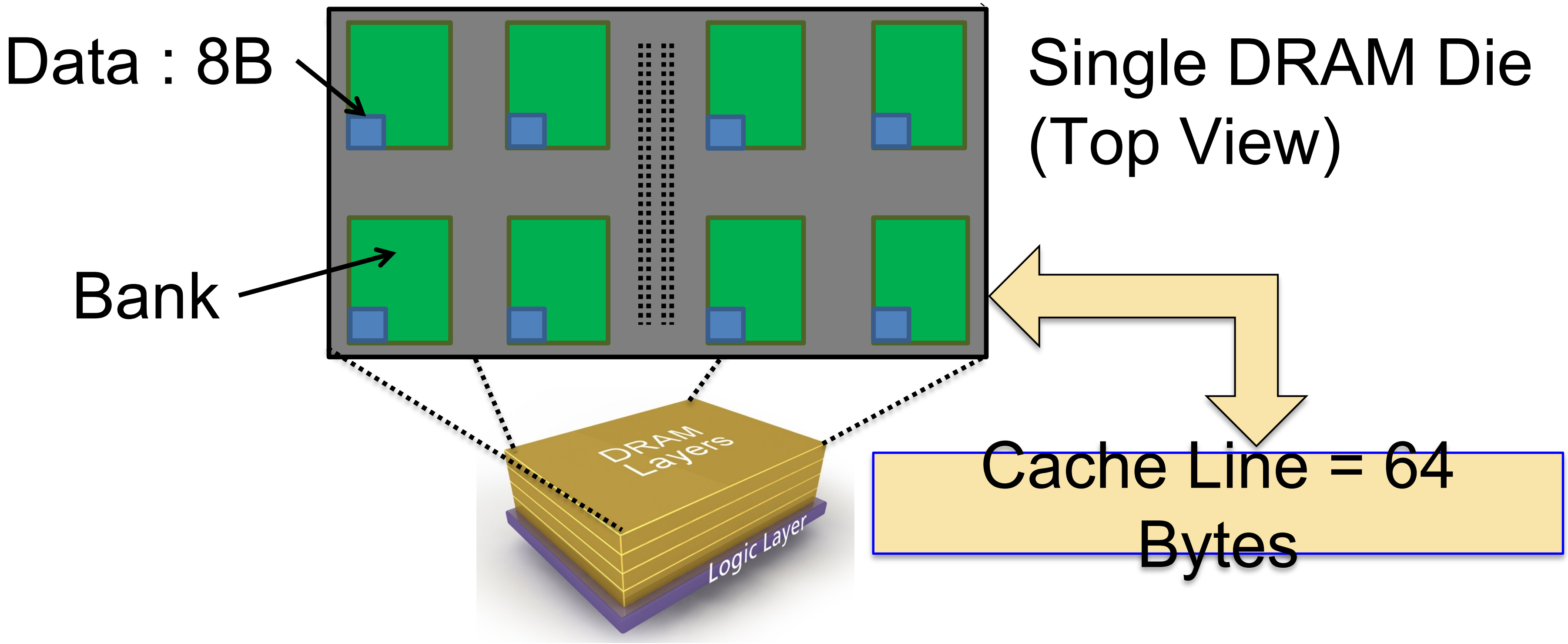
CHIPKILL IN STACKED MEMORY



Single DRAM Die (Top View)

Bank

CHIPKILL IN STACKED MEMORY



Data : 8B

Bank

Single DRAM Die
(Top View)

Cache Line = 64 Bytes

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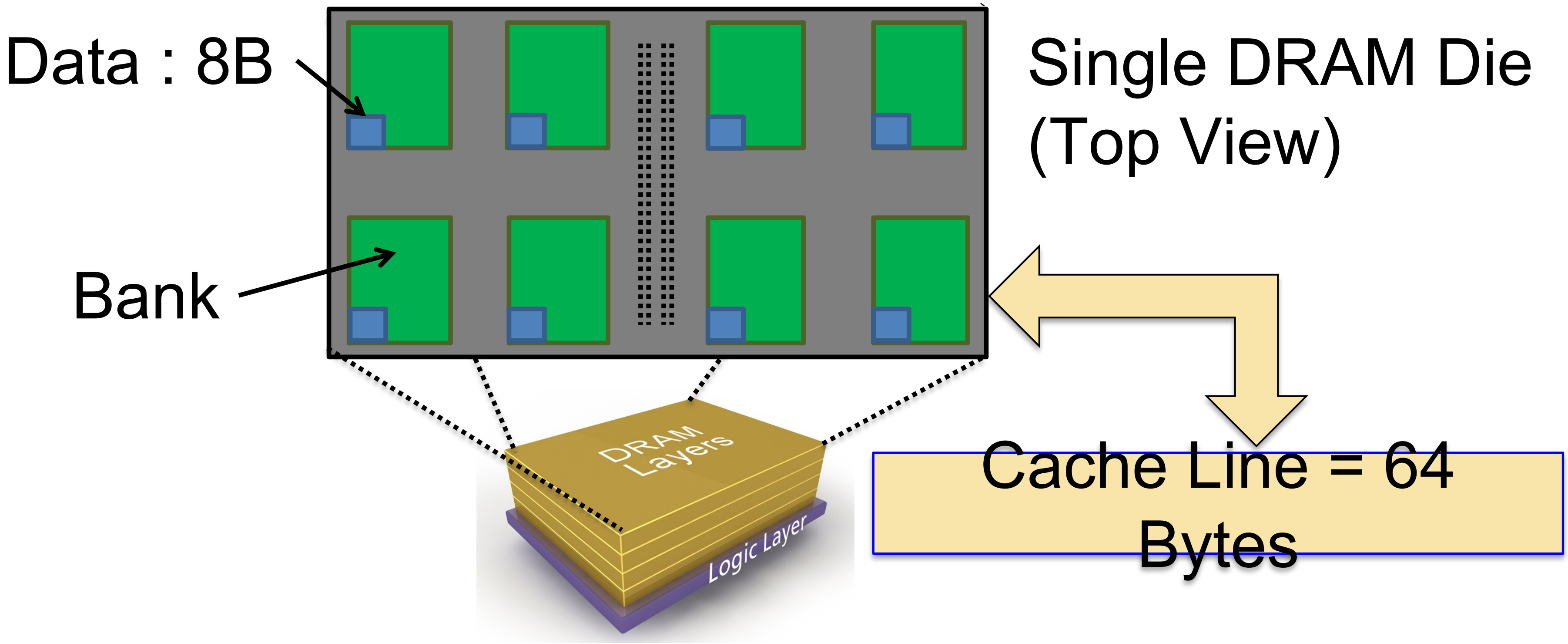

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- A request activates at least 8 Banks or 8 Channels

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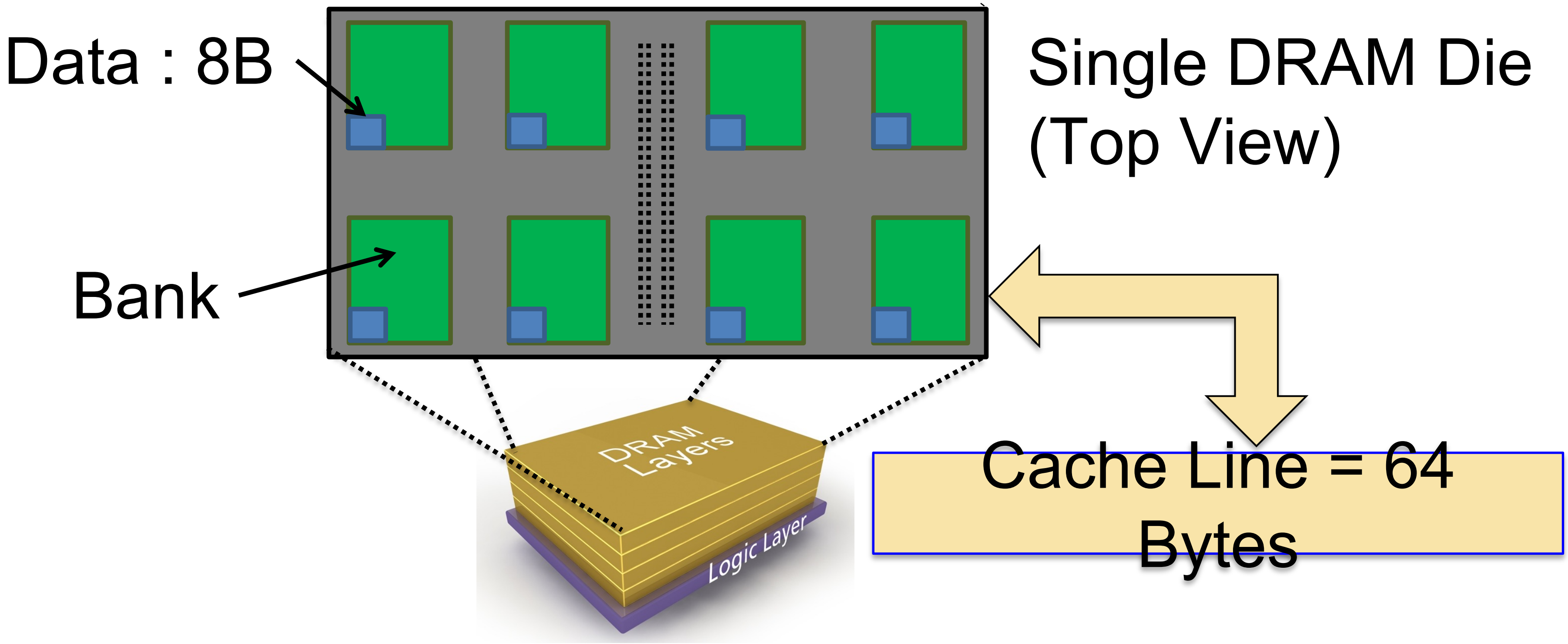

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Bank

Single DRAM Die
(Top View)

Cache Line = 64 Bytes

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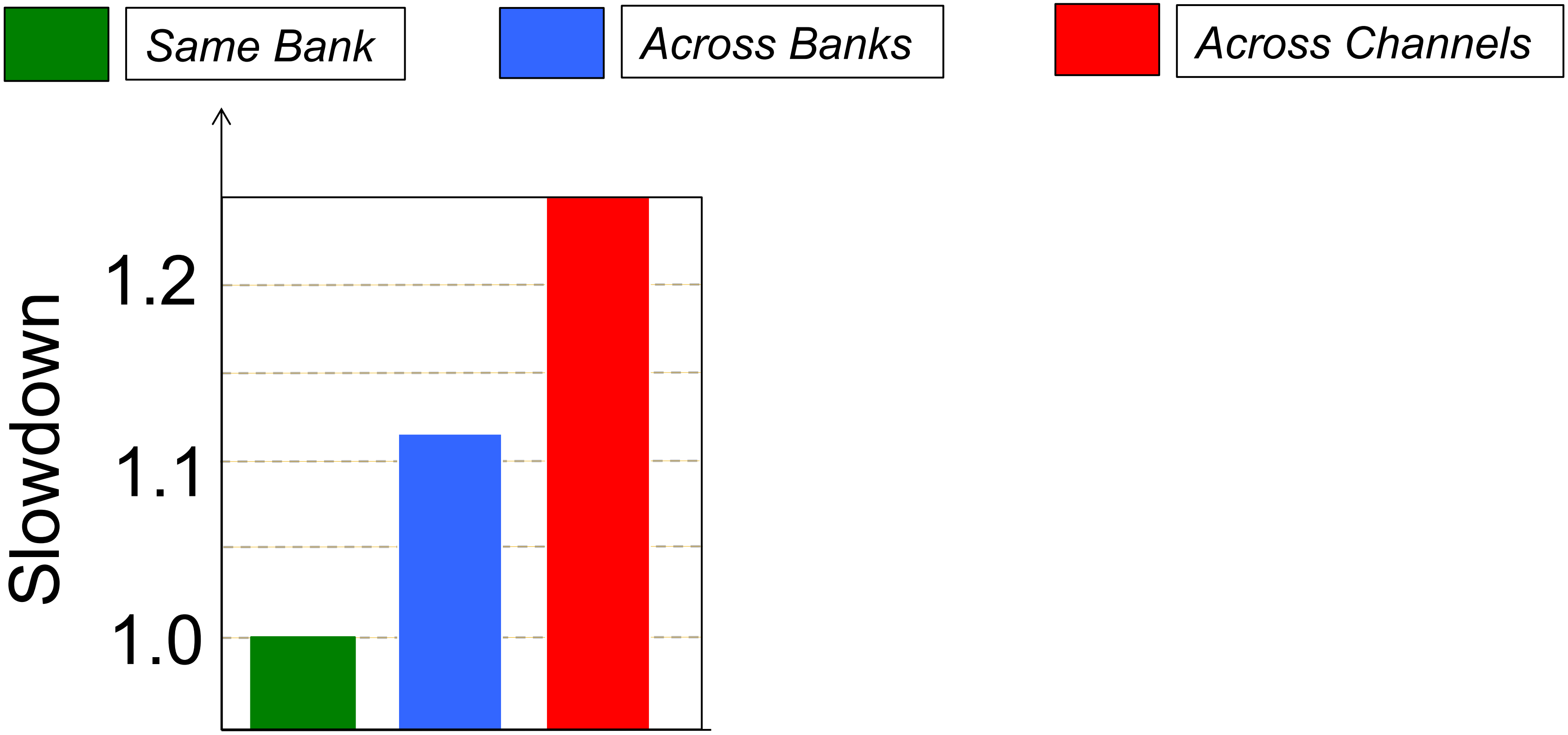
At least 8X↑ activation power, 8X↓ DRAM parallelism

COST OF STRIPING IN 3D DRAM



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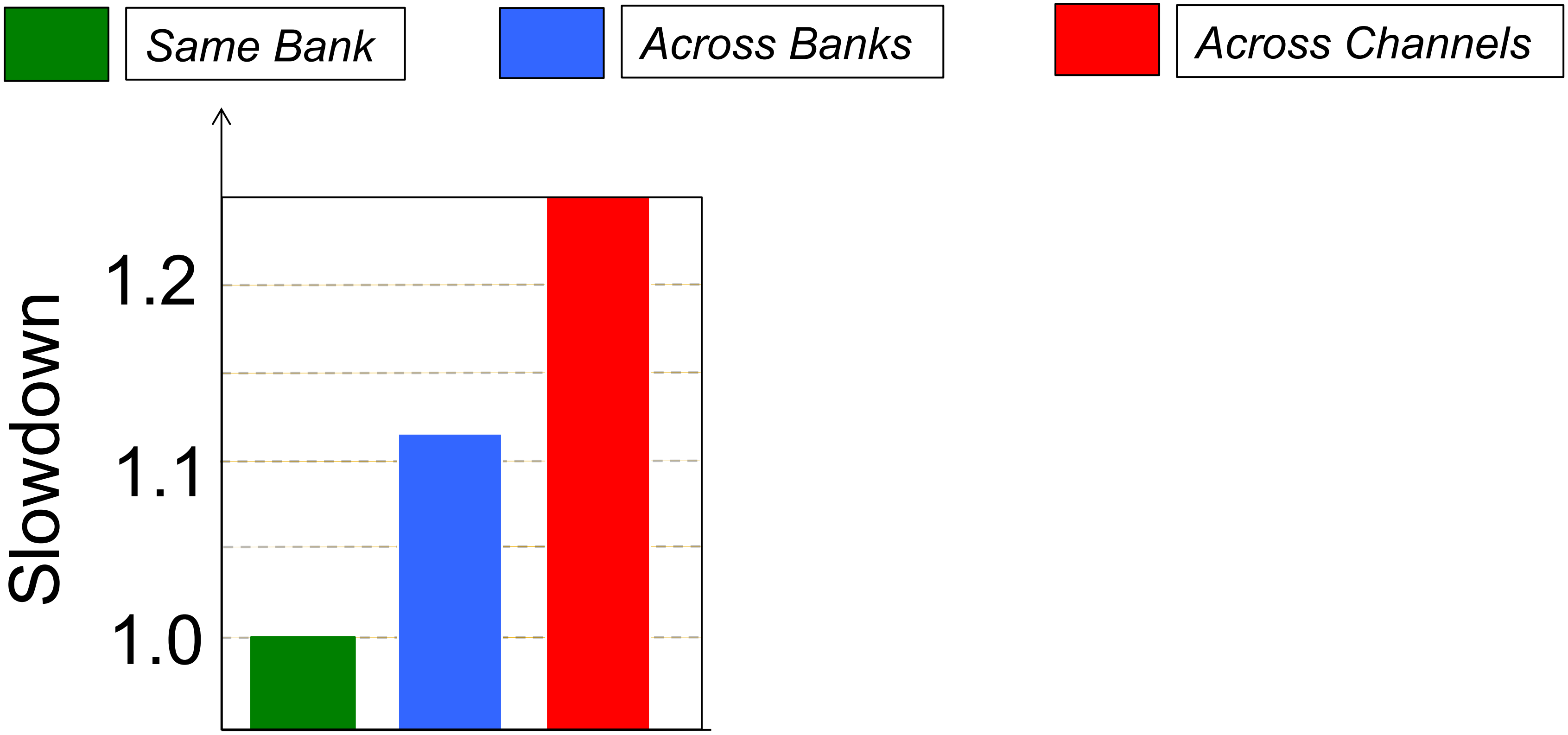

25% More Execution Time

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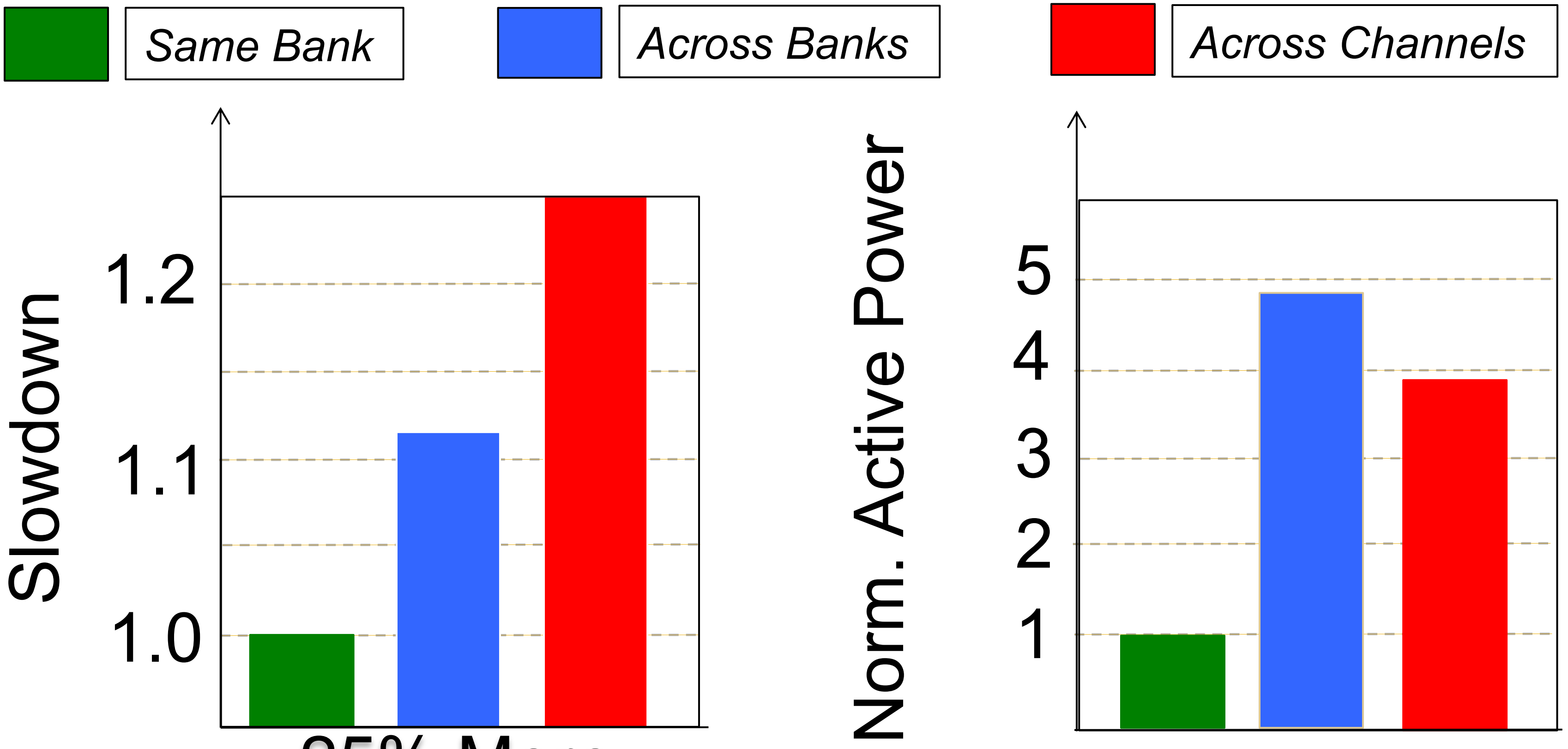

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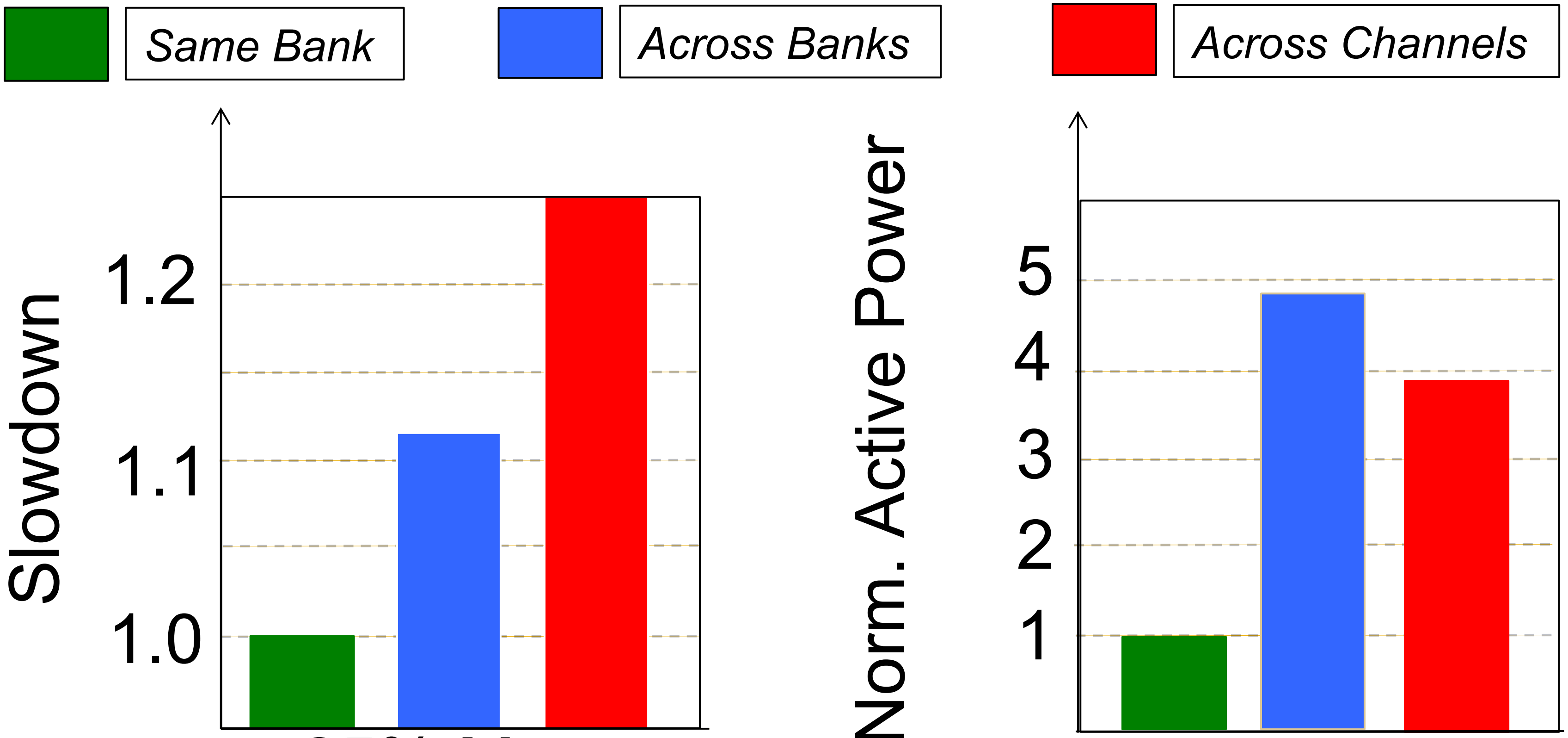

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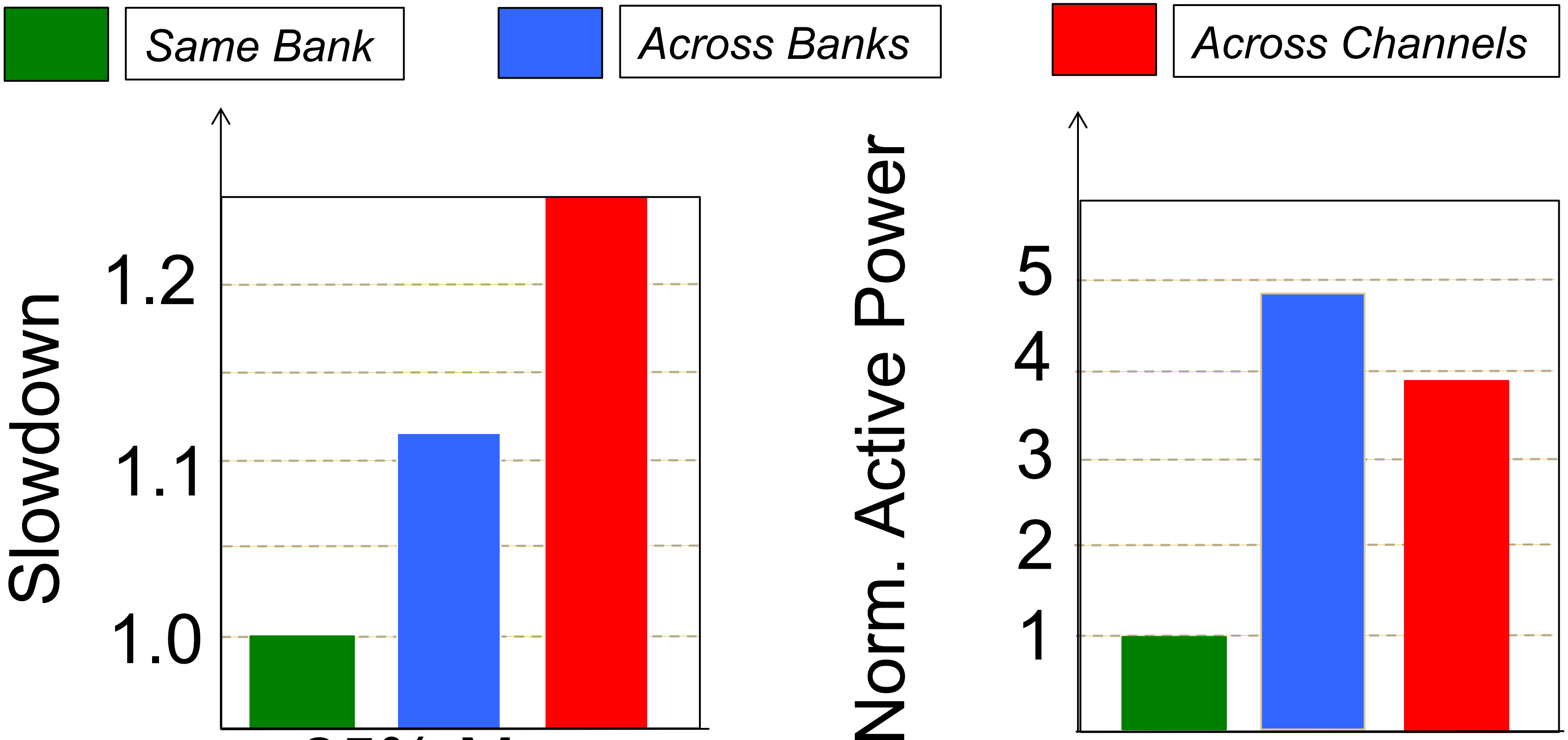


25% More Execution Time

4.8X More Activation Power

Striping data across banks/channels in 3D is costly

GOAL

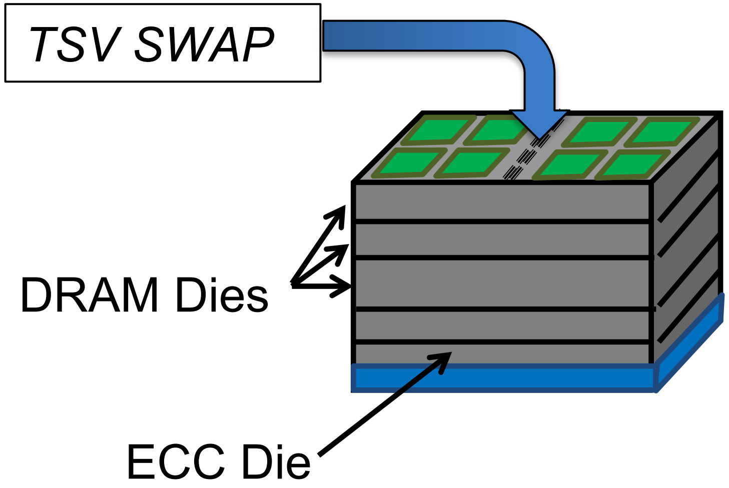
Develop Efficient Solutions to Mitigate TSV and other Large Granularity Faults in Stacked Memory without striping data

OUTLINE

- Introduction and Background
- Citadel ⇦
- Scheme - 1 : TSV-SWAP
- Scheme - 2 : Three Dimensional Parity (3DP)
- Scheme - 3 : Dynamic Dual Grain Sparing (DDS)
- Summary

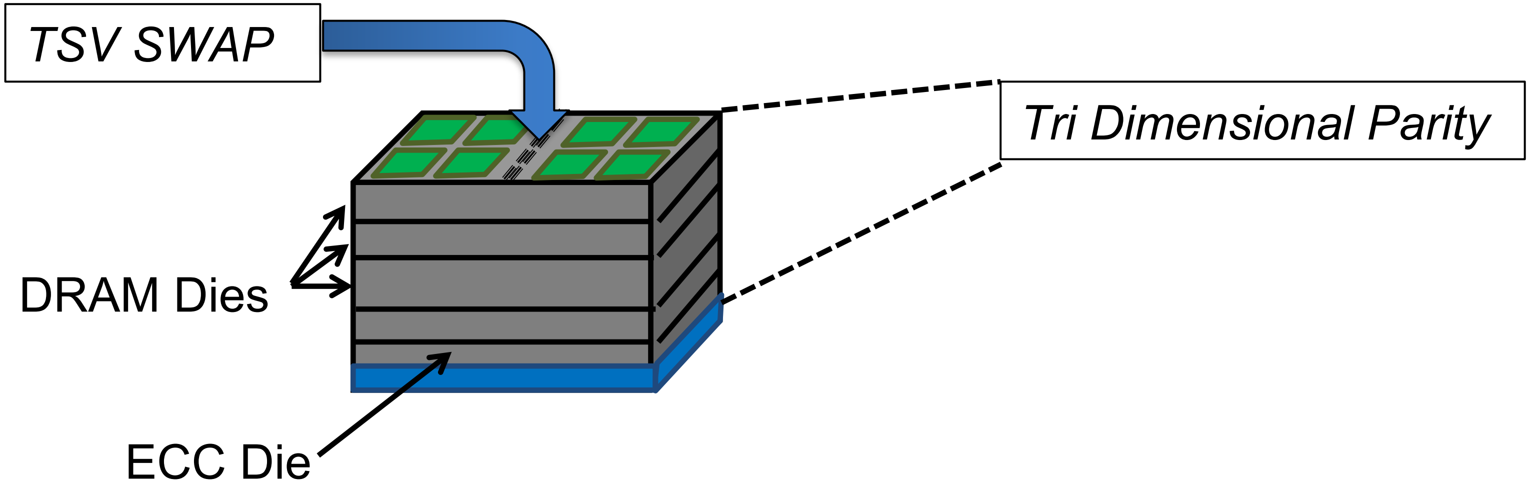
CITADEL: AN OVERVIEW

- Runtime TSV Sparing (TSV-SWAP)



CITADEL: AN OVERVIEW

- Runtime TSV Sparing (TSV-SWAP)
- RAID-5 across 3 dimensions (Tri dimensional parity)

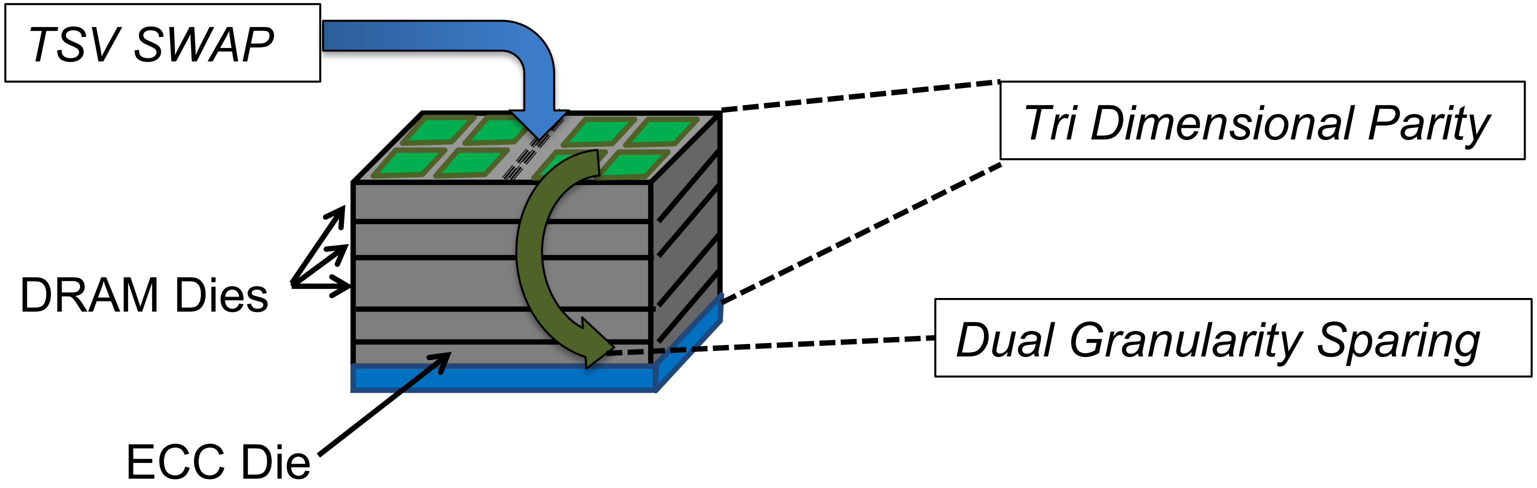


CITADEL: AN OVERVIEW

- Runtime TSV Sparing (TSV-SWAP)

•RAID-5 across 3 dimensions (Tri dimensional parity)

•Spare Faults Regions (Dual Granularity Sparing)



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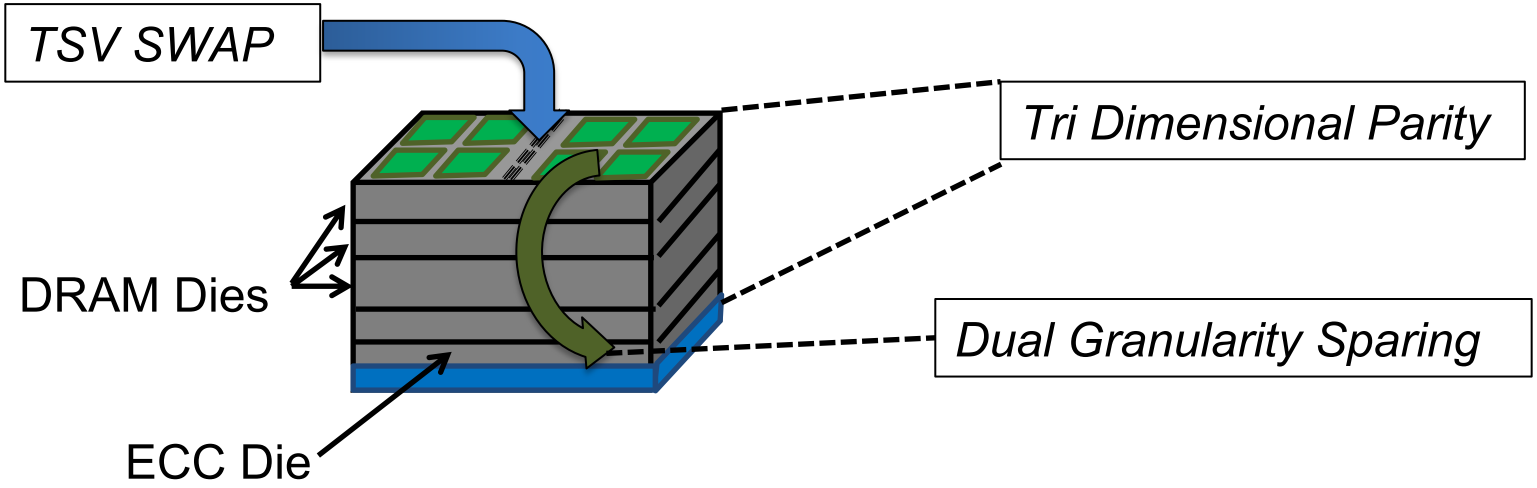

Enable robust stacked memory at very low overheads

OUTLINE

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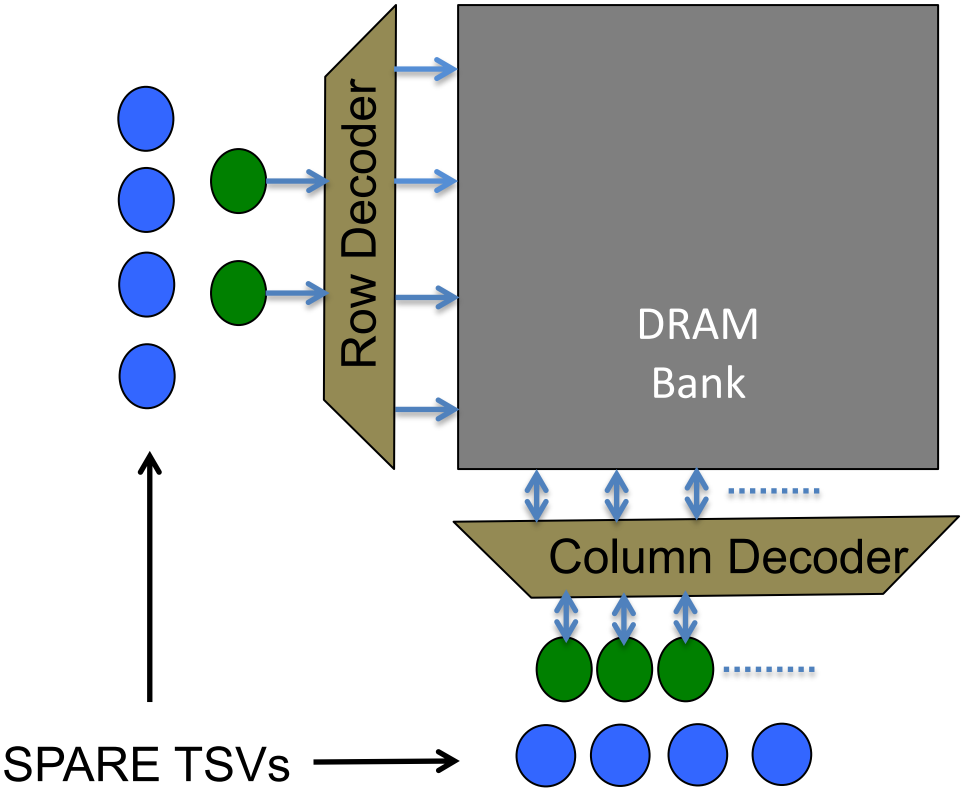
DESIGN-TIME TSV SPARING

Designers provision spares TSVs alongside

Data TSVs and Address TSVs



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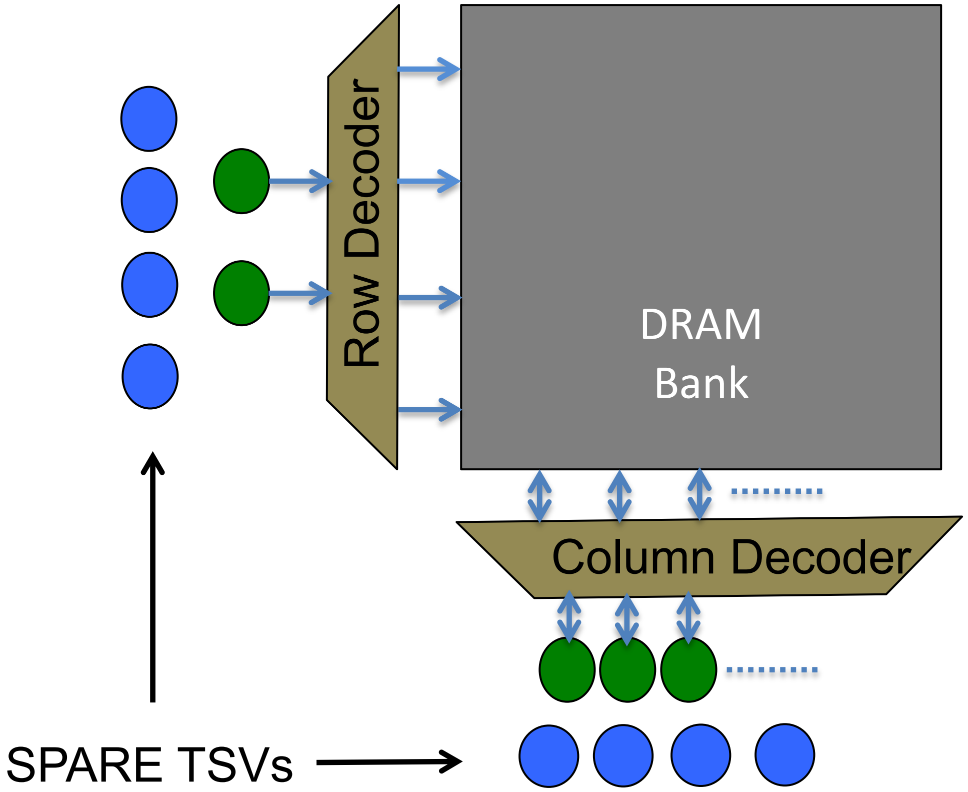
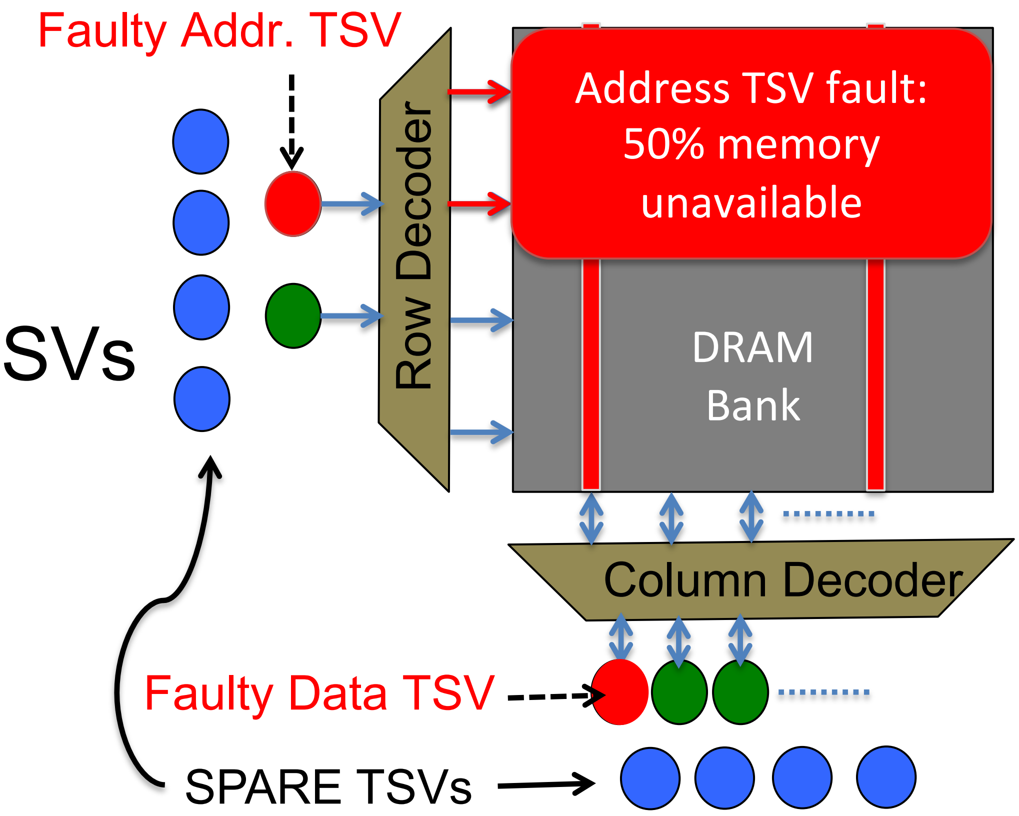


Additional Spare TSVs can replace faulty TSVs

DESIGN-TIME TSV SPARING: OPERATION

- Deactivate Broken TSVs



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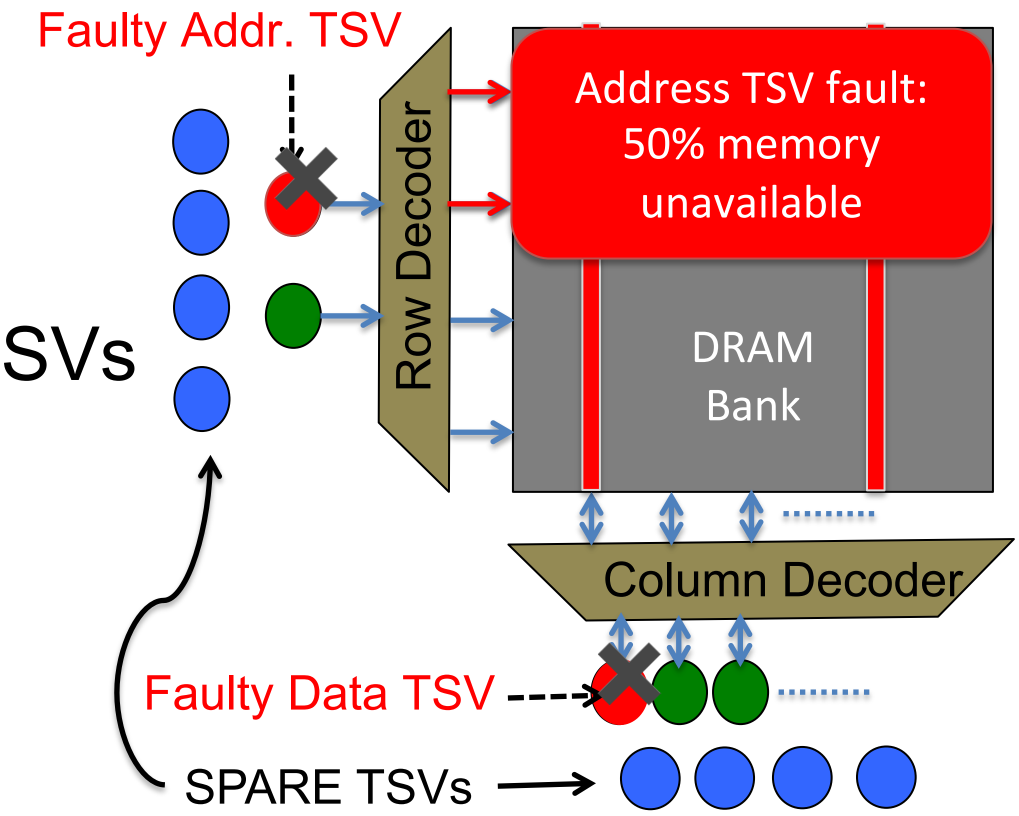

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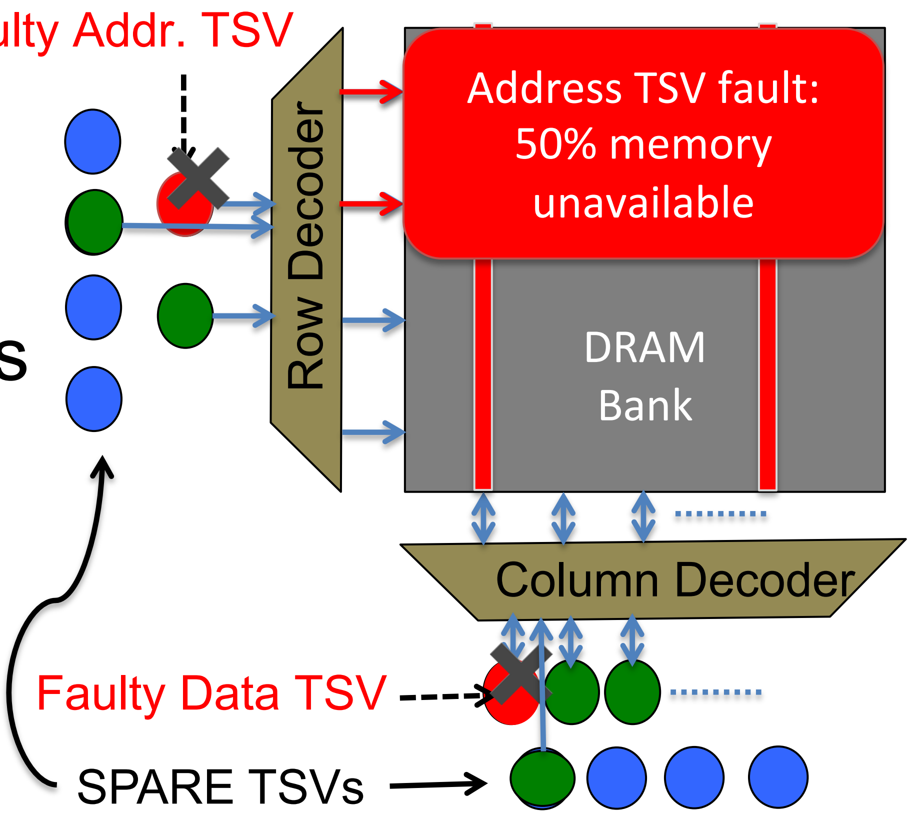
- Deactivate Broken TSVs
- Activate SPARE TSVs



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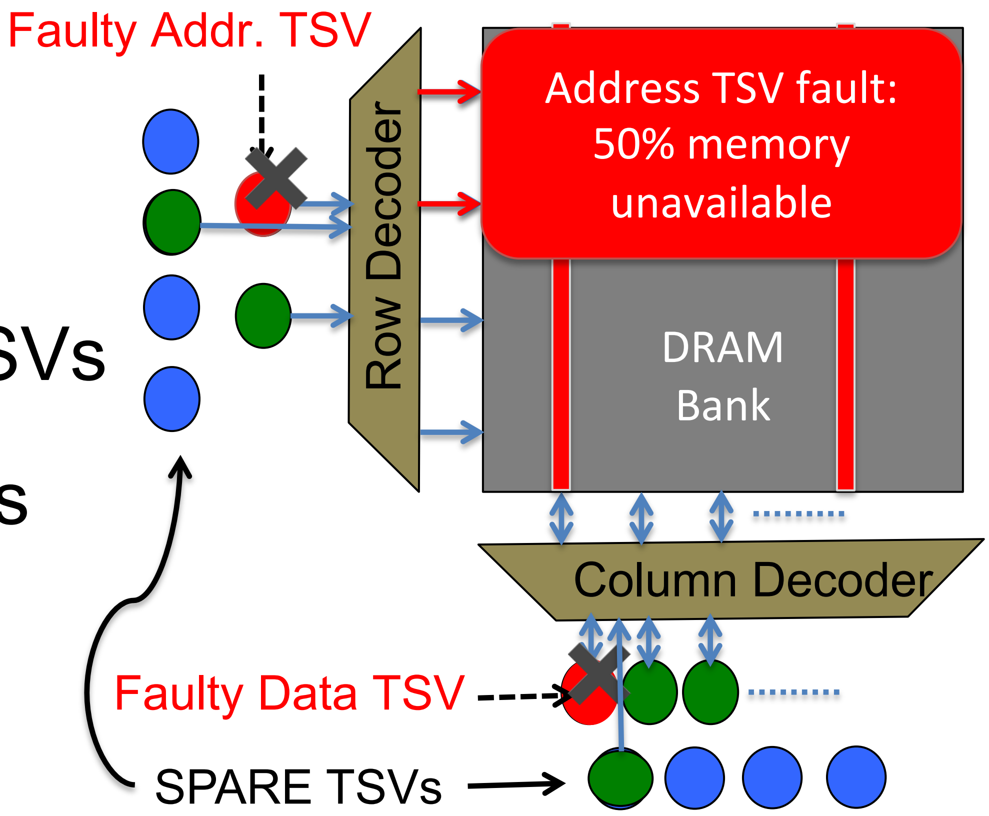


Deactivation of Faulty TSVs and Activation of Spare TSVs is performed at design time

DESIGN-TIME TSV SPARING: PROBLEMS

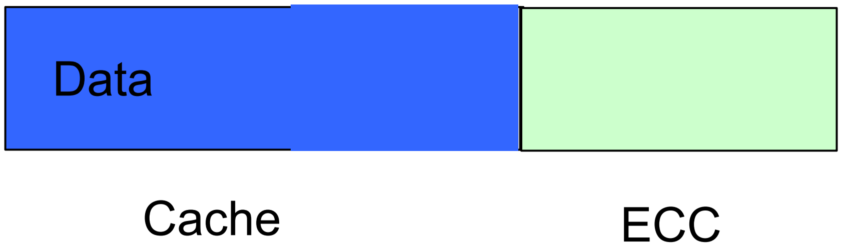
Additional TSVs are required for TSV Sparing

and

What happens if TSVs turn faulty at runtime?

TSV-SWAP: RUNTIME TSV SPARING

STEP-1: CREATE STANDBY TSVs



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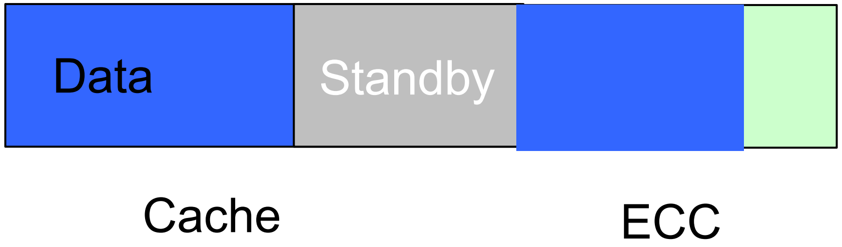

- Few Data TSVs as Standby TSVs
- Replicate Standby Data in ECC

TSV-SWAP: RUNTIME TSV SPARING

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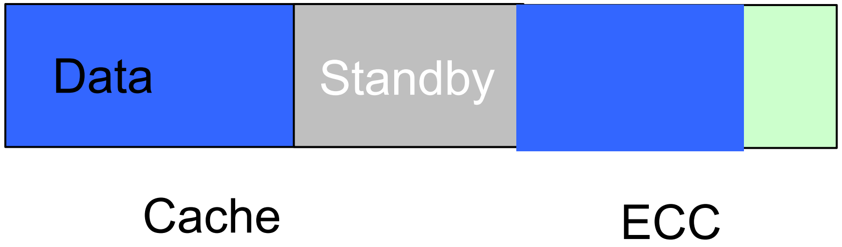
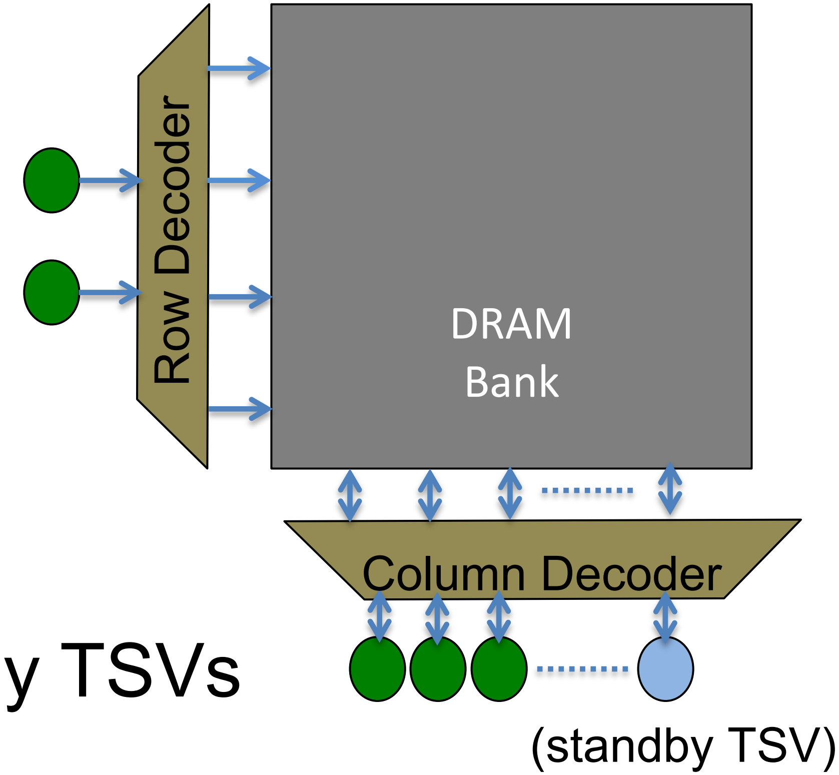




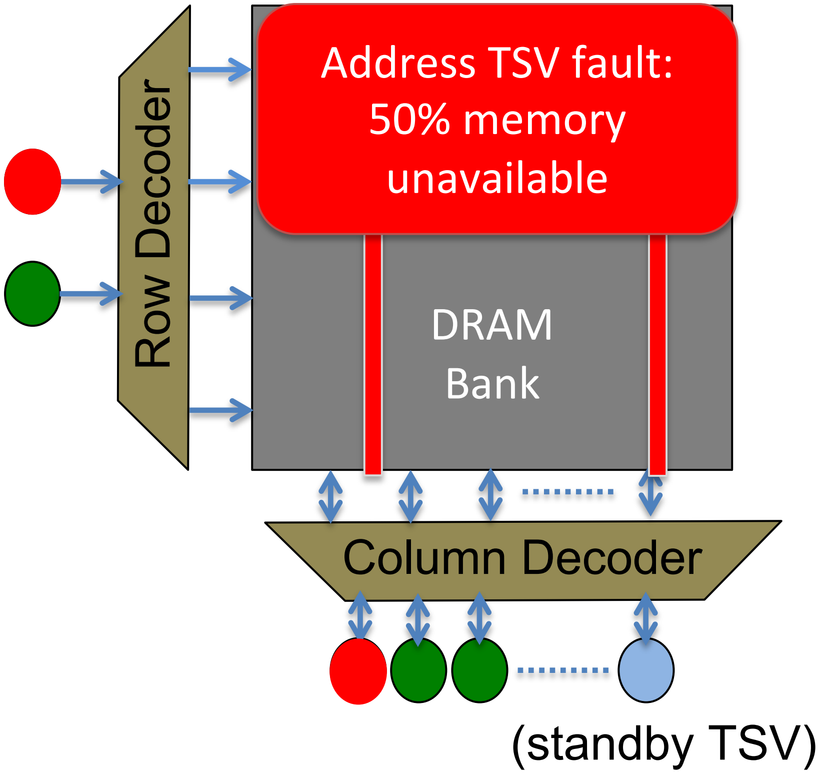
- Few Data TSVs as Standby TSVs
- Replicate Standby Data in ECC

Data TSVs reused as Standby TSVs

TSV-SWAP: RUNTIME TSV SPARING

STEP-2: DETECTING FAULTY TSVs

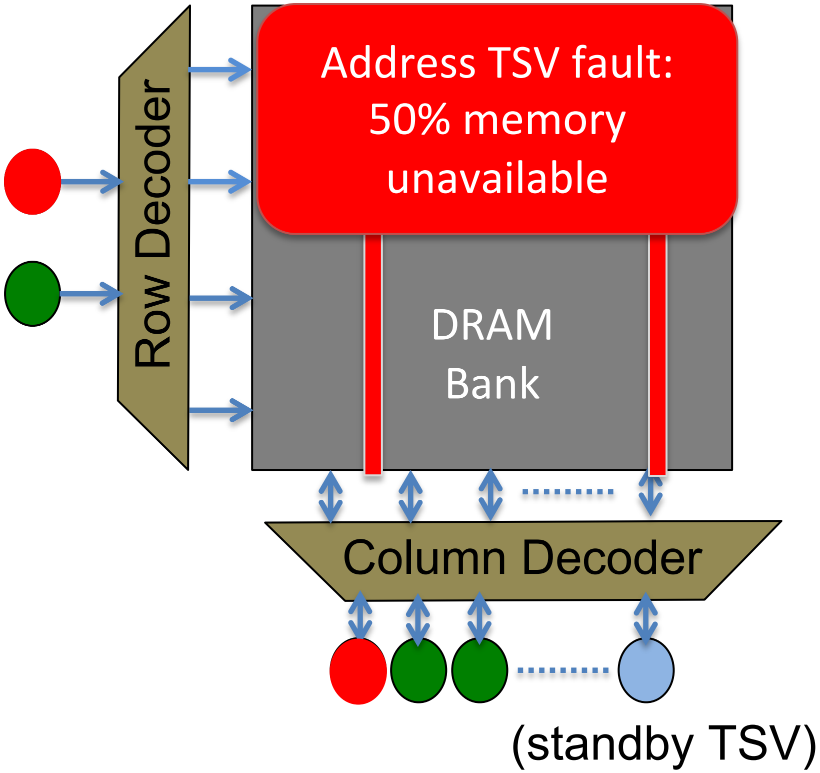
- CRC-32 ➡ address + data



TSV-SWAP: RUNTIME TSV SPARING

STEP-2: DETECTING FAULTY TSVs

- CRC-32 ➡ address + data
- BIST diagnoses faulty TSVs



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- CRC-32 ➡ address + data
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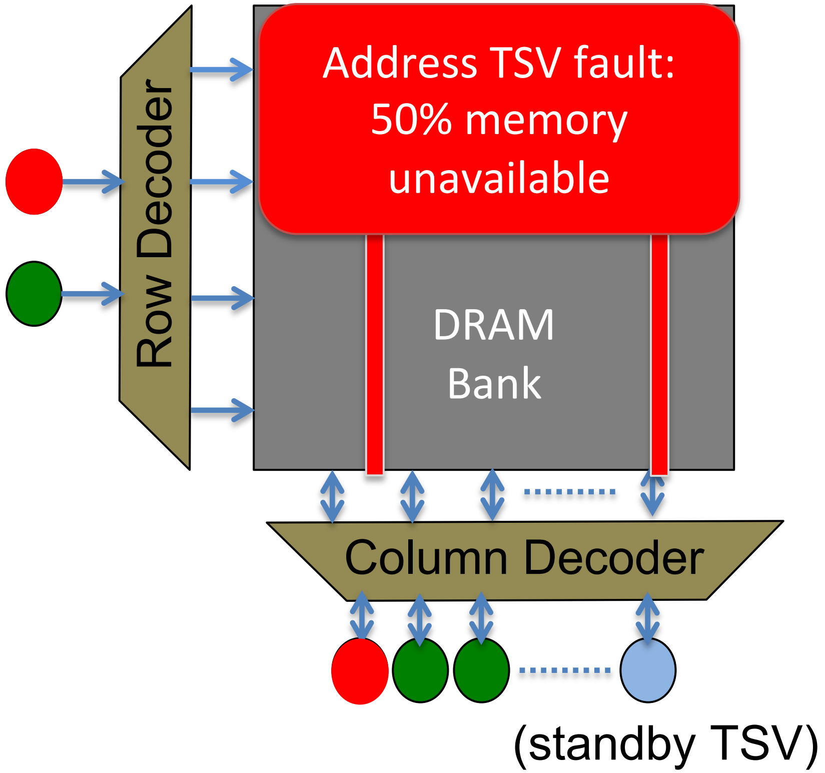
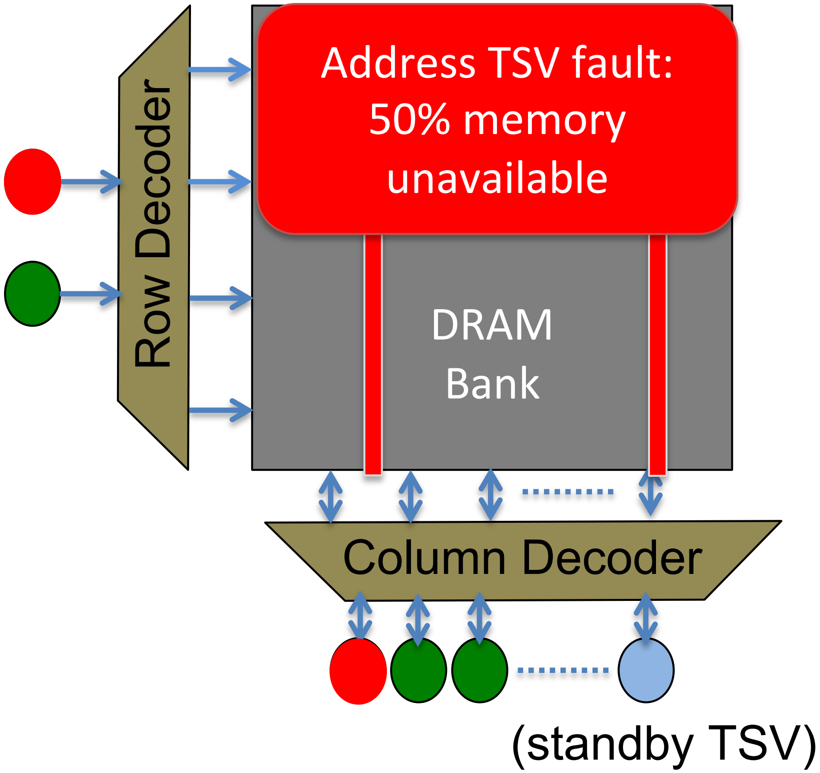


Data vs Address TSV Faults Using CRC-32+BIST

TSV-SWAP: RUNTIME TSV SPARING

STEP-3: REDIRECTING FAULTY TSVs

Swap Faulty TSVs with Standby TSVs at runtime



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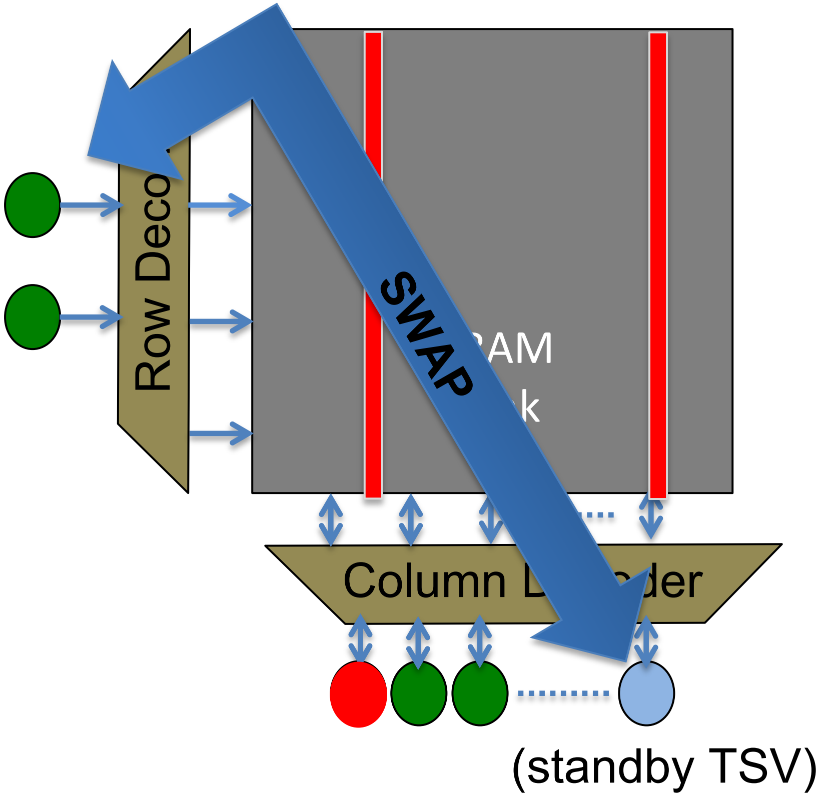

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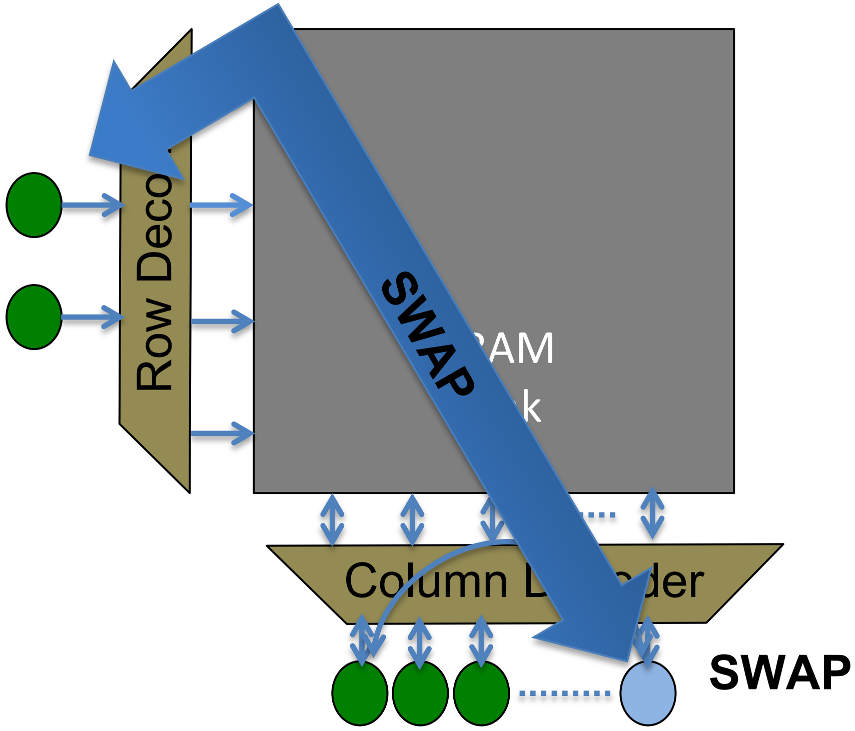

(standby TSV)

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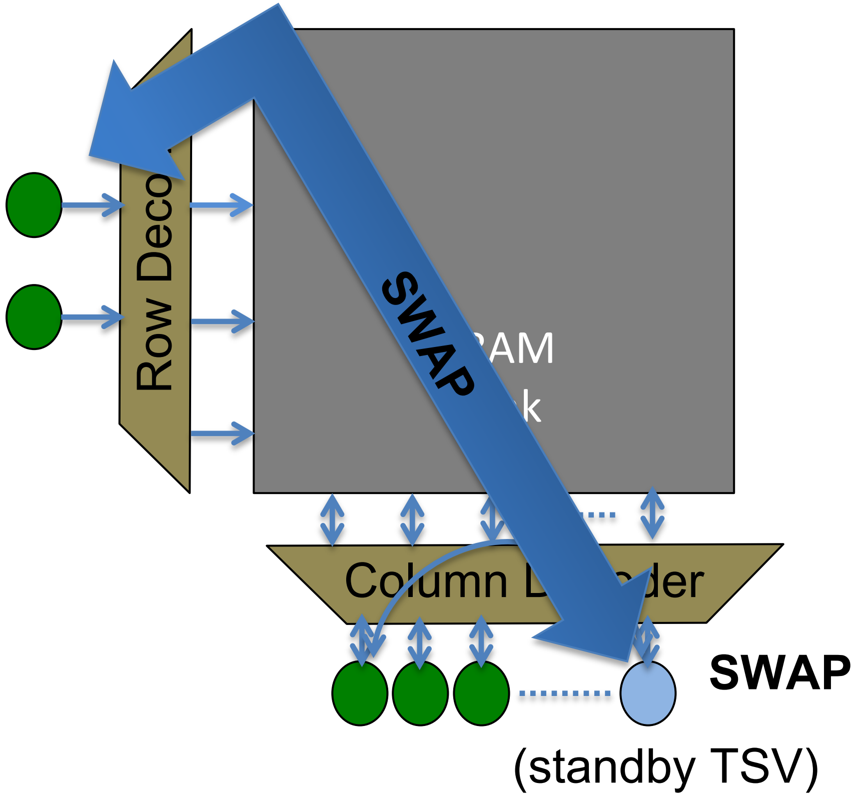
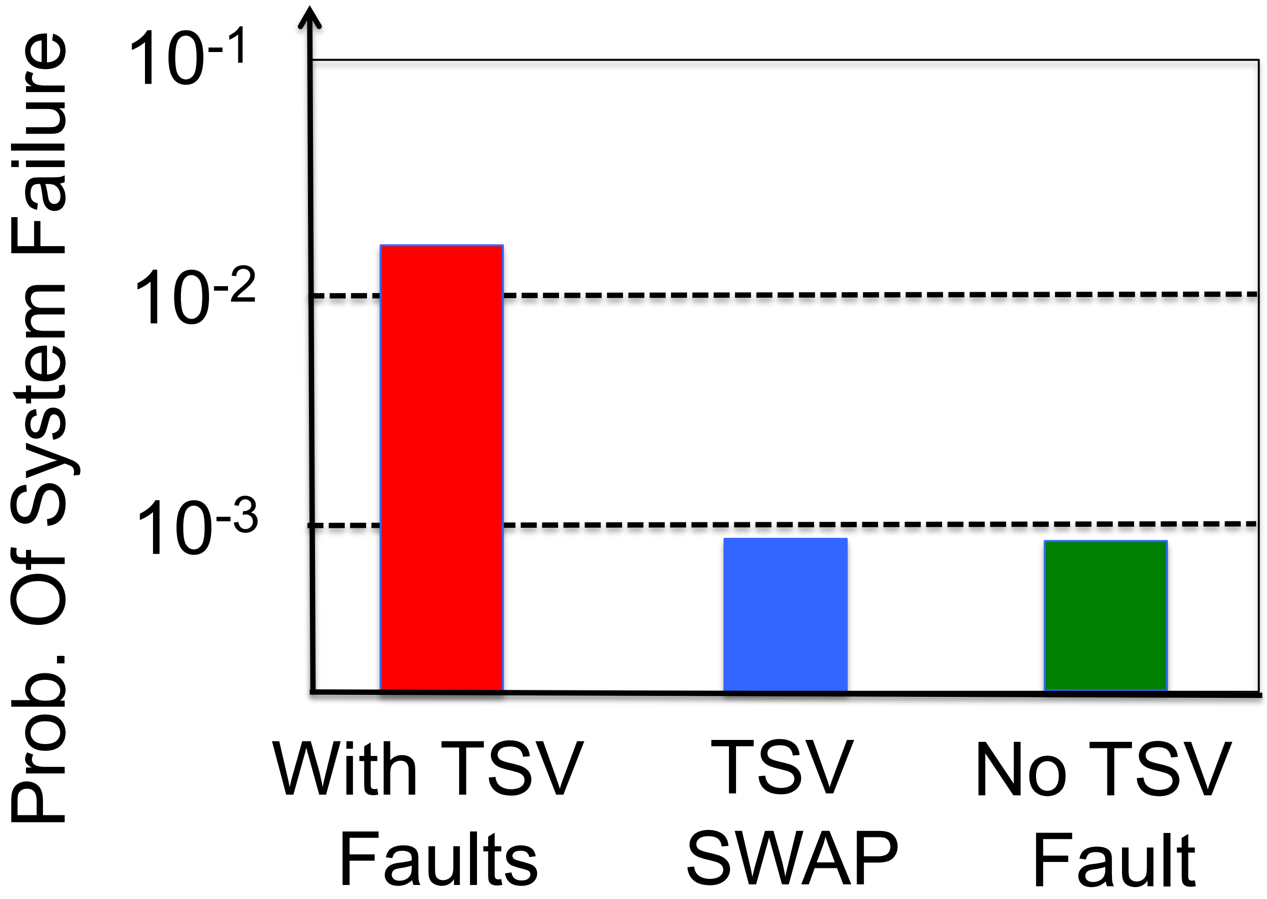


TSV-SWAP is a runtime technique that does not rely on additional spare TSVs

EFFECTIVENESS OF TSV-SWAP



Rate: One TSV Fault Every 7 years

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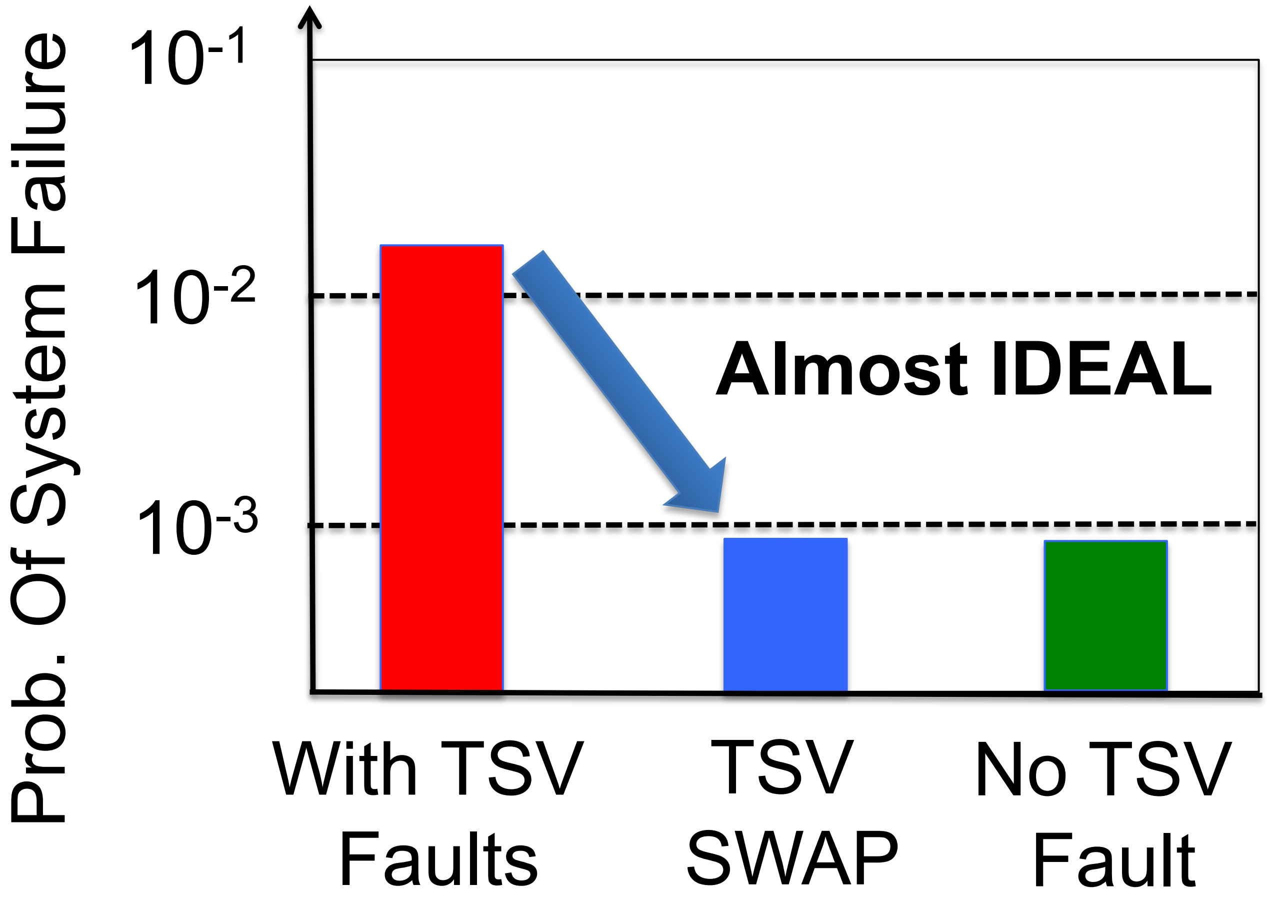

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TSV-SWAP is Effective at Tolerating TSV Faults

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- Use RAID-5 like scheme over three dimensions

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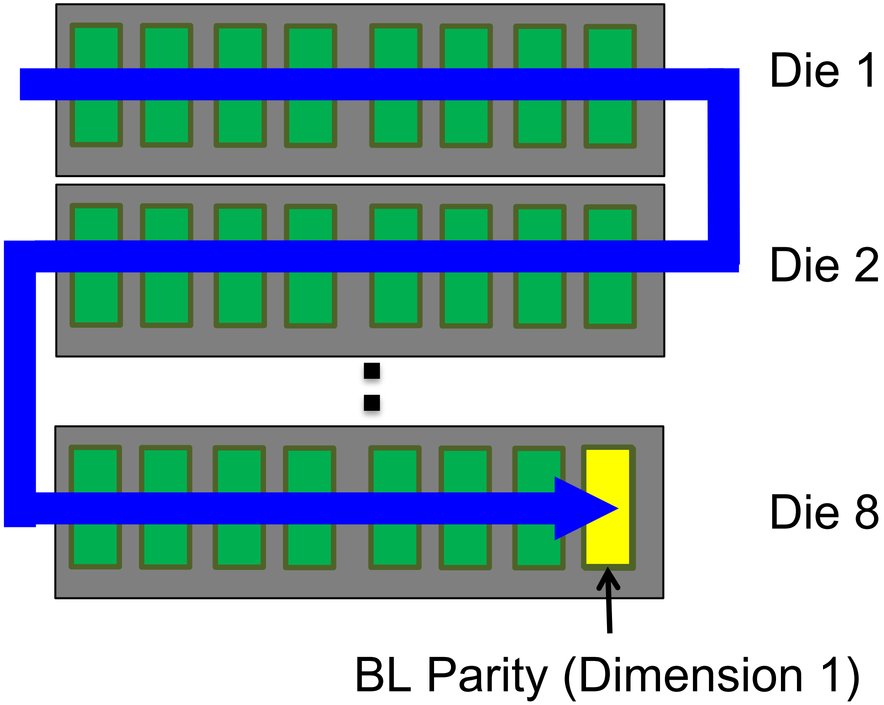

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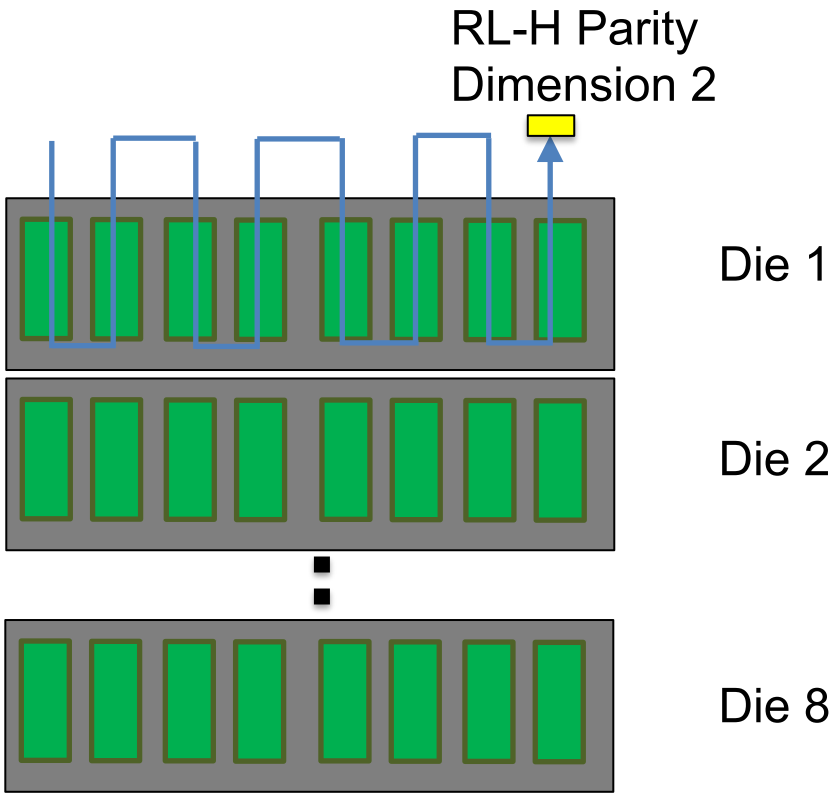

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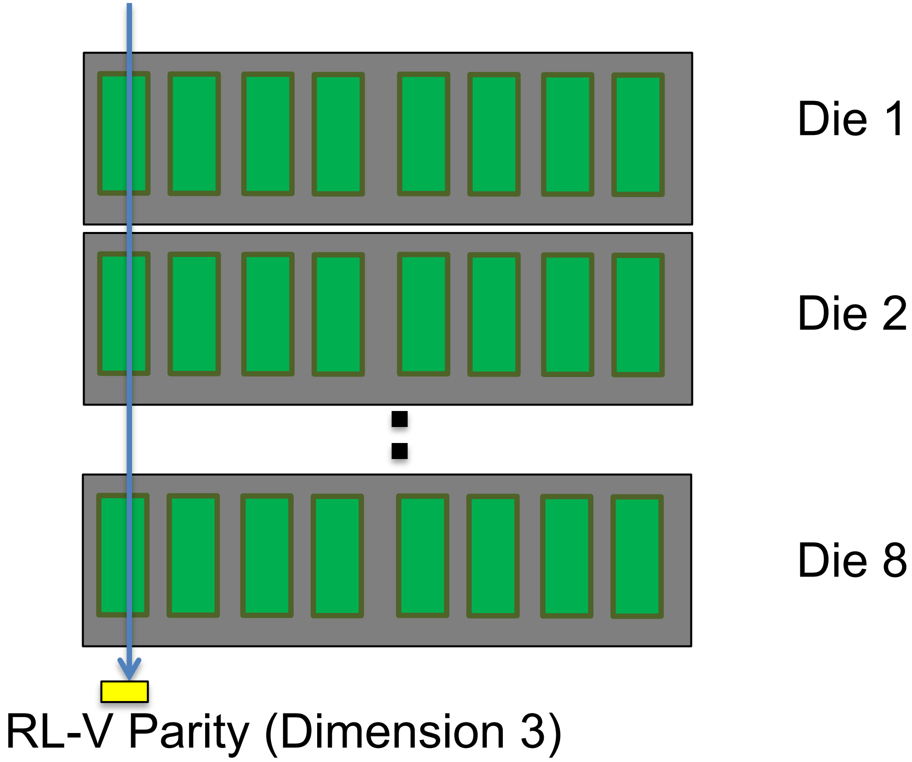
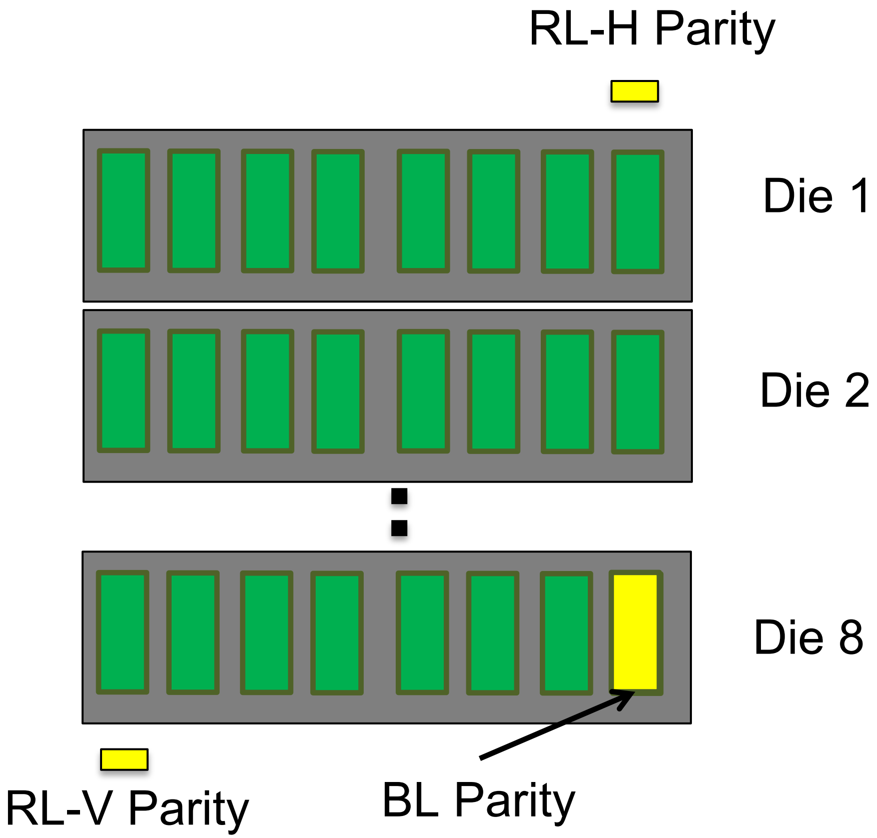


Three Dimensions Help In Multi-Fault Handling

3DP: DATA CORRECTION

If Fault → Compute Parity and Correct



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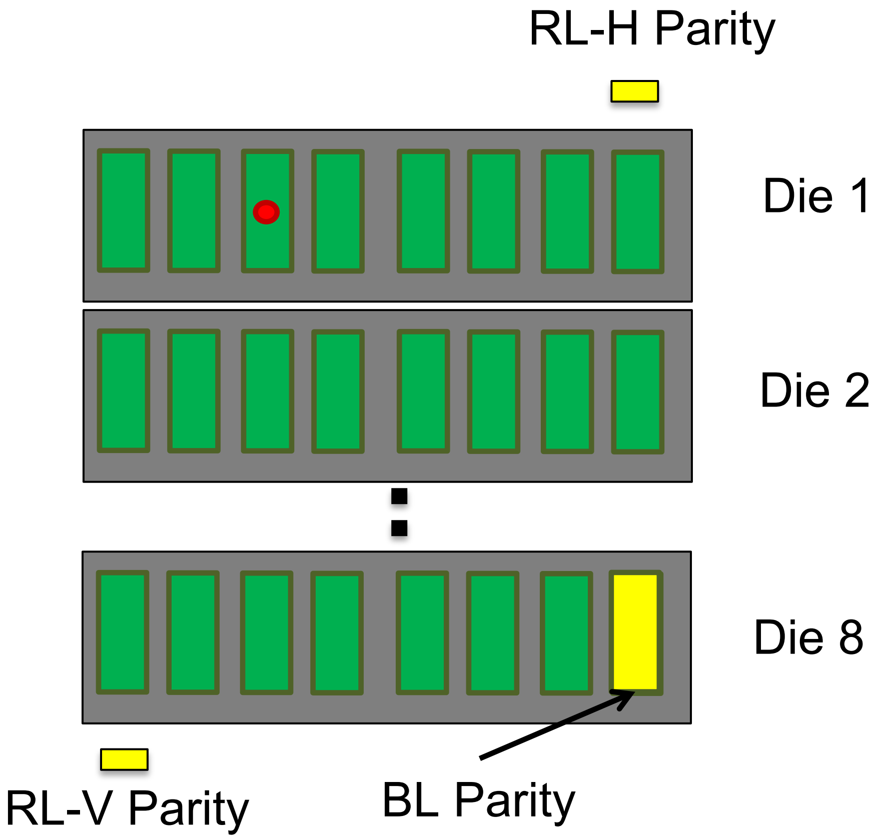

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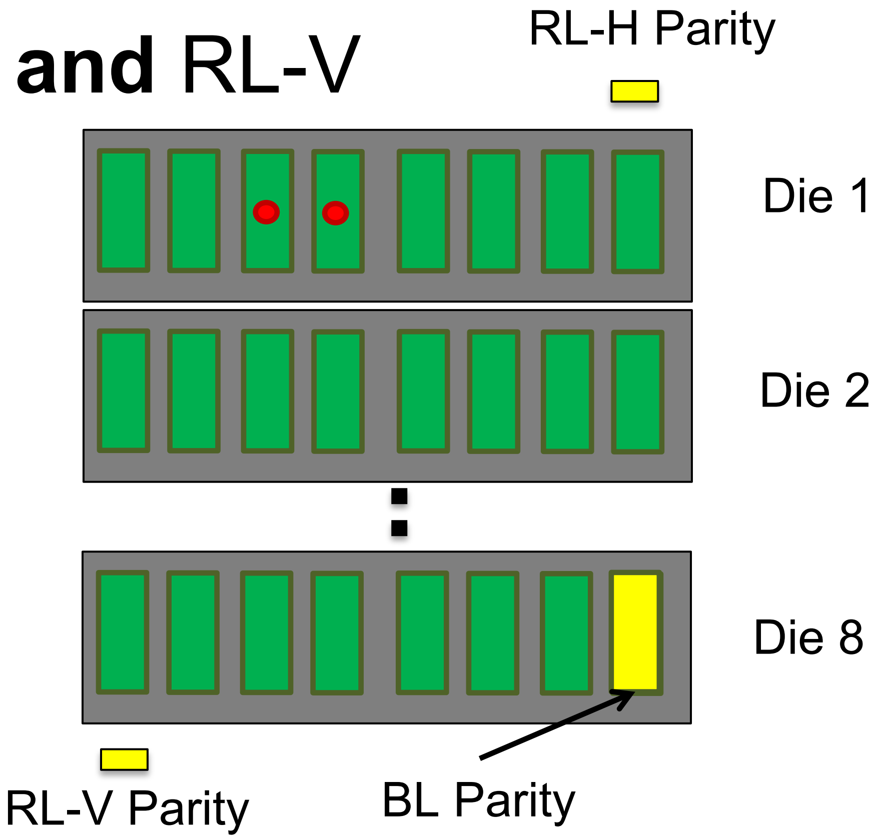

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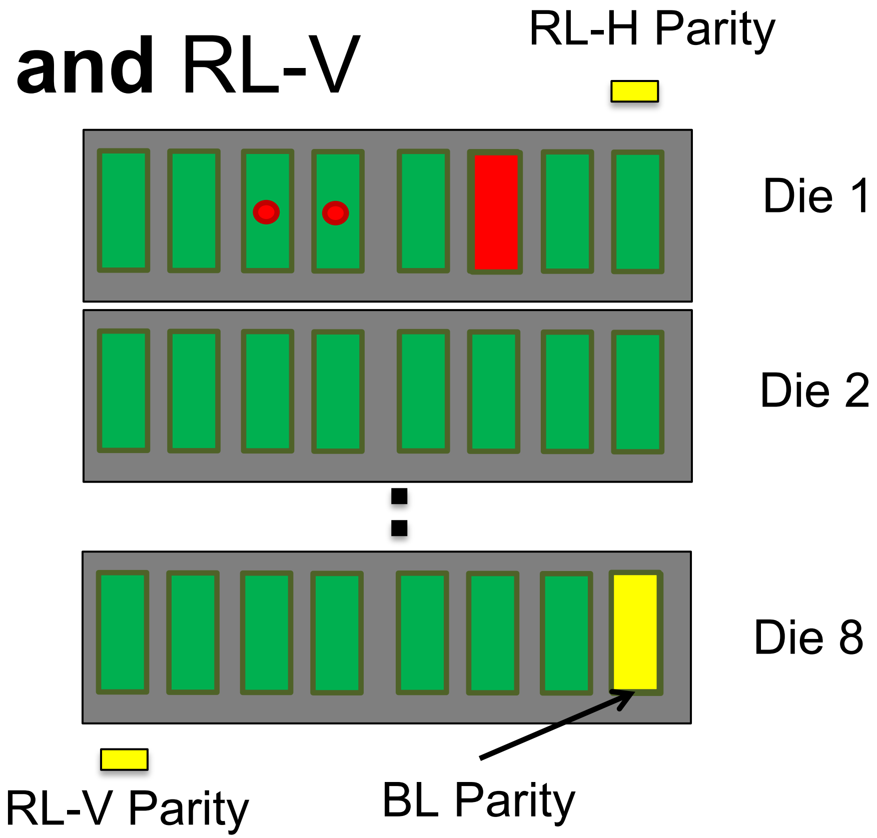

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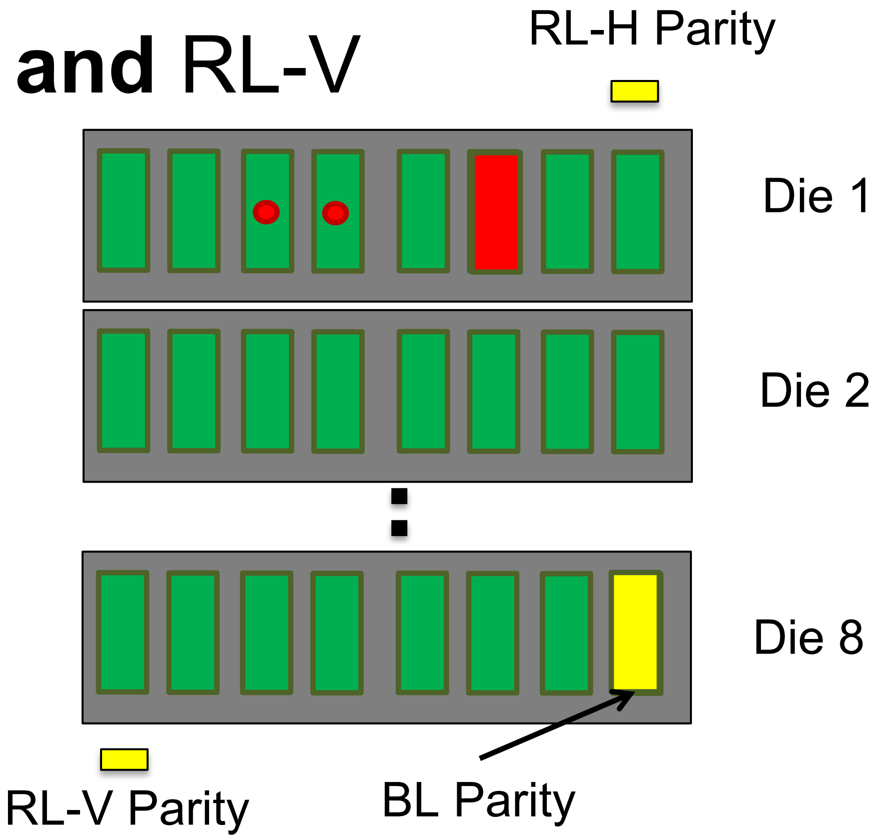

Multiple Multi-granularity Faults Are Corrected At Runtime

OVERHEADS IN UPDATING PARITY

- RL-H and RL-V Parity just 32 KB → stored in SRAM
- BL Parity is 128 MB → stored in DRAM

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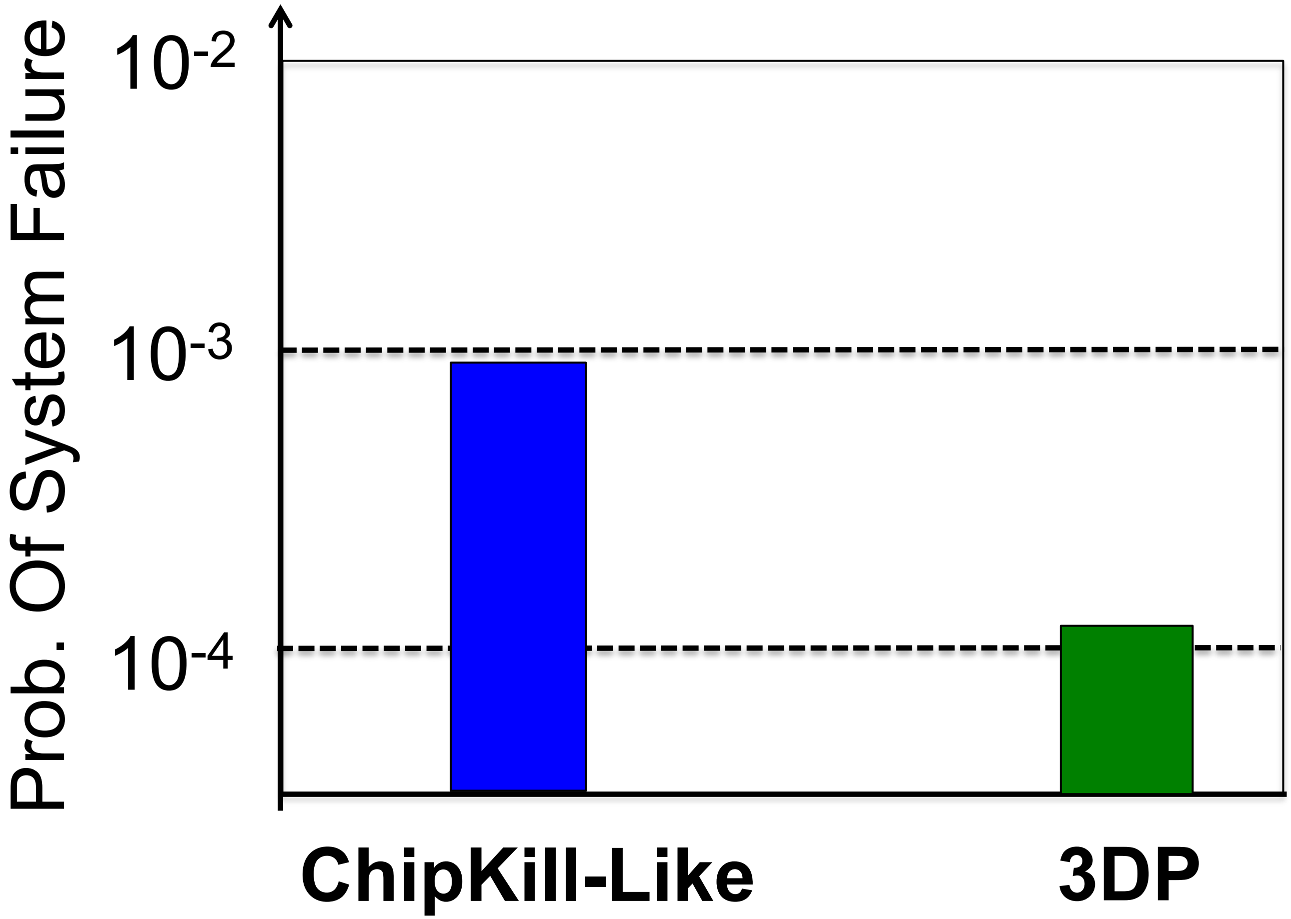
Demand Caching of BL Parity Has 85% Hit Rate And Mitigates Performance Overheads

EFFECTIVENESS OF 3DP



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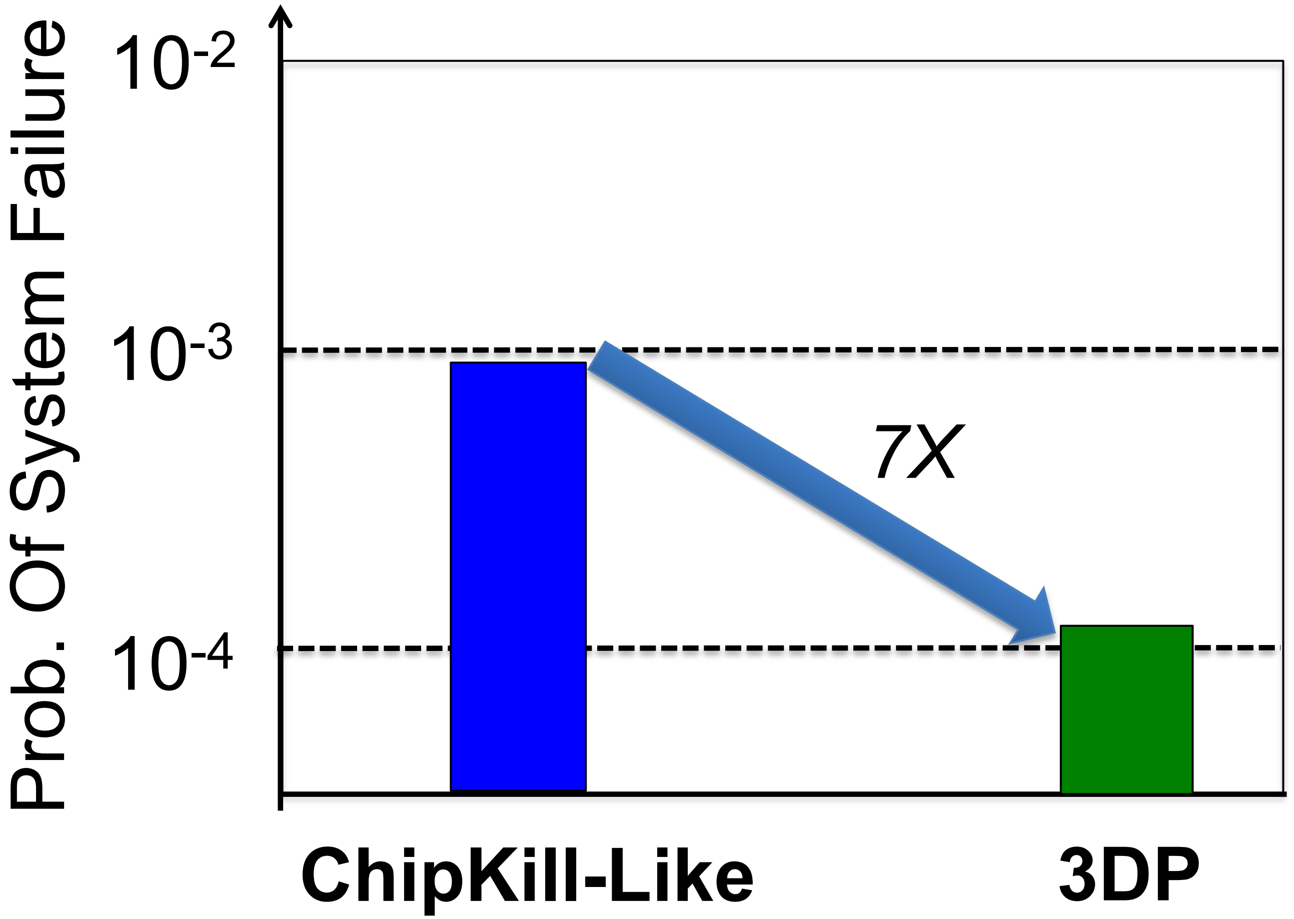

3DP is 7X Stronger Than A ChipKill-Like Scheme

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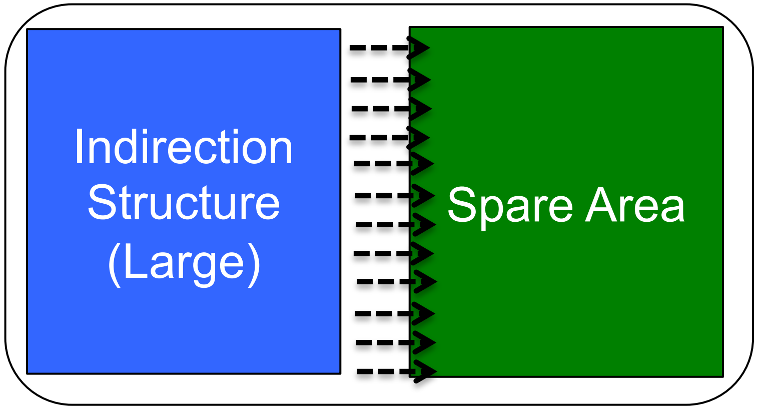
Sparing Mitigates Performance Overheads and Enhances Reliability

TRACKING STRUCTURES IN SPARING

- Row Level Tracking
  - Large Indirection Structure
  - Sparing Area Used Efficiently



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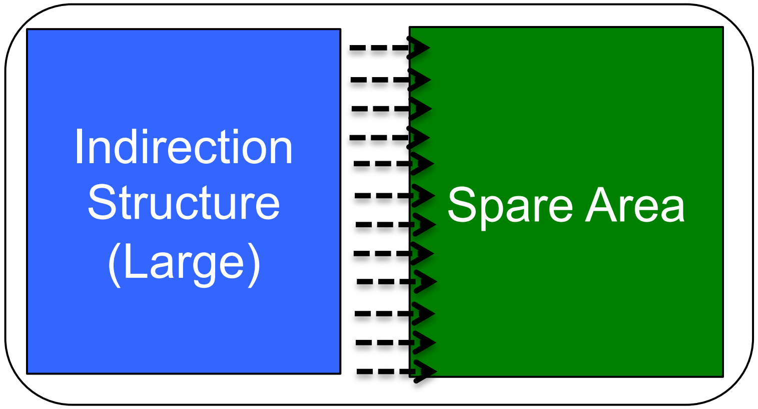

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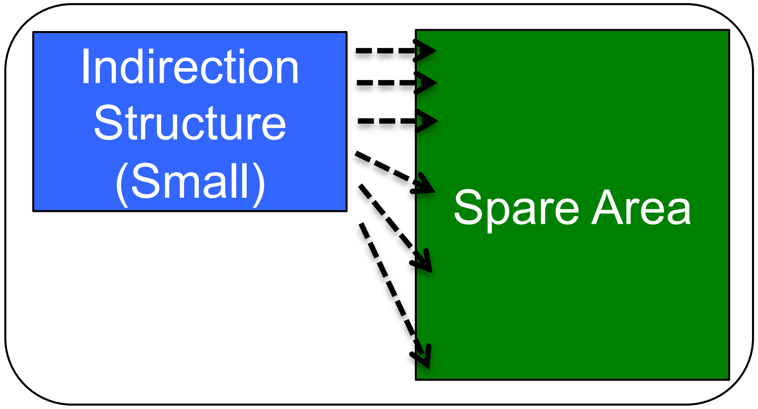

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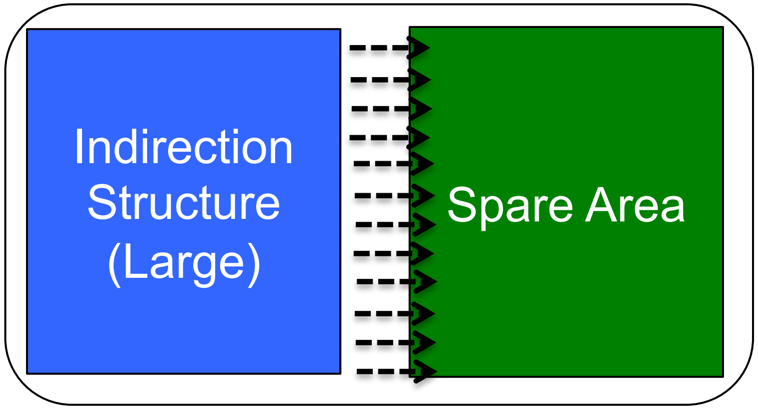

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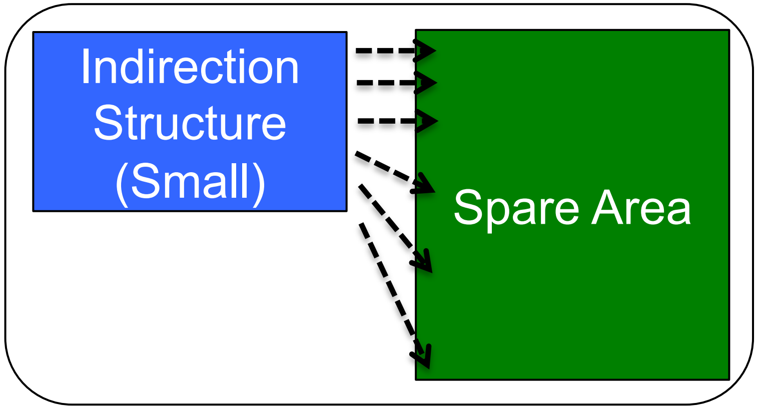
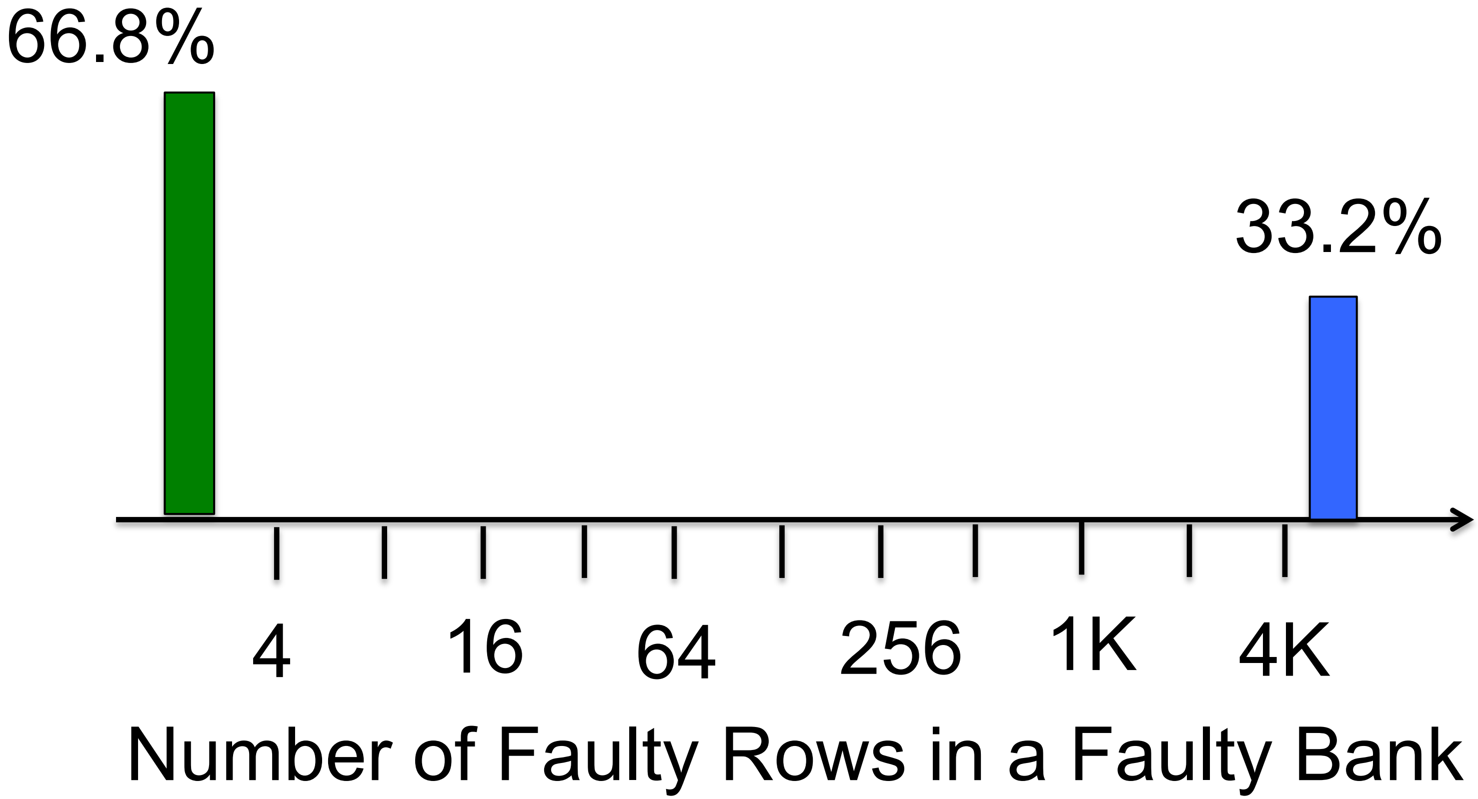


Ideally We Need Small Indirection Structures Which Use Spare Area Efficiently

BIMODAL FAILURES

- **Observation** : Either < 4 or > 4000 row failures



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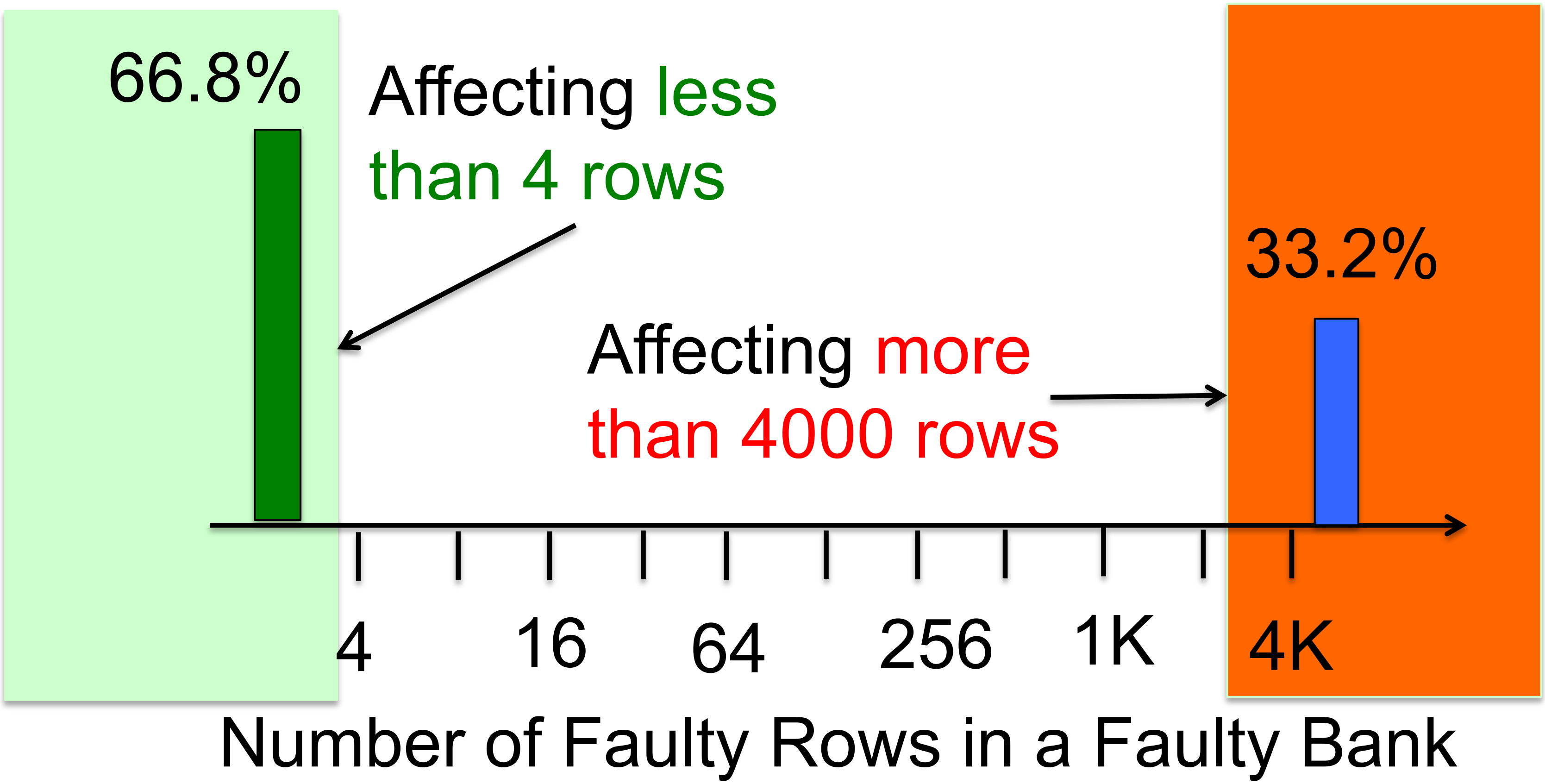

Affecting less than 4 rows

Affecting more than 4000 rows

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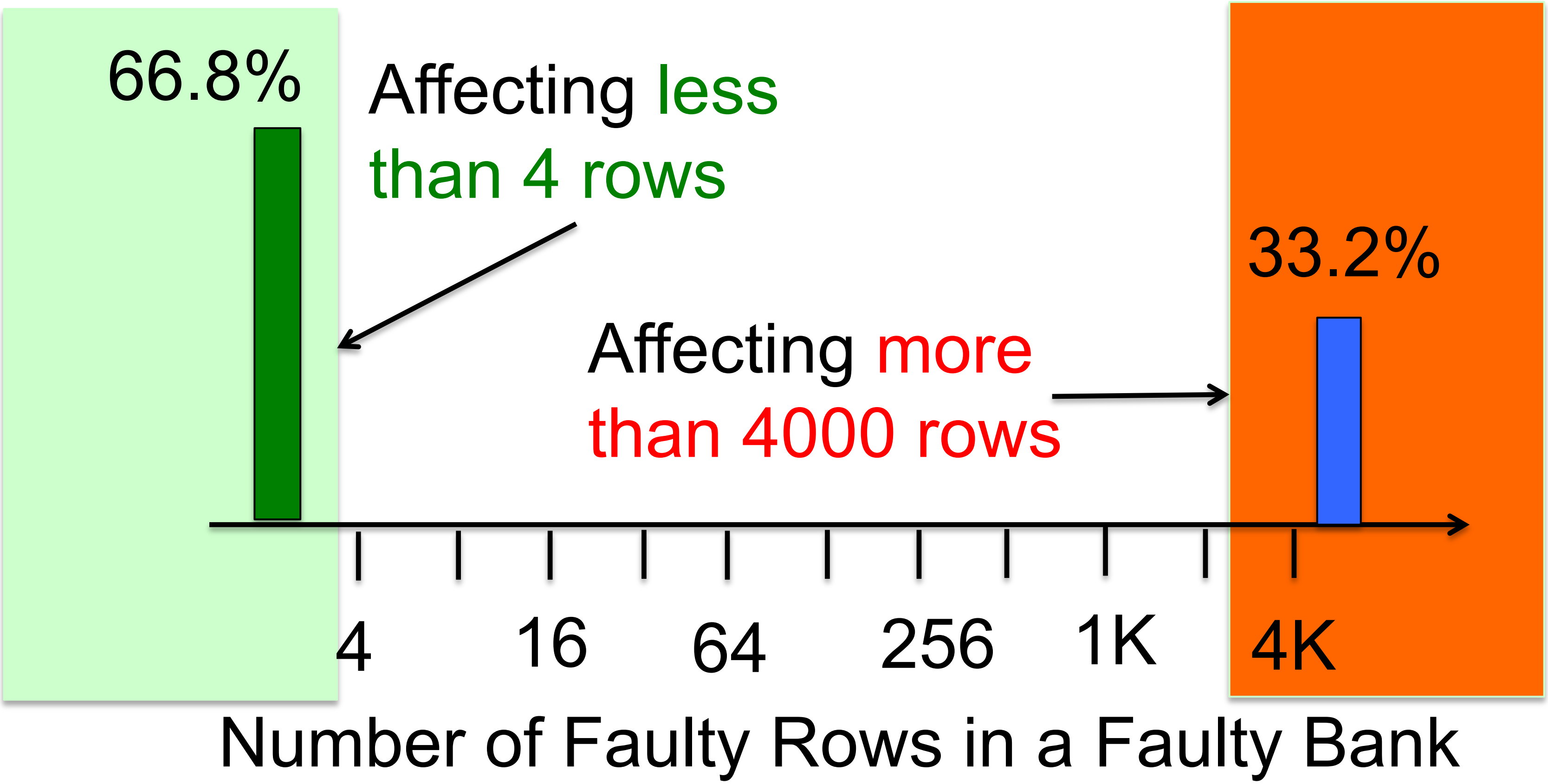
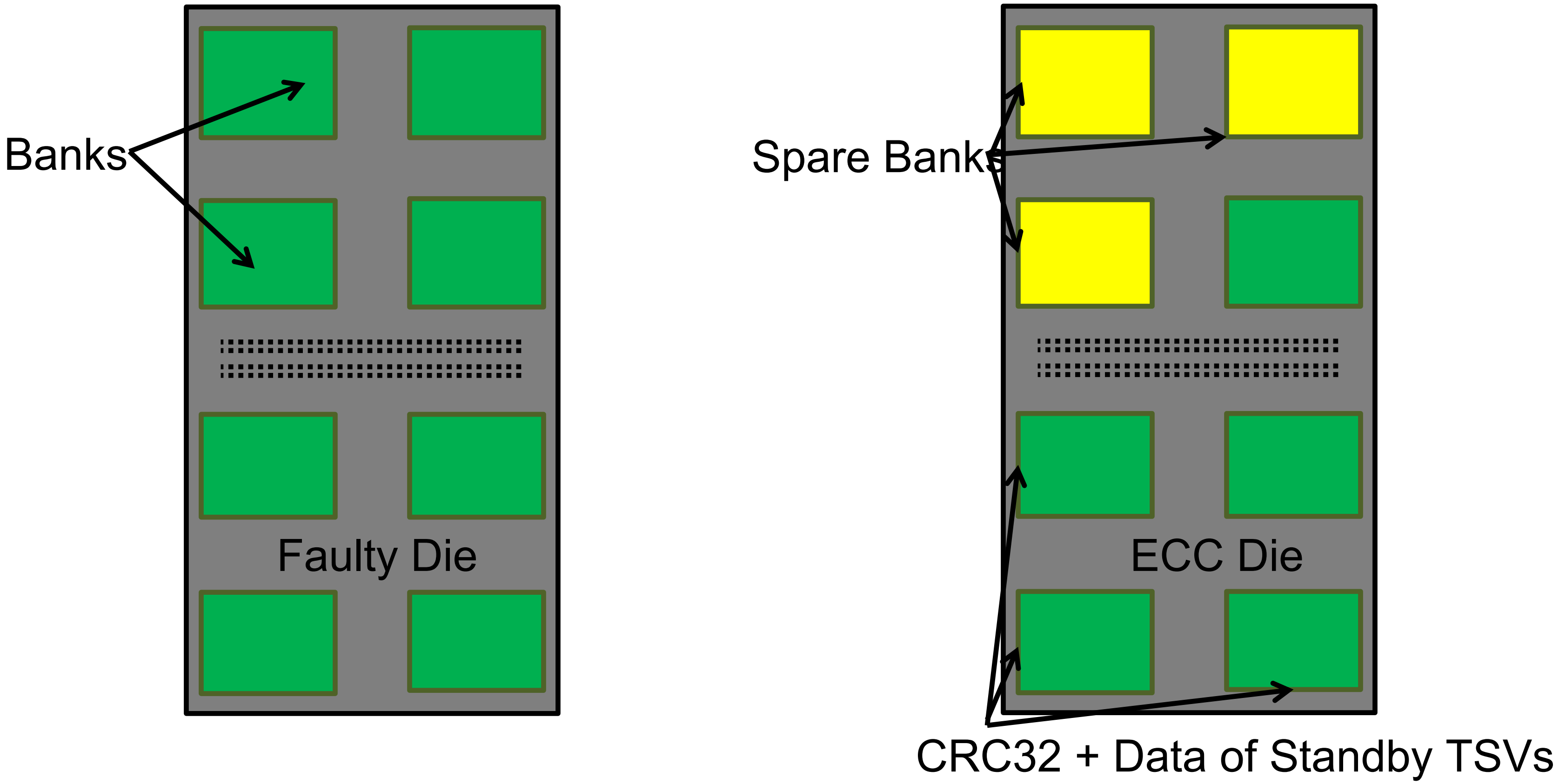


Spare Faulty Regions At Two Granularities

DYNAMIC DUAL GRAIN SPAIRING

- Provision Spare Area for Two Granularities



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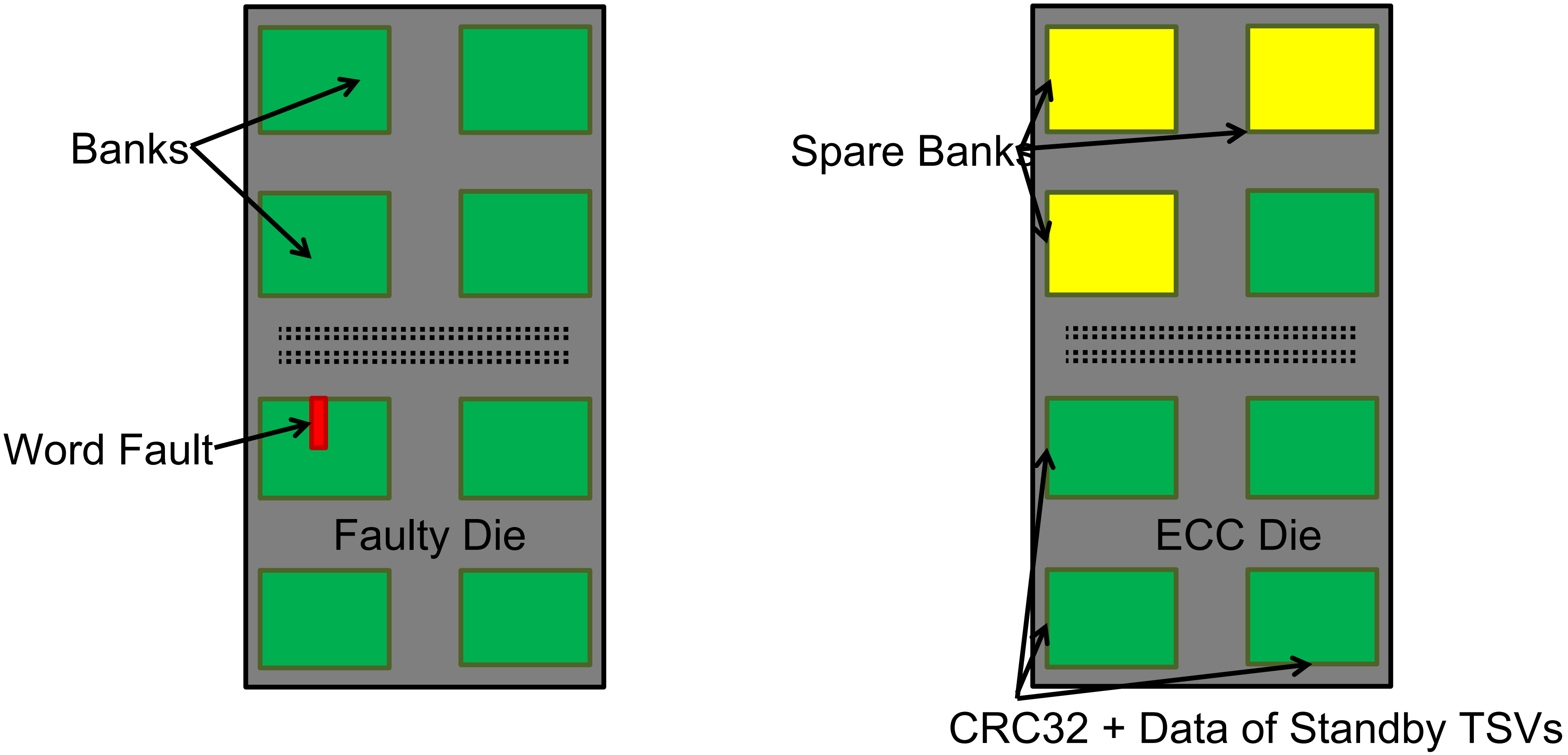

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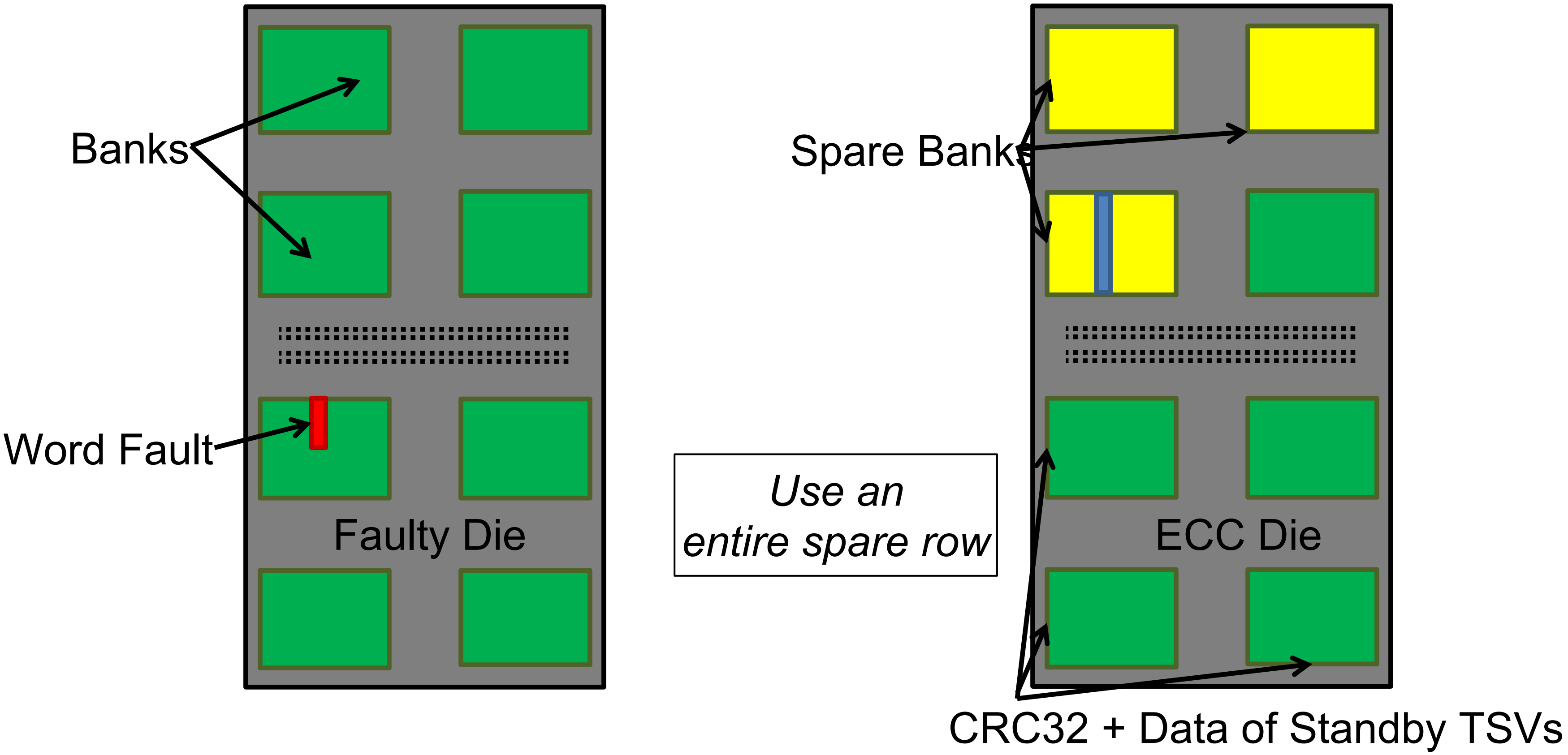

Use an entire spare row

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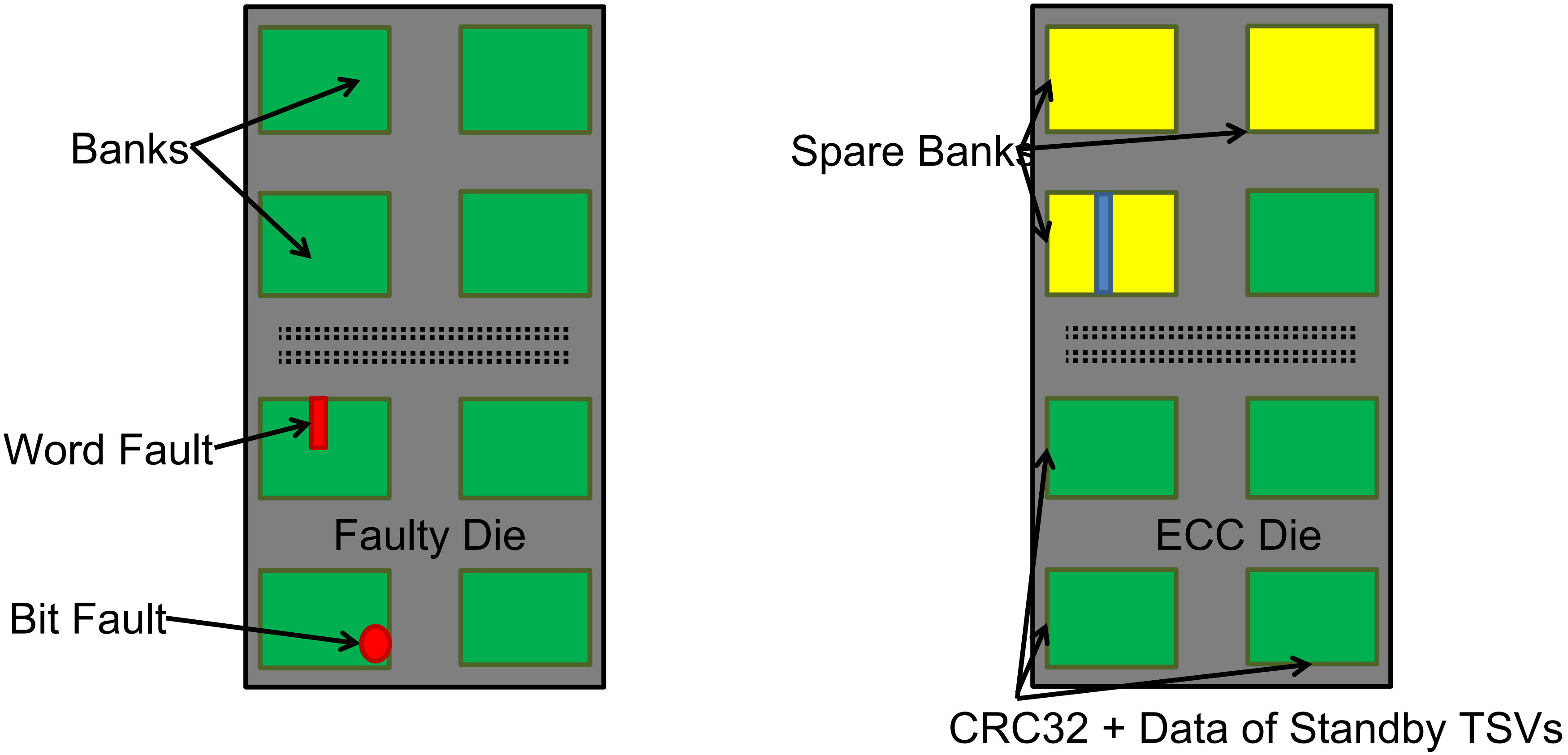

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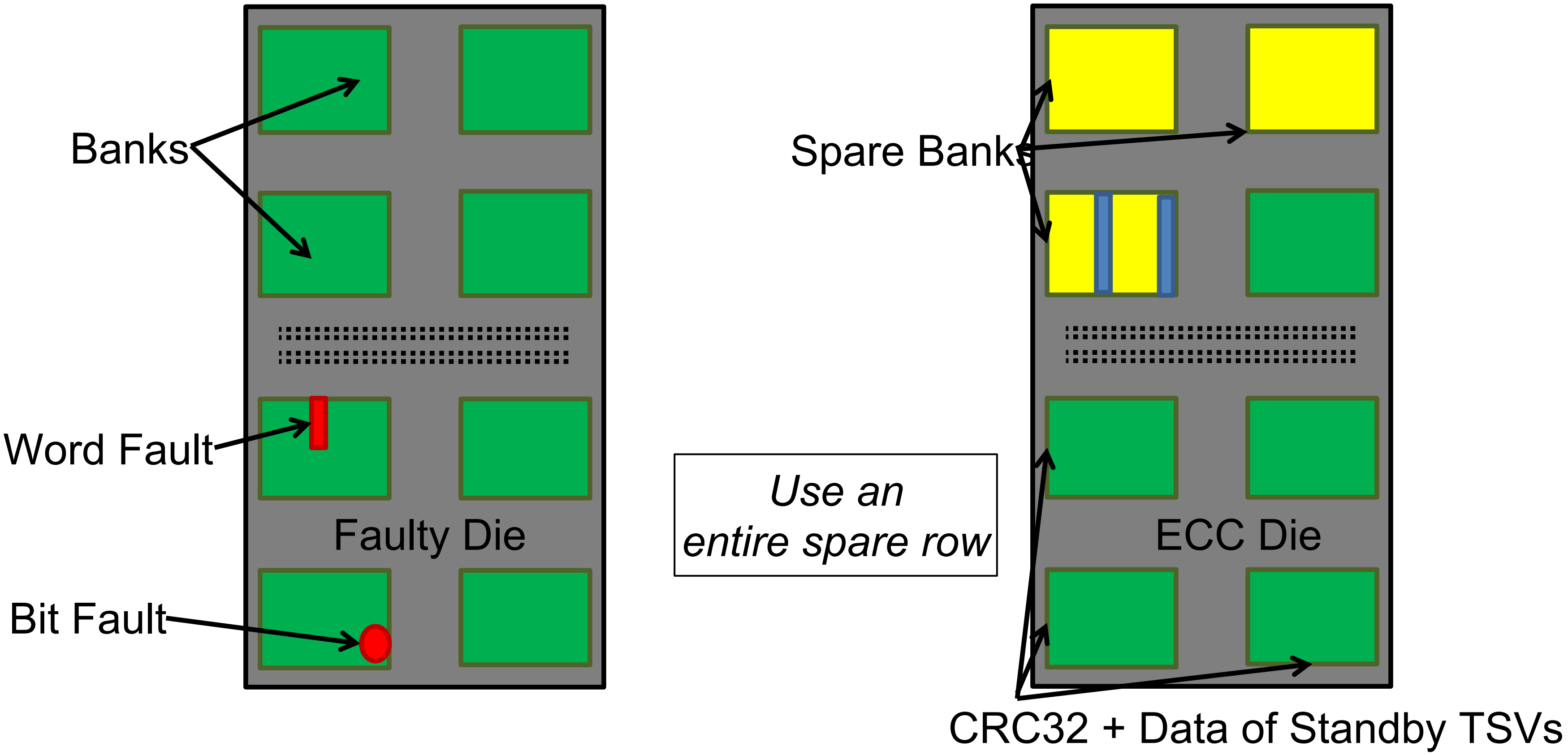

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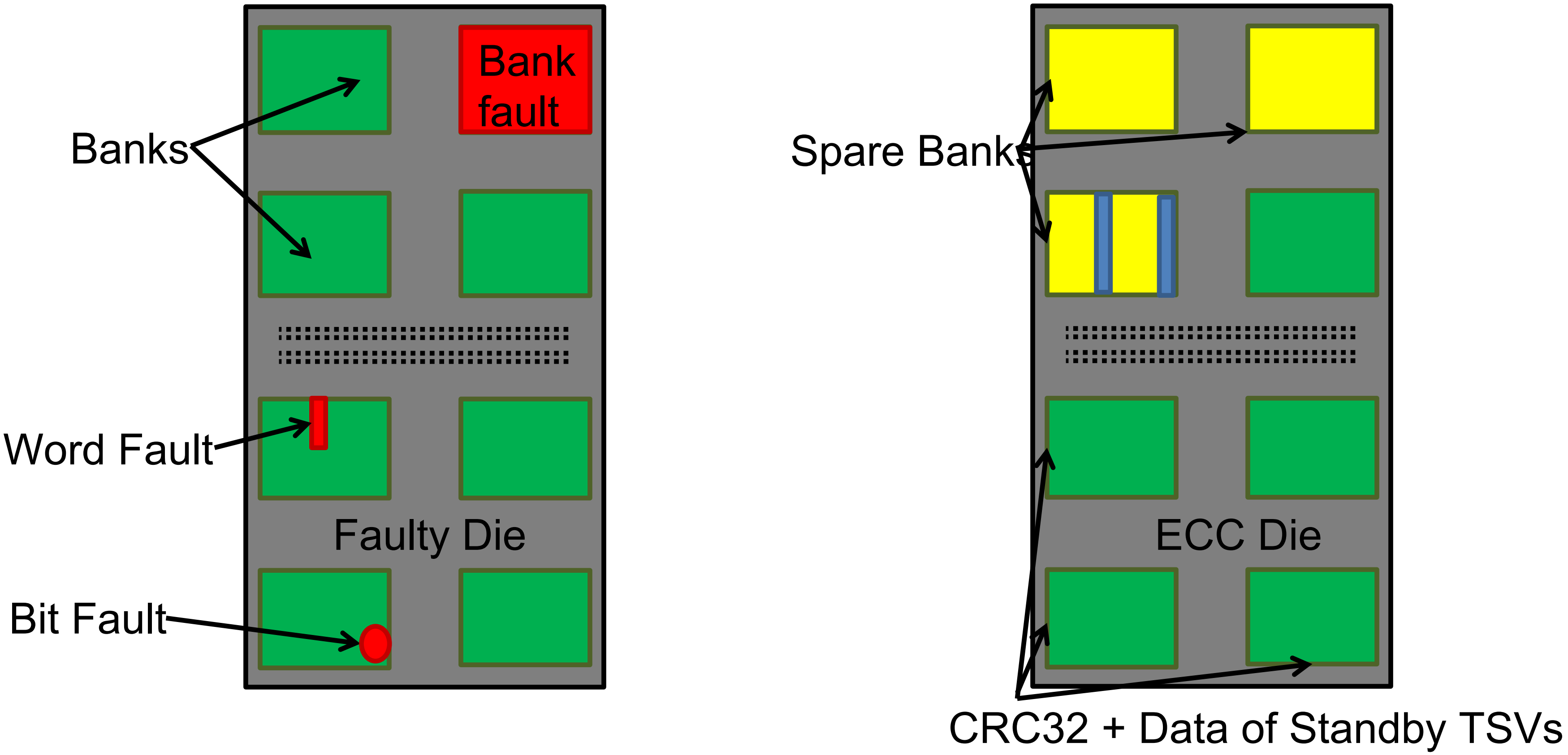

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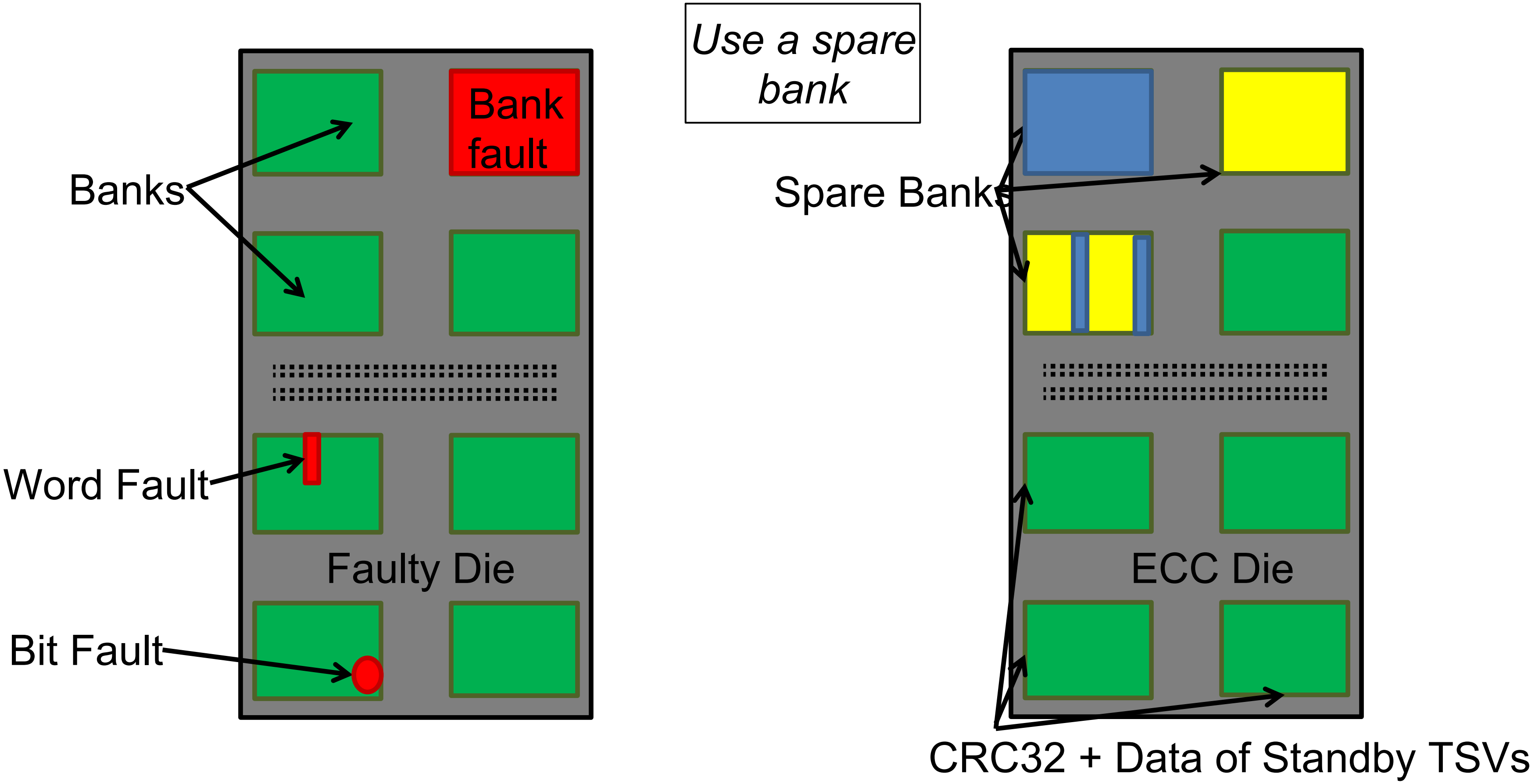

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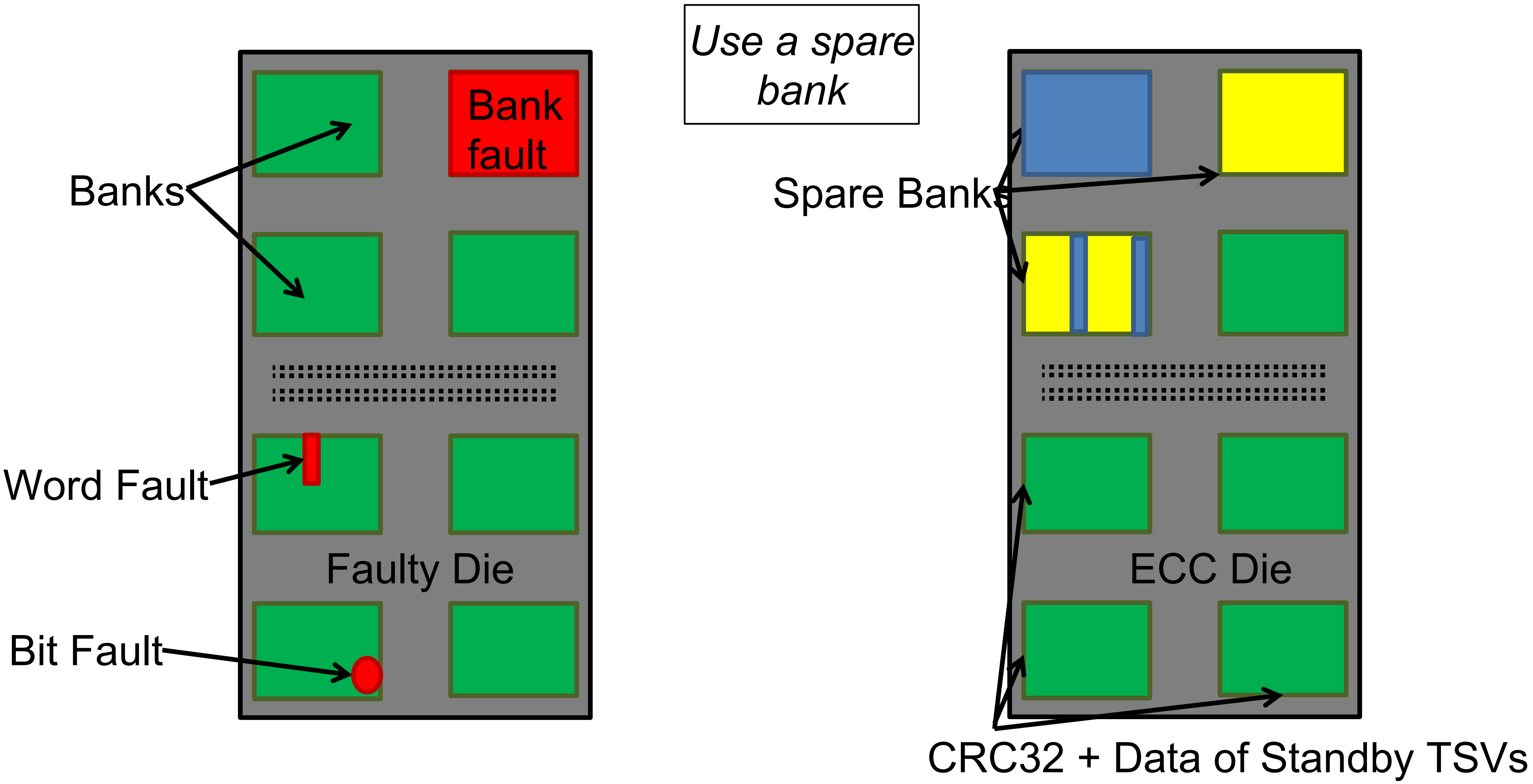
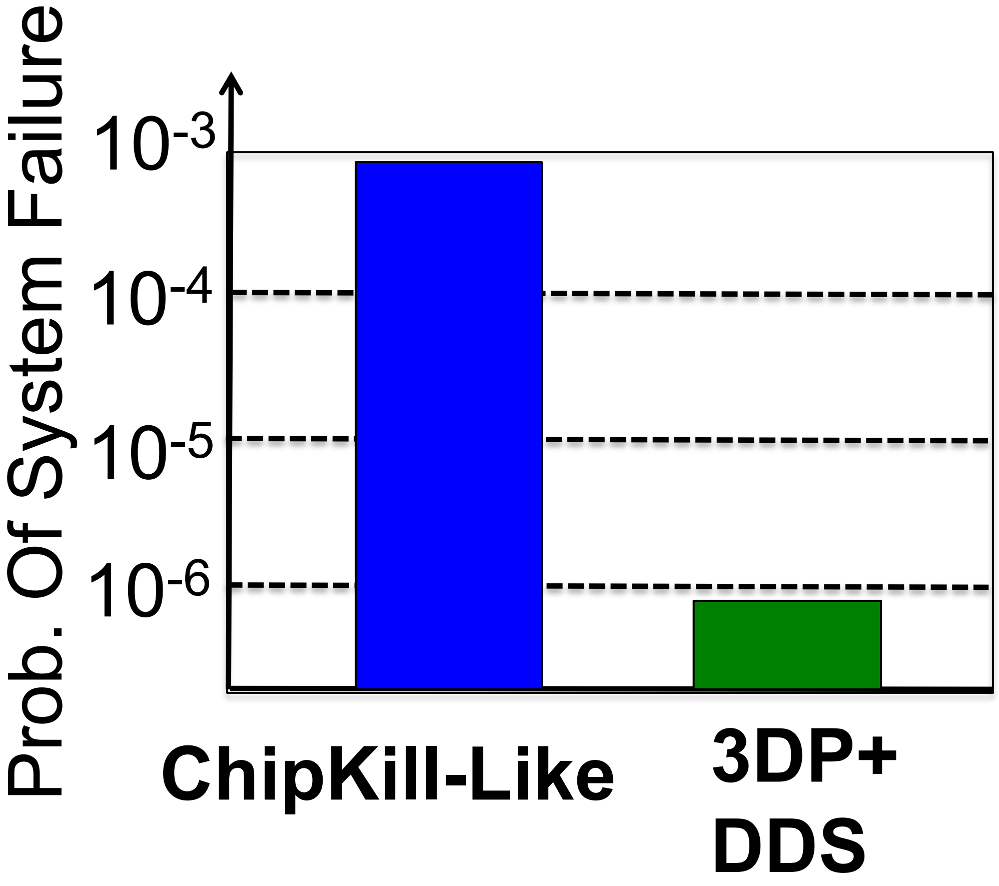


Dual Grain Sparing Efficiently Uses Spare Area

CITADEL: RESULTS



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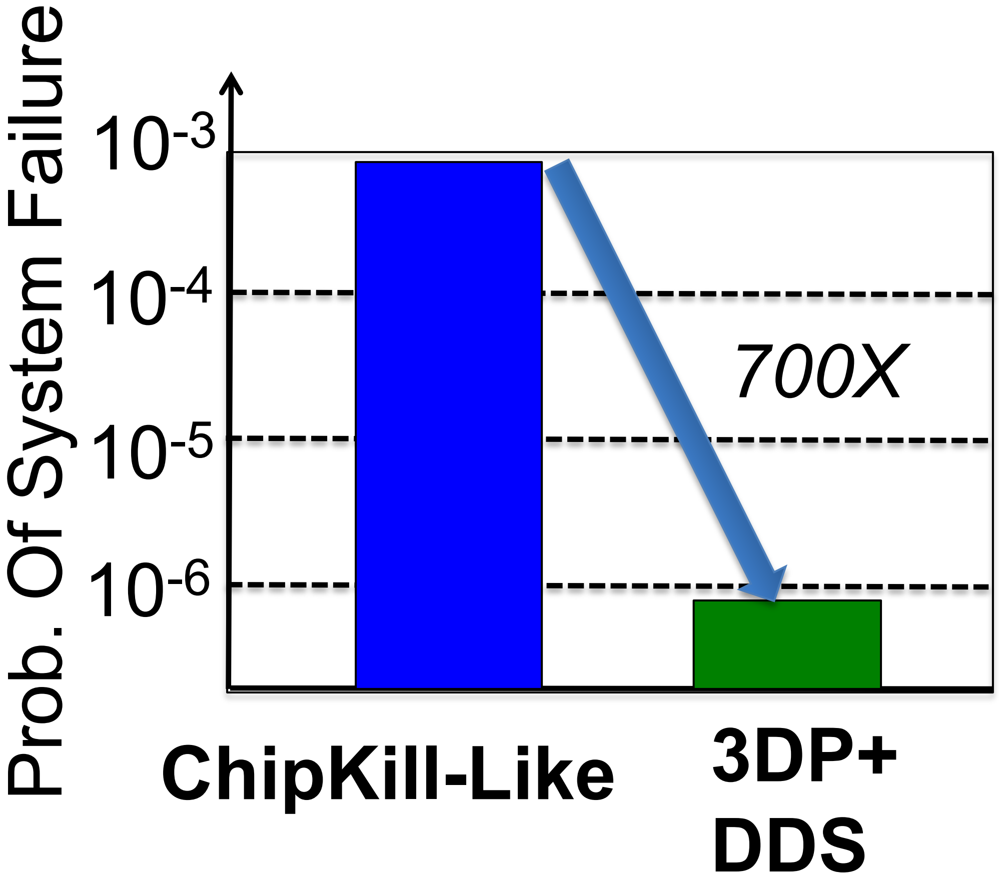

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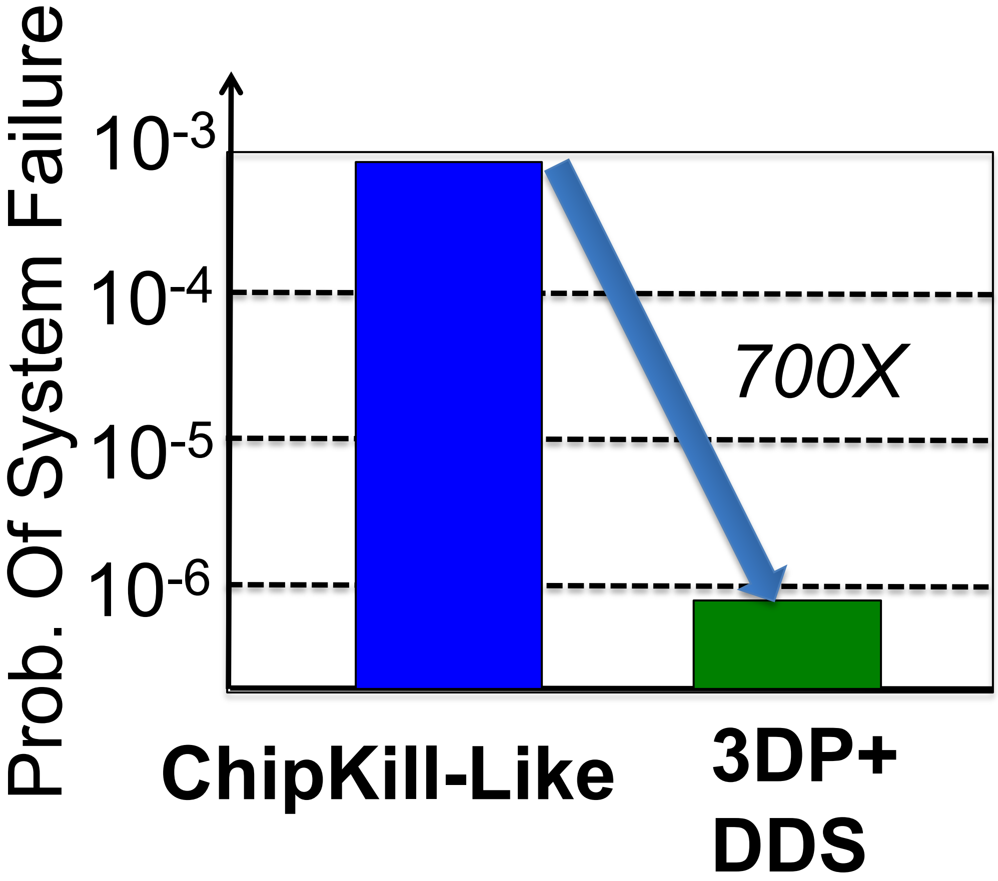

System: 8GB HBM @ DDR3-1600
Baseline: No Protection + Same Bank

Scheme	Slowdown	Active Power
ChipKill	1.25	3.8X
Citadel	1.01	1.04X

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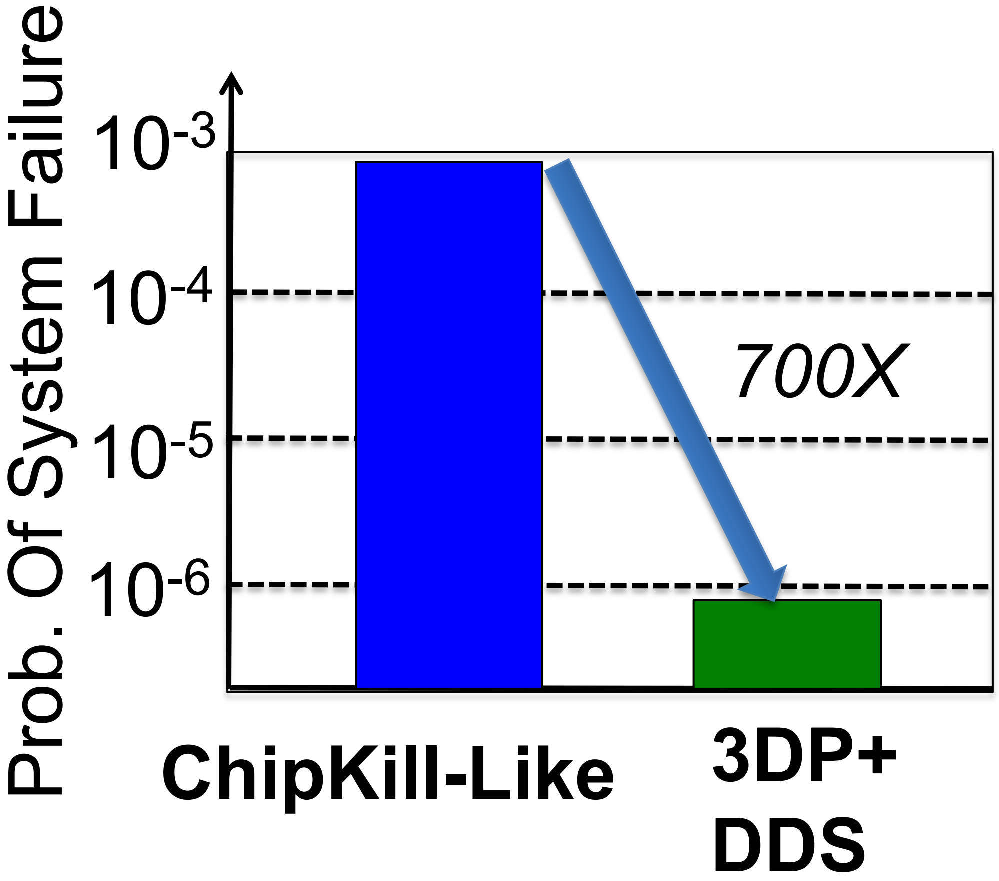

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Citadel provides **700X** more resilience, consuming only 4% additional power and 1% additional execution time

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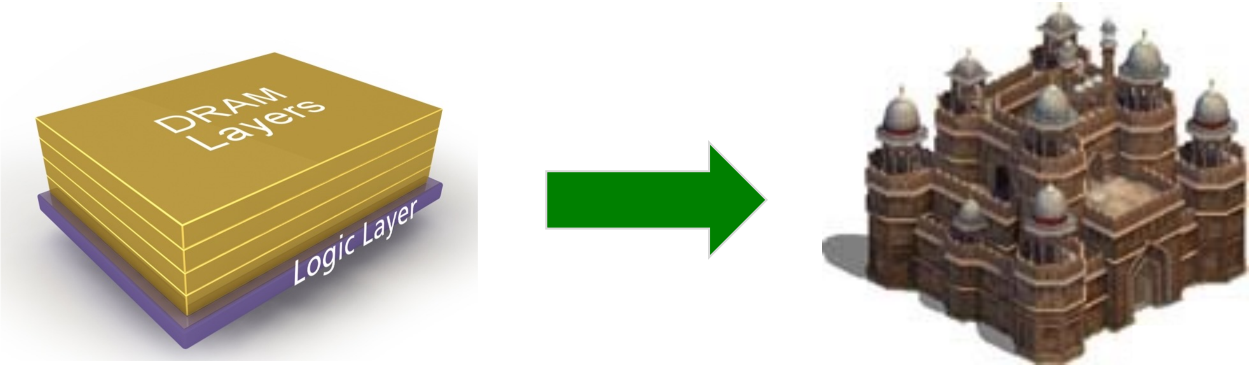


Thank You

Questions?

BACKUP SLIDES

CAUSES OF TSV FAULTS

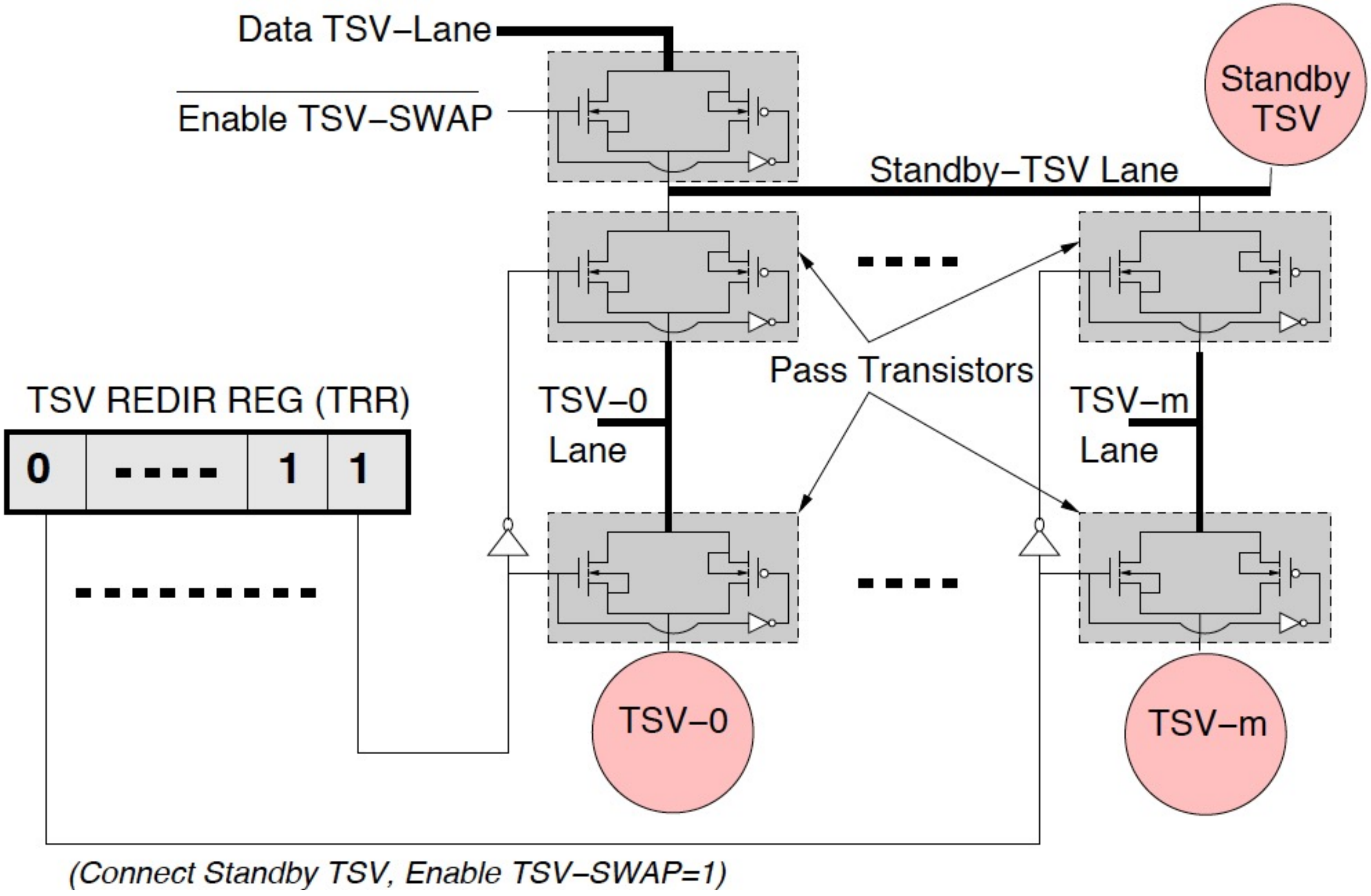
Recent papers[*+] shows that

1. TSVs prone to EM-induced voiding effects[*+]
2. Interfacial cracks → thermal-mechanical stress[*+]
3. EM-induced voids increase TSV resistance, causing path delay faults and TSV open defects[*+]
4. Micro-Bump faults[+]

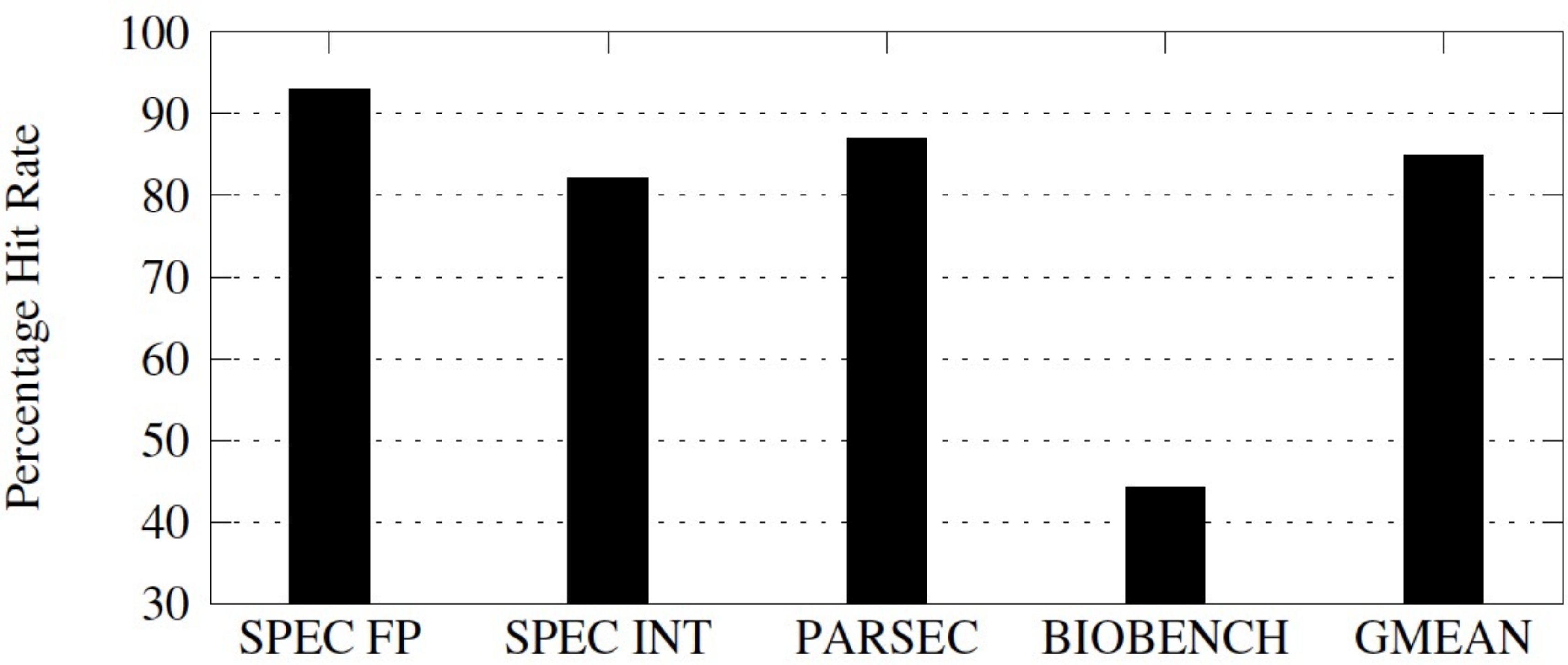
[*] Li Jiang et. al. [DAC 2013]

[+] Krishnendu C. et. al. [IRPS 2012]

TSV-SWAP REPAIR CIRCUIT



PARITY CACHE: HIT RATE



Benchmarks