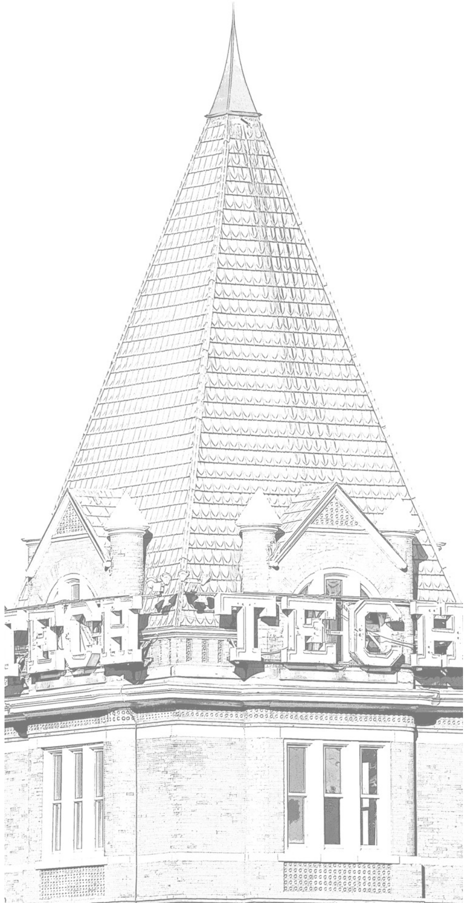
Reducing Read Latency of Phase Change Memory via Early Read and Turbo Read



Feb 9th 2015

HPCA-21 San Francisco, USA

Prashant Nair - Georgia Tech

Chiachen Chou - Georgia Tech

Bipin Rajendran – IIT Bombay

Moinuddin Qureshi - Georgia Tech

INTRODUCTION TO PCM

- Phase Change Memory (PCM) promises higher density and better scalability

Key Challenges:

- Limited Endurance (10-100M writes/cell)
- High Write Latency (4X-8X higher than PCM read)
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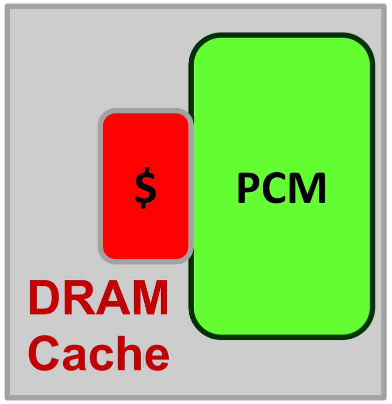

Hybrid Memory

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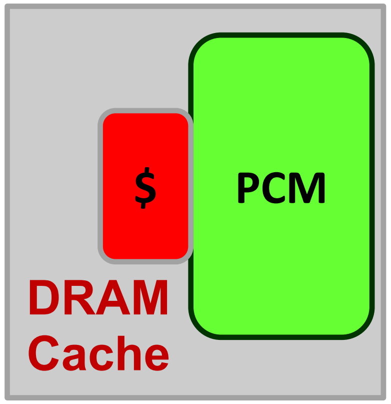


Hybrid Memory

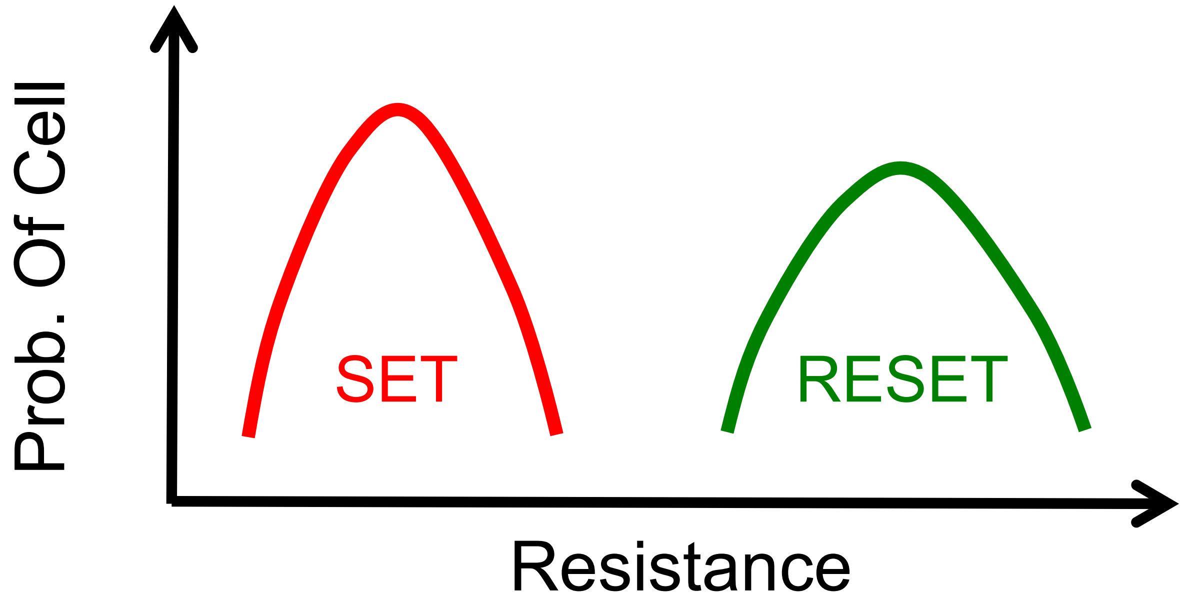
Goal ➔ Reduce the high read latency of PCM

OUTLINE

- Background ⇦
- Early Read
- Turbo Read
- Early+Turbo Read
- Results
- Summary

STORING DATA IN PCM CELLS

- Low (SET) and High (RESET) resistance states



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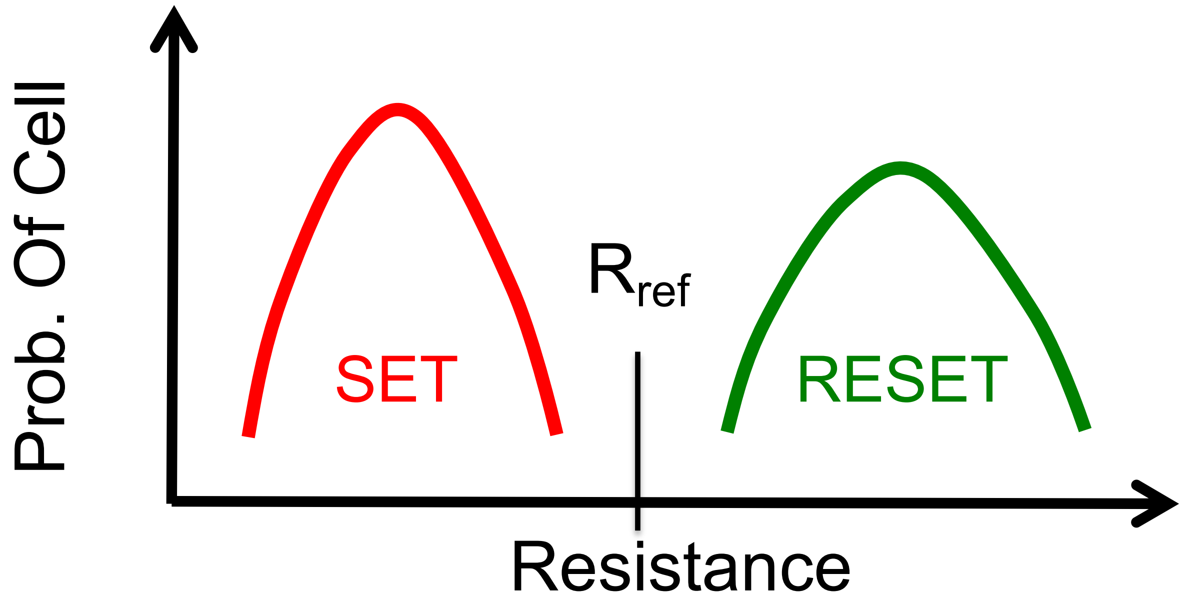

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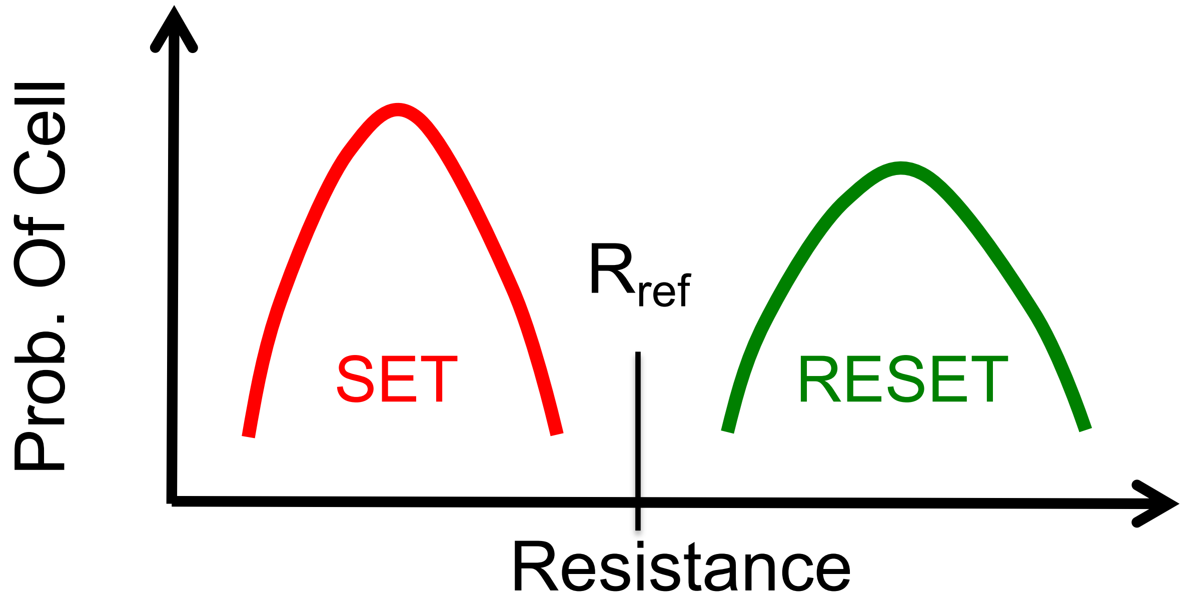

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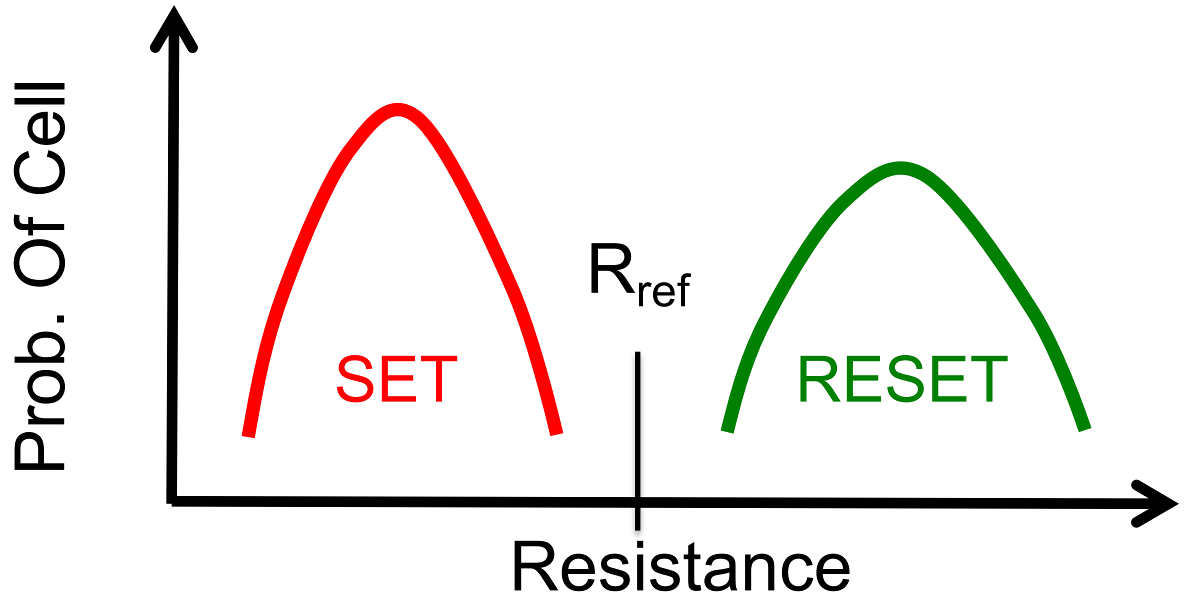

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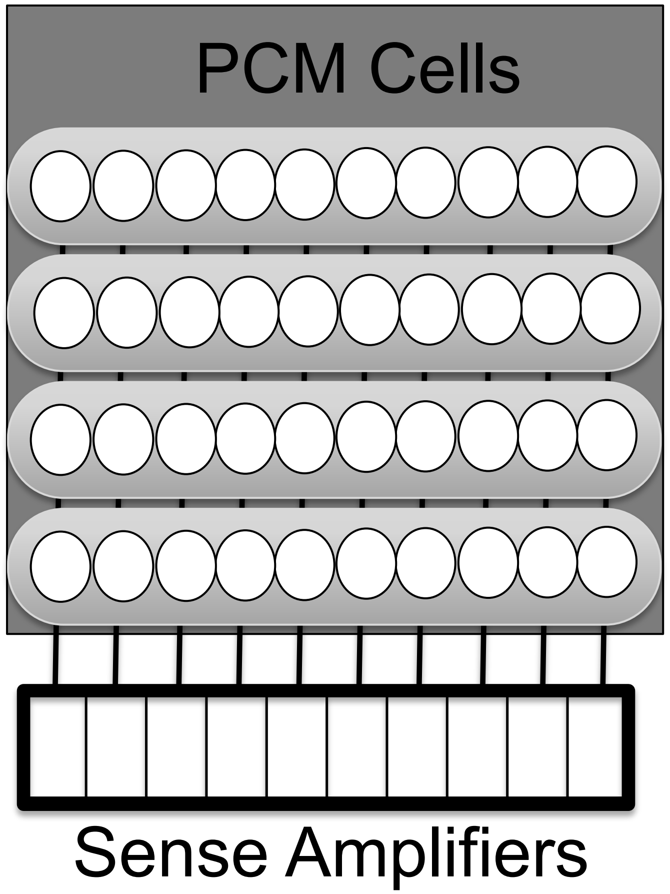
PCM stores binary values by varying resistance of cells

READ PROCESS IN PCM

Three step process to read a PCM cell

V_{DD}
0
time
V
time



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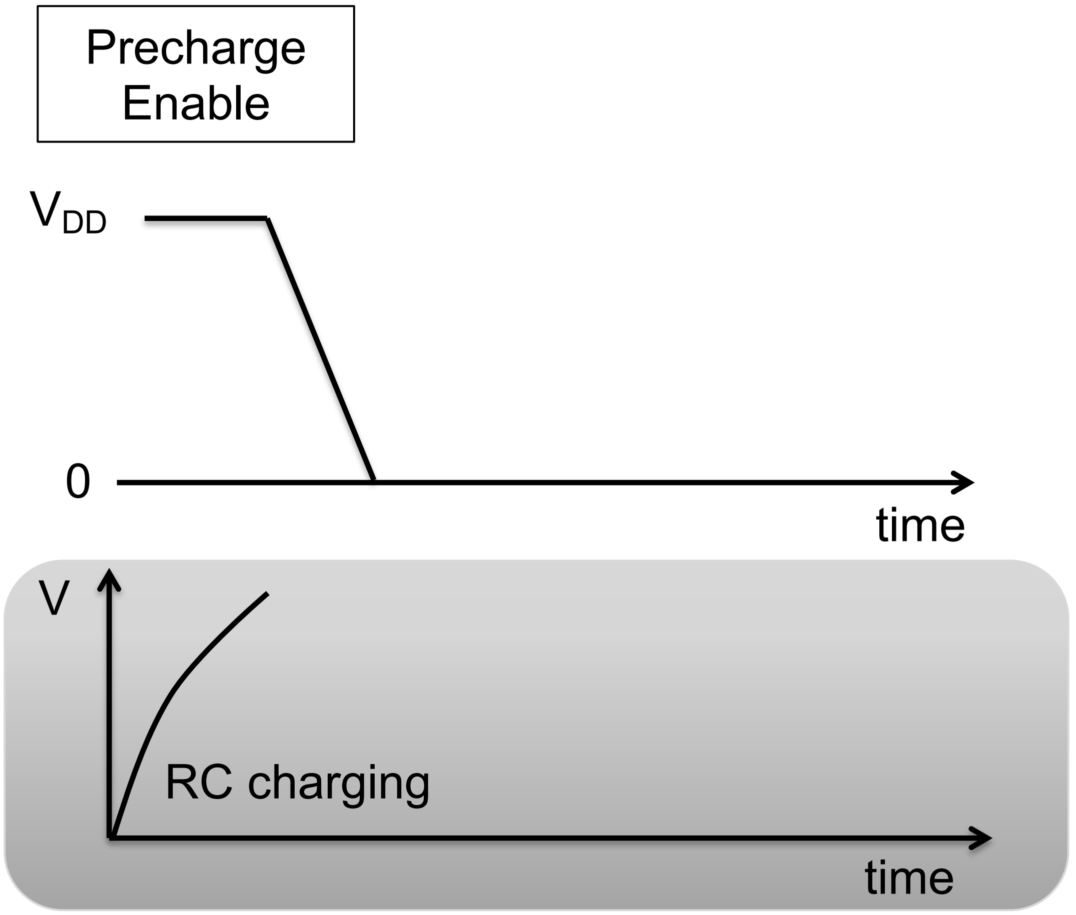

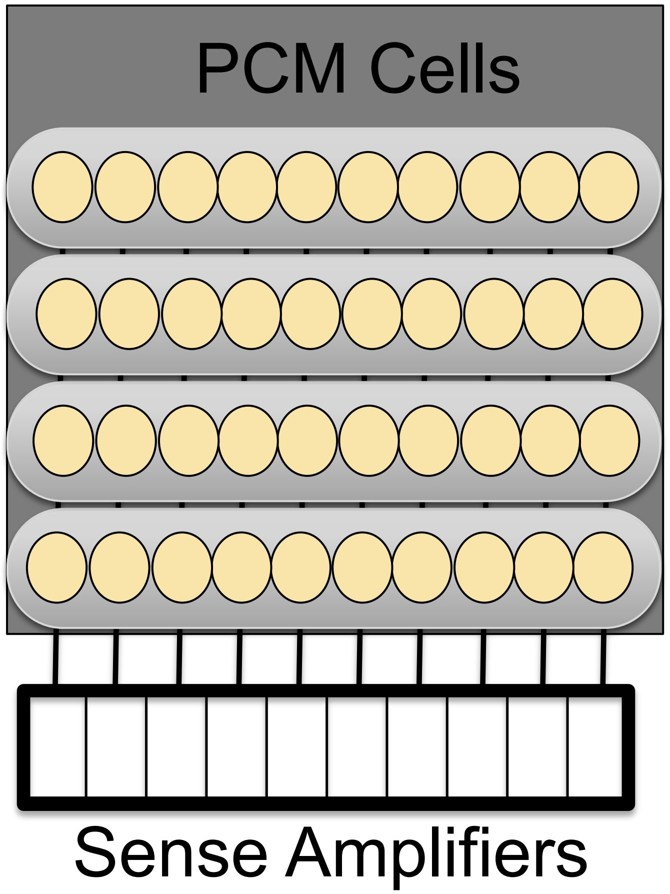

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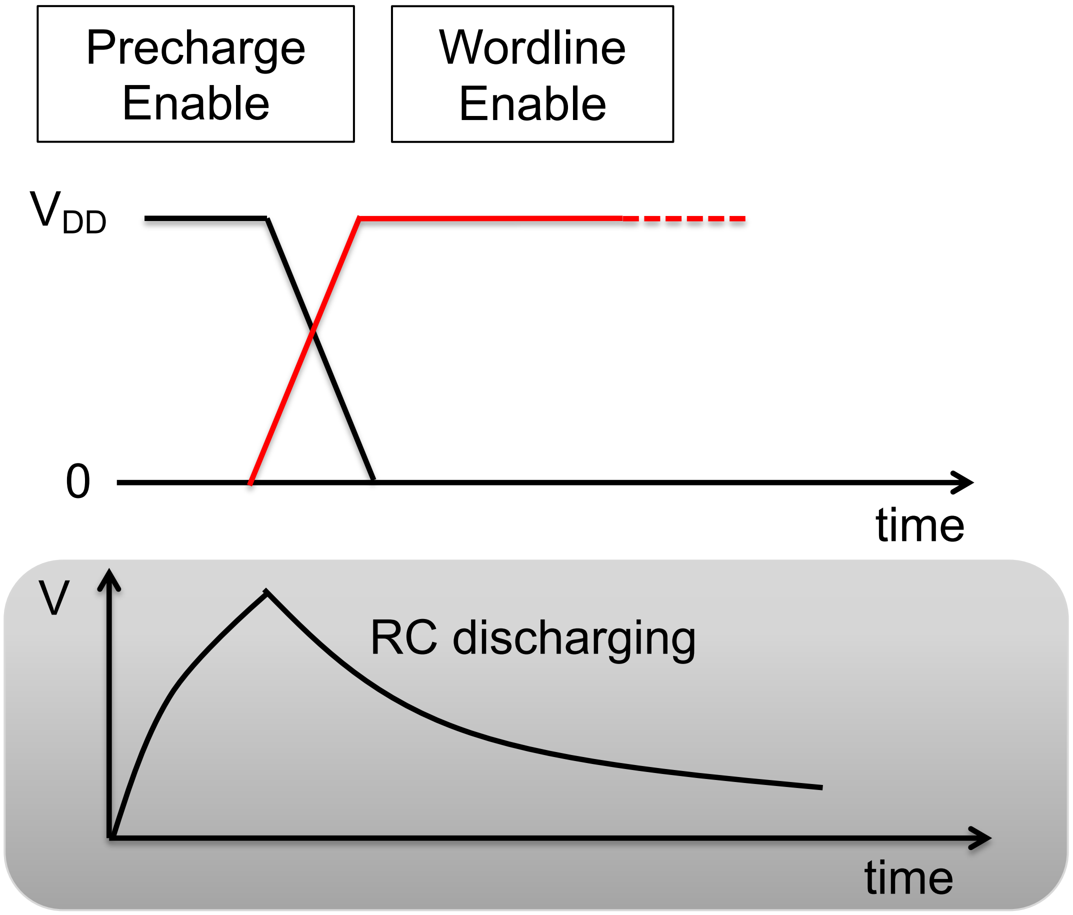

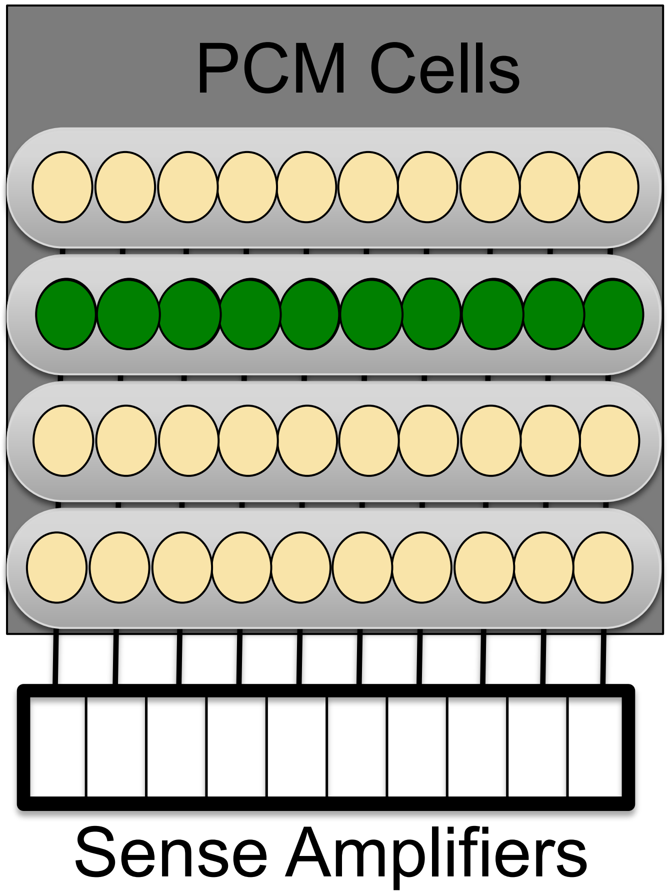

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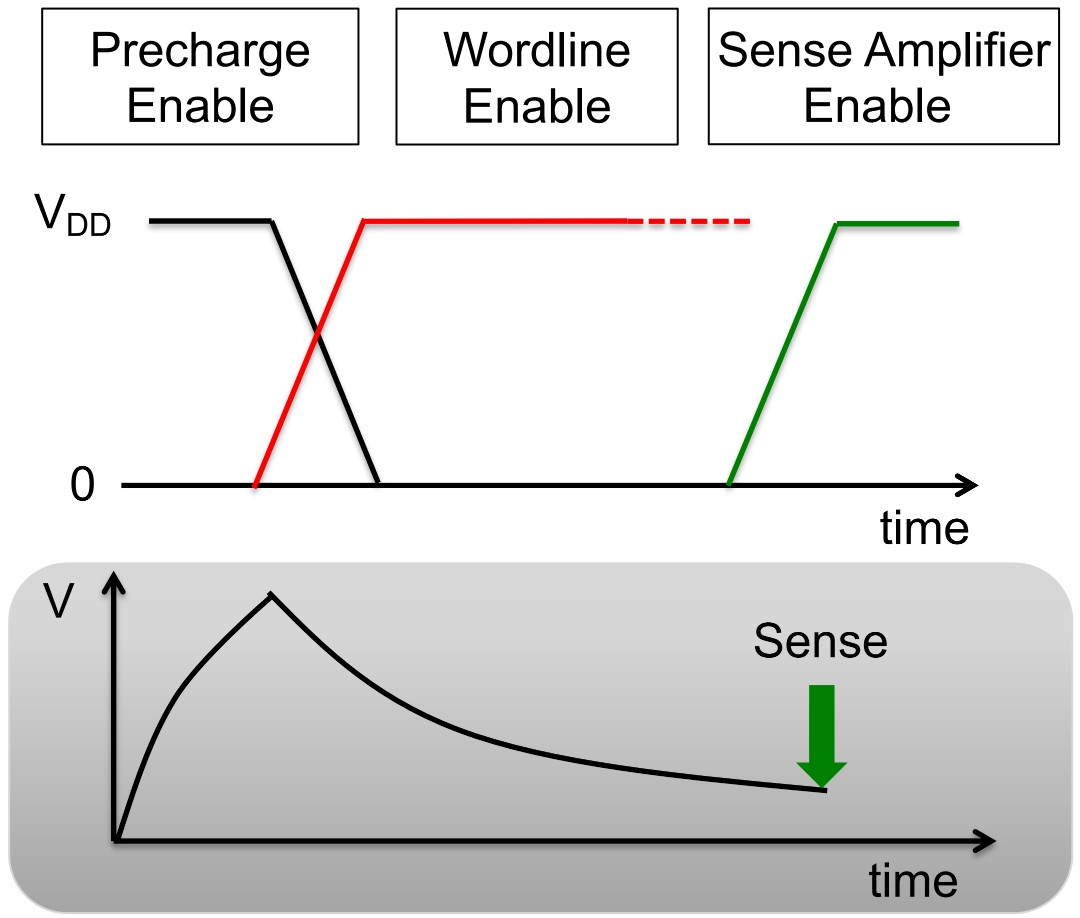

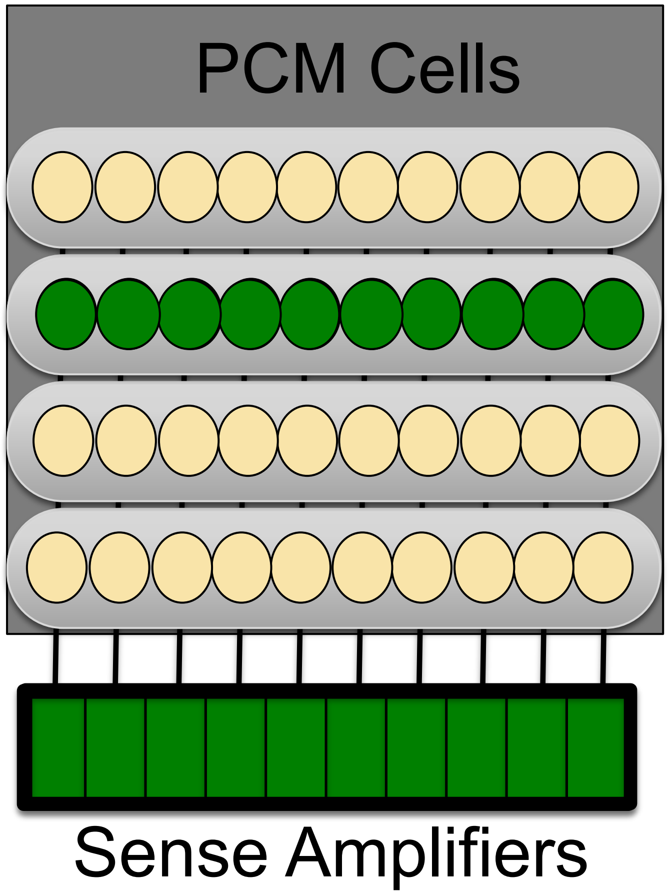

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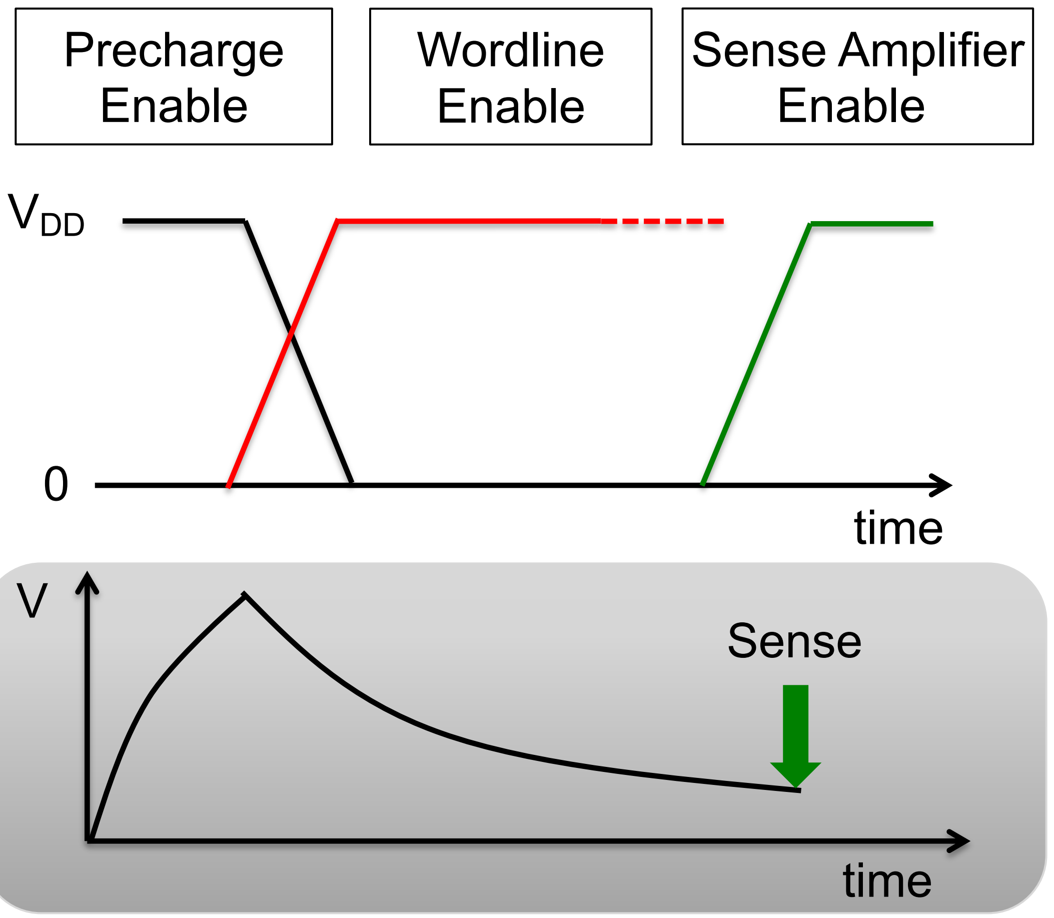
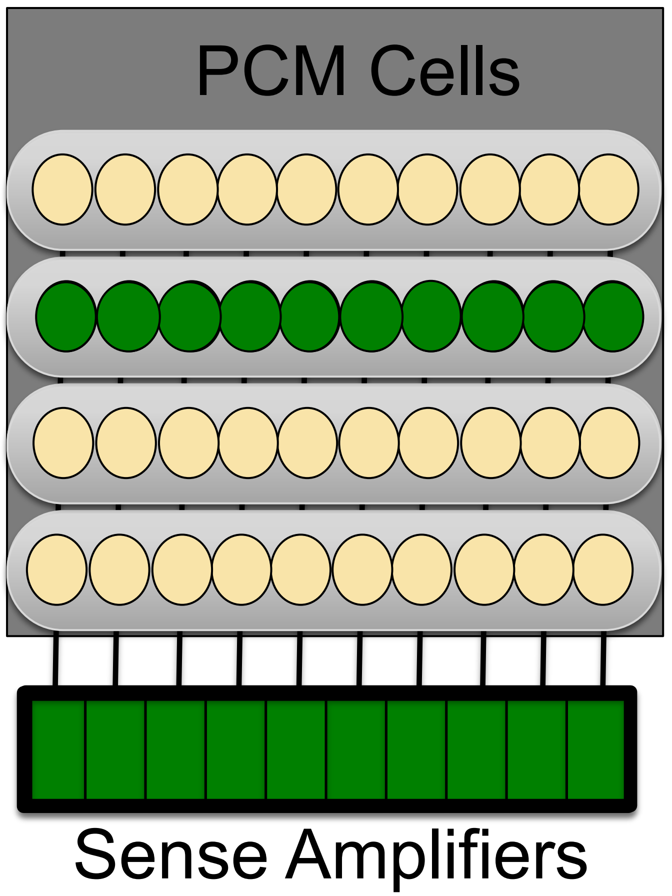
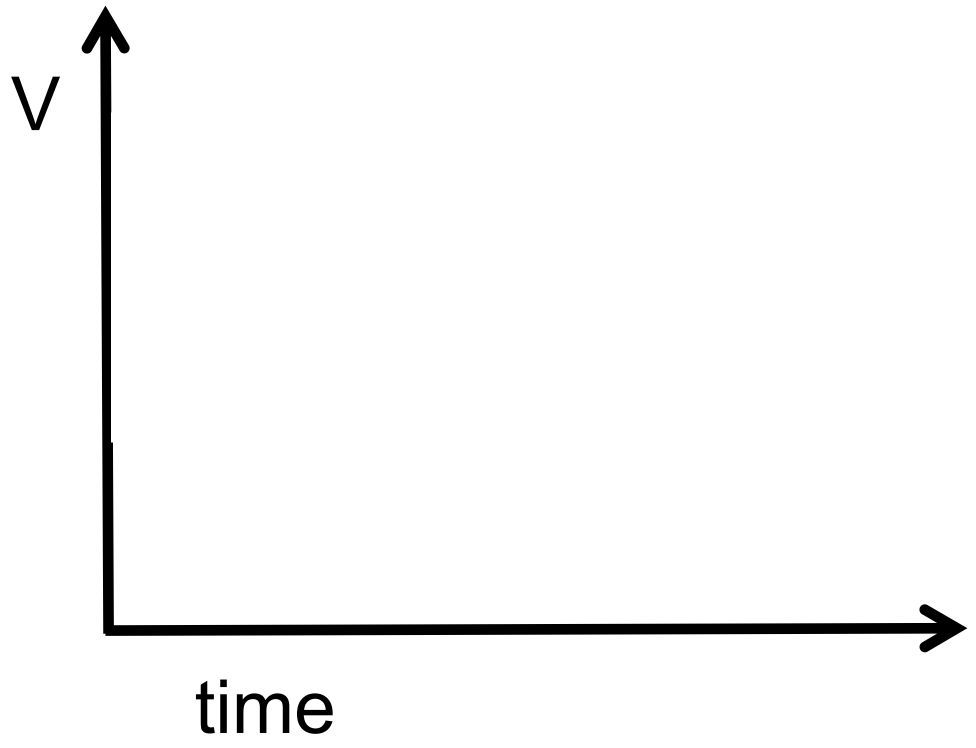
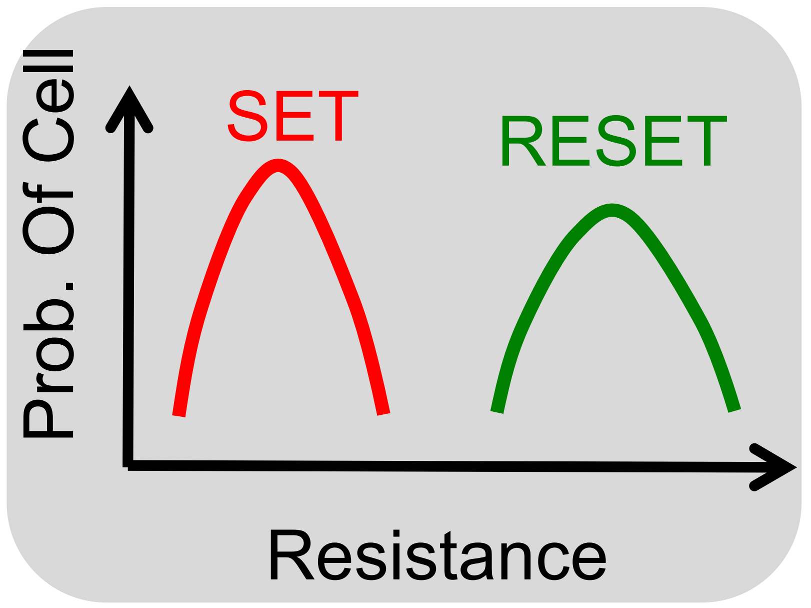




The discharging time determines the sensing time

SENSING DATA FOR READ





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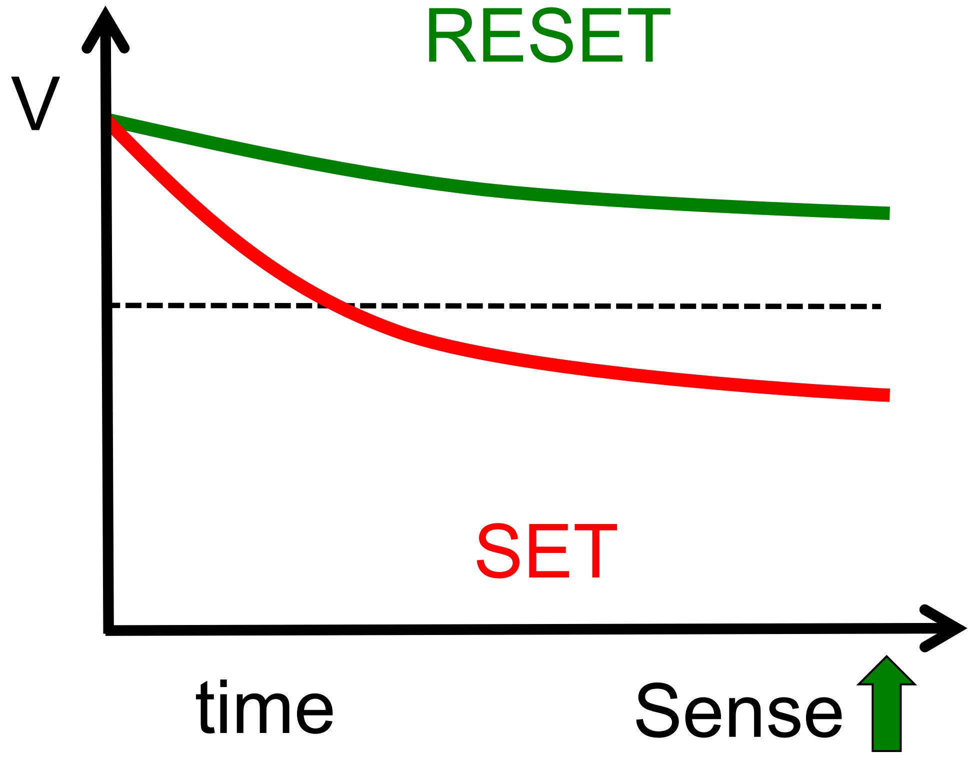

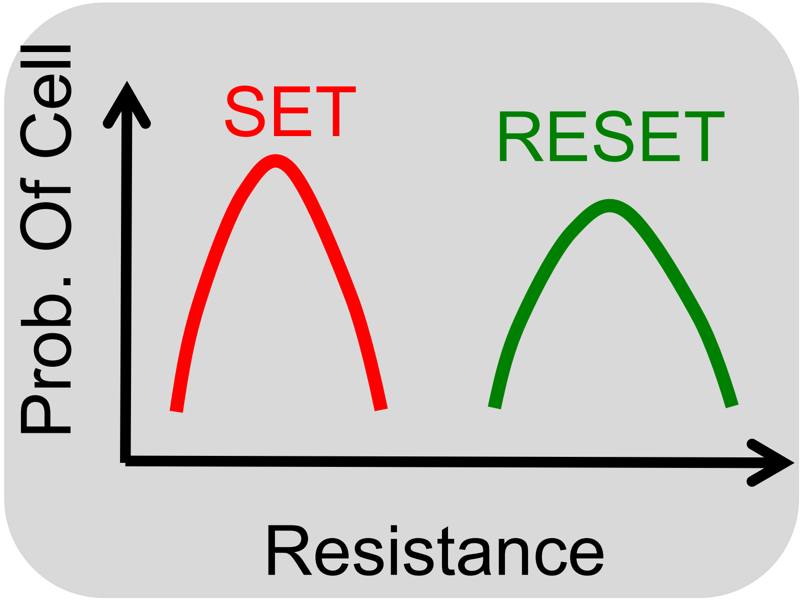

- Capacitive Discharge and compare against V_{ref}

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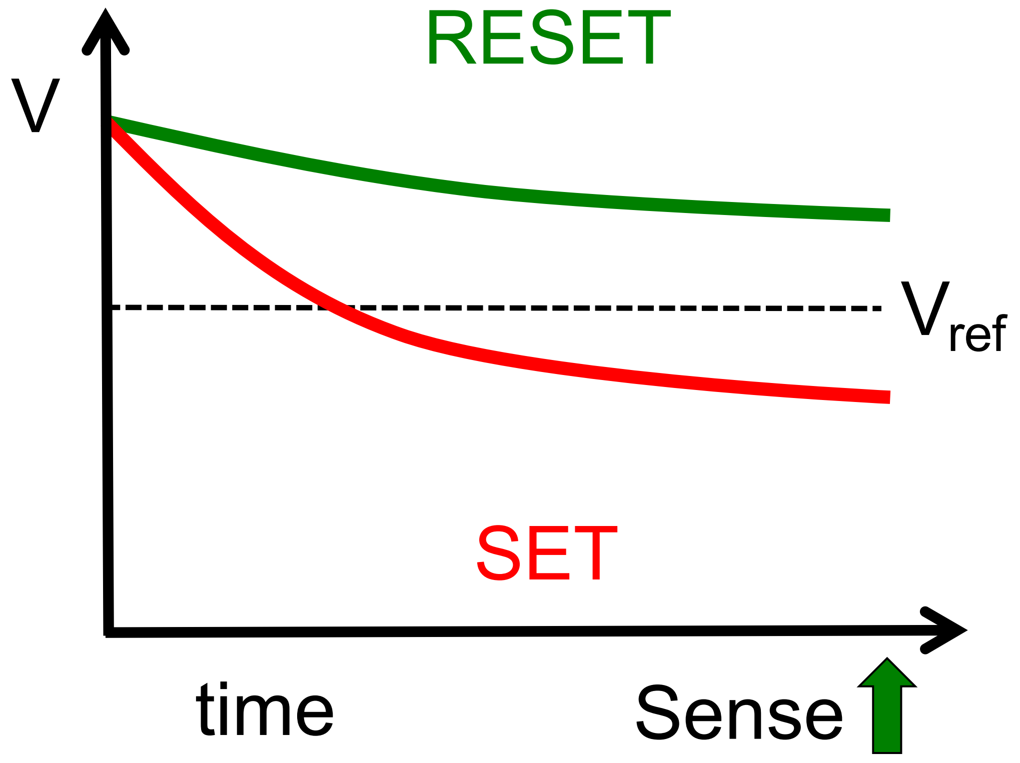

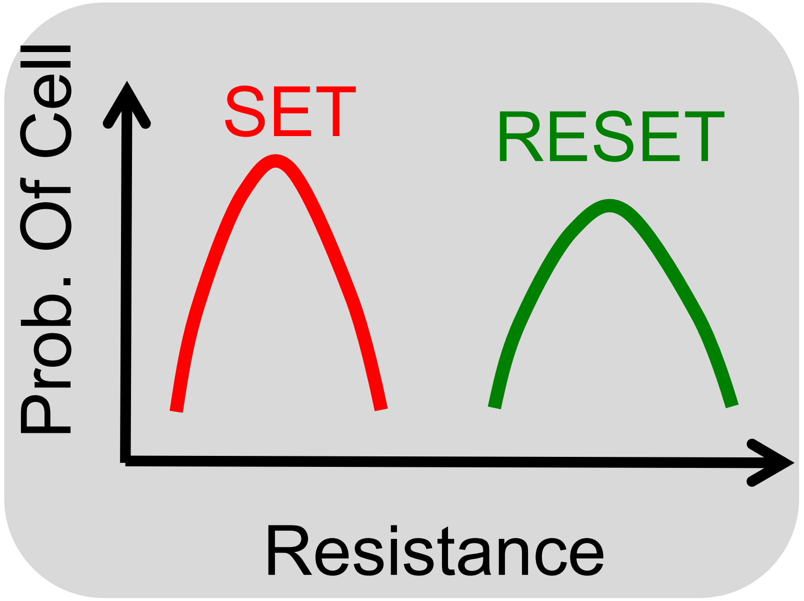

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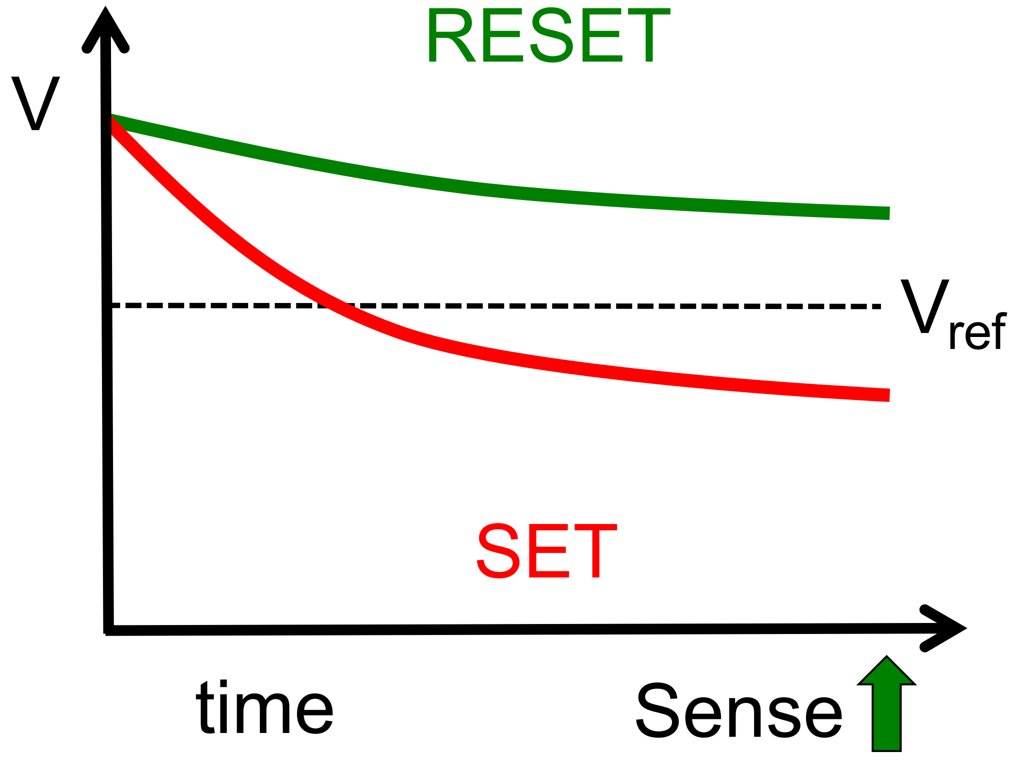

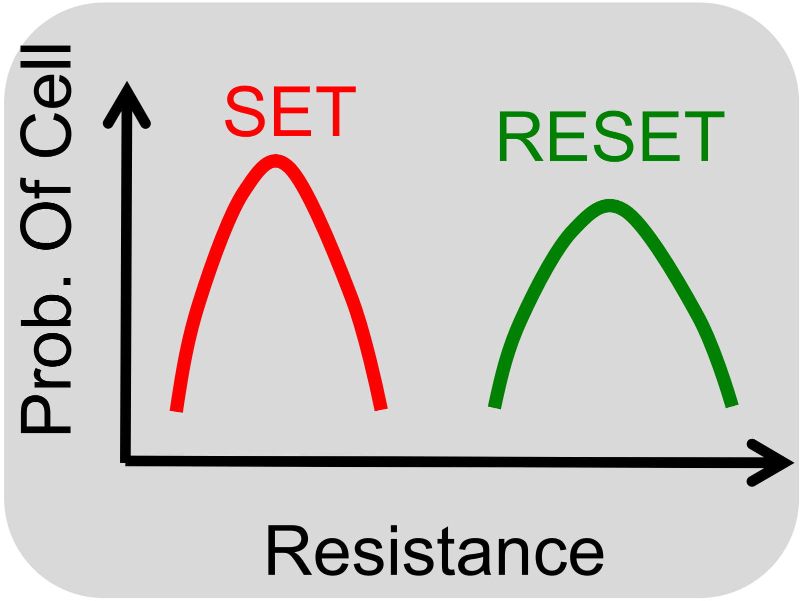

- Capacitive Discharge and compare against V_{ref}
- Variation in SET and RESET distributions

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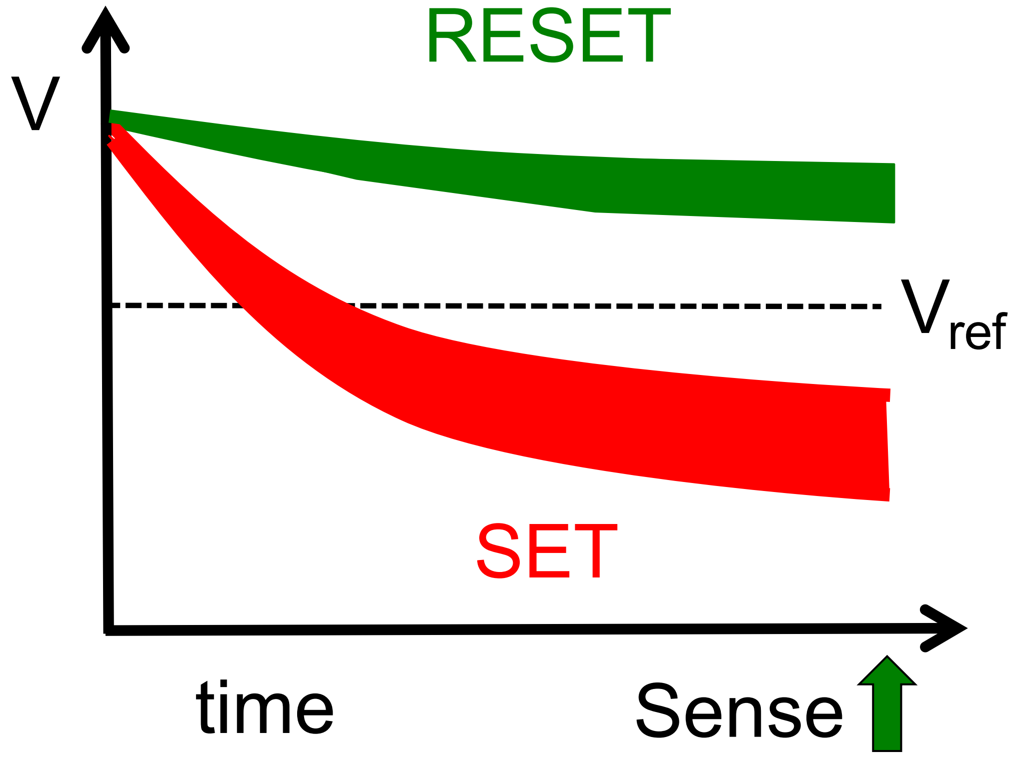

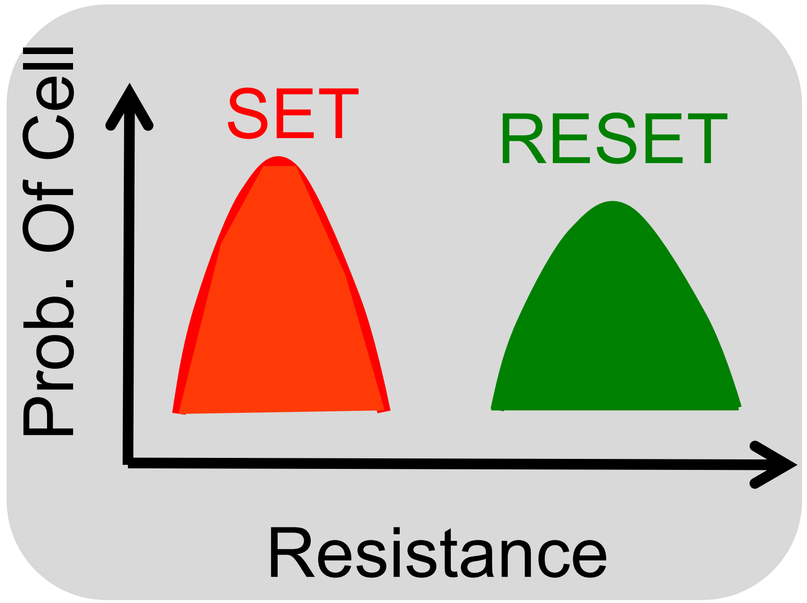

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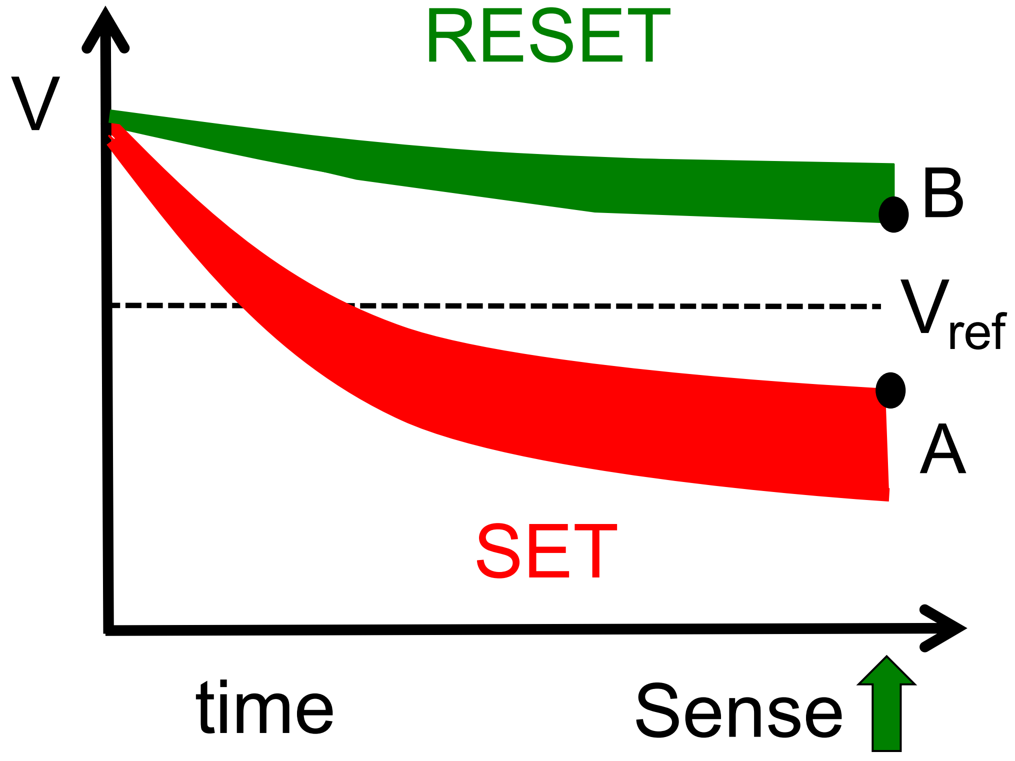

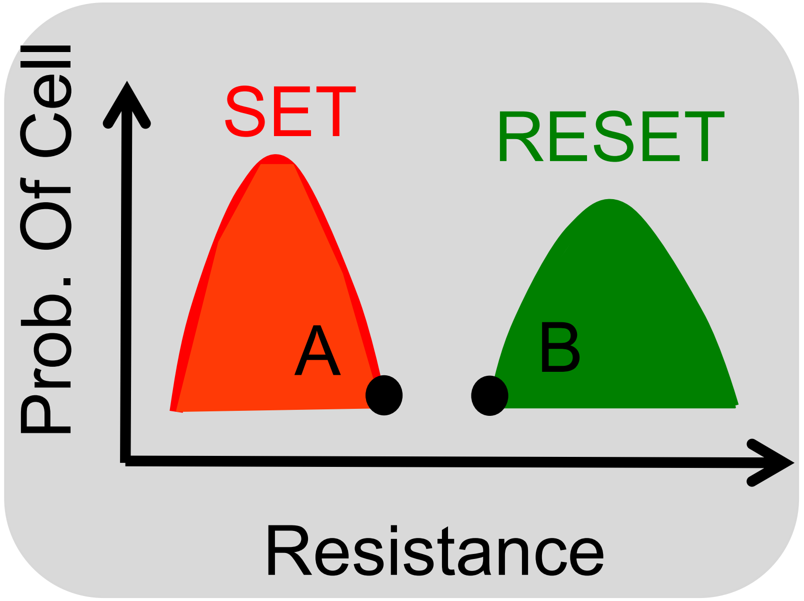

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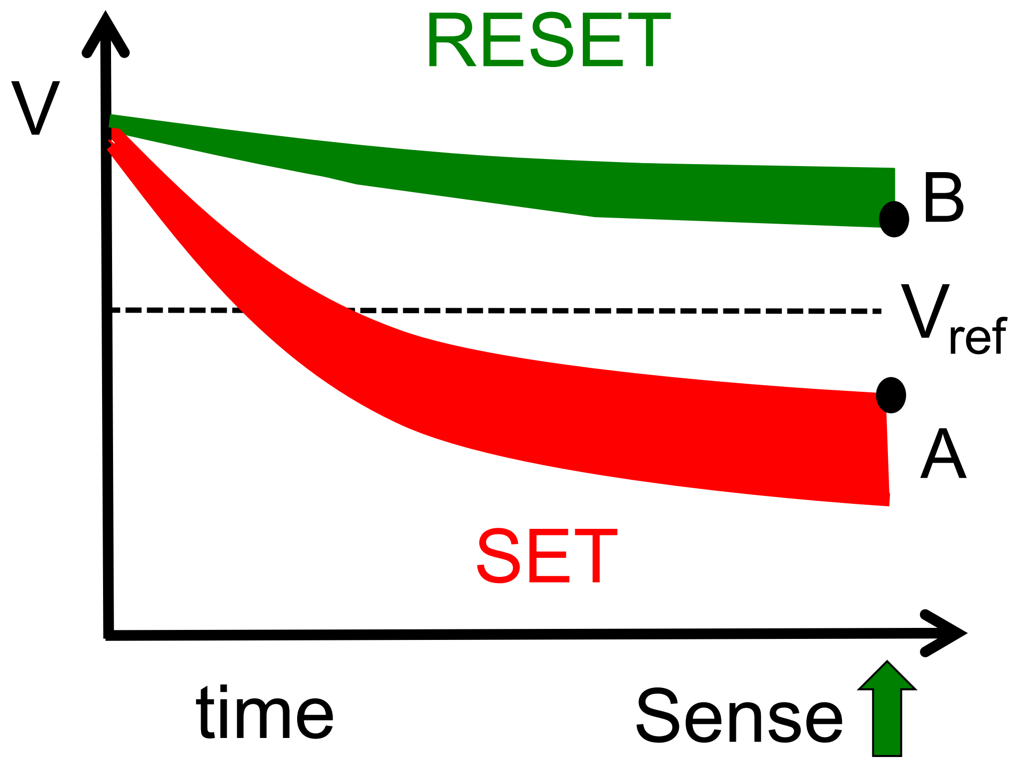

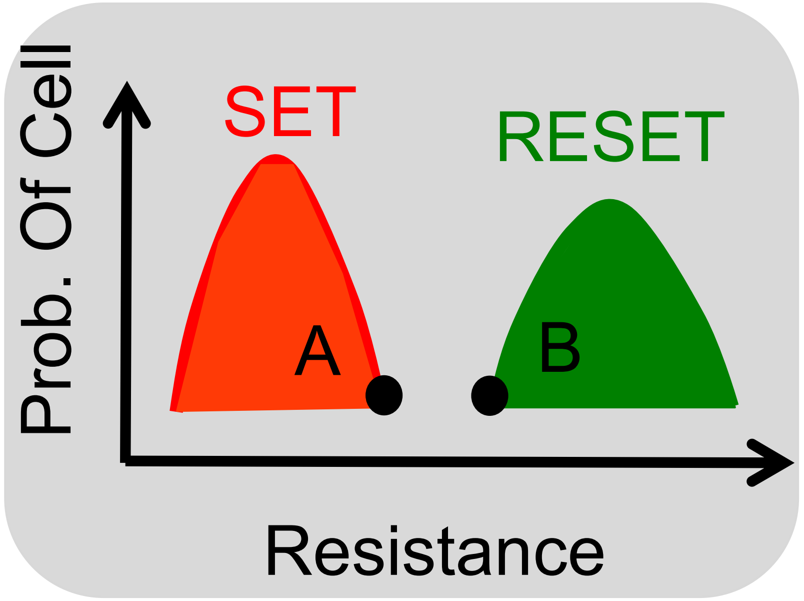

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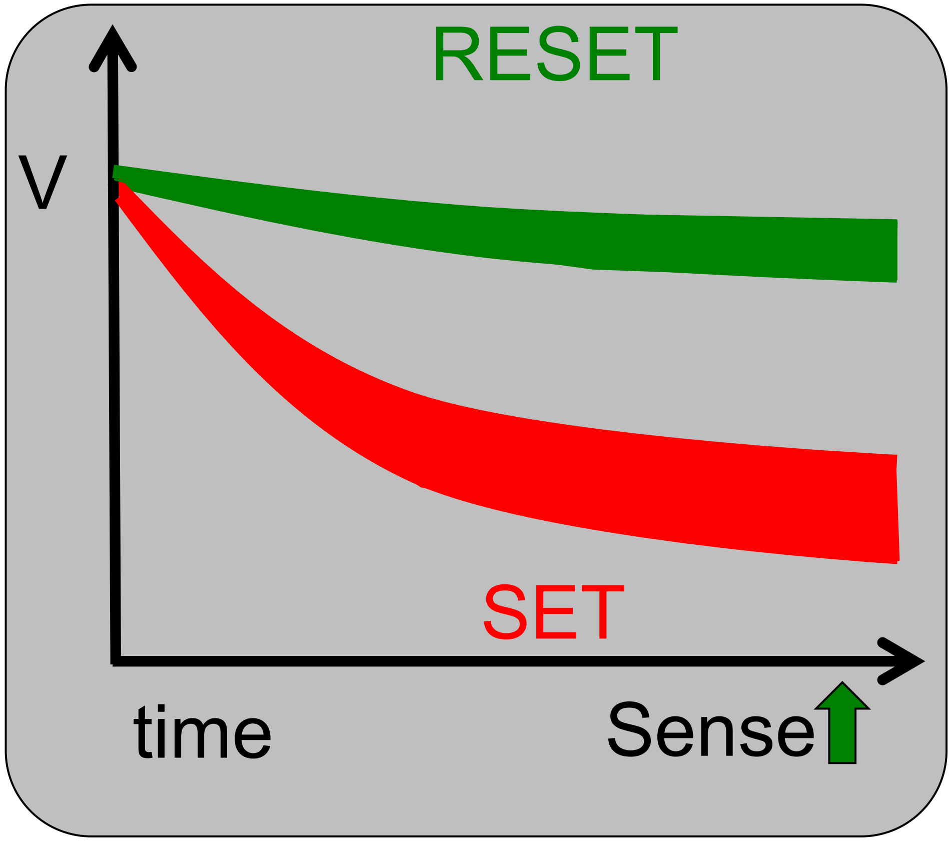
Sensing time is determined by worst case cells

REDUCE READ LATENCY : SENSE EARLIER

- Sense data earlier than the provisioned time



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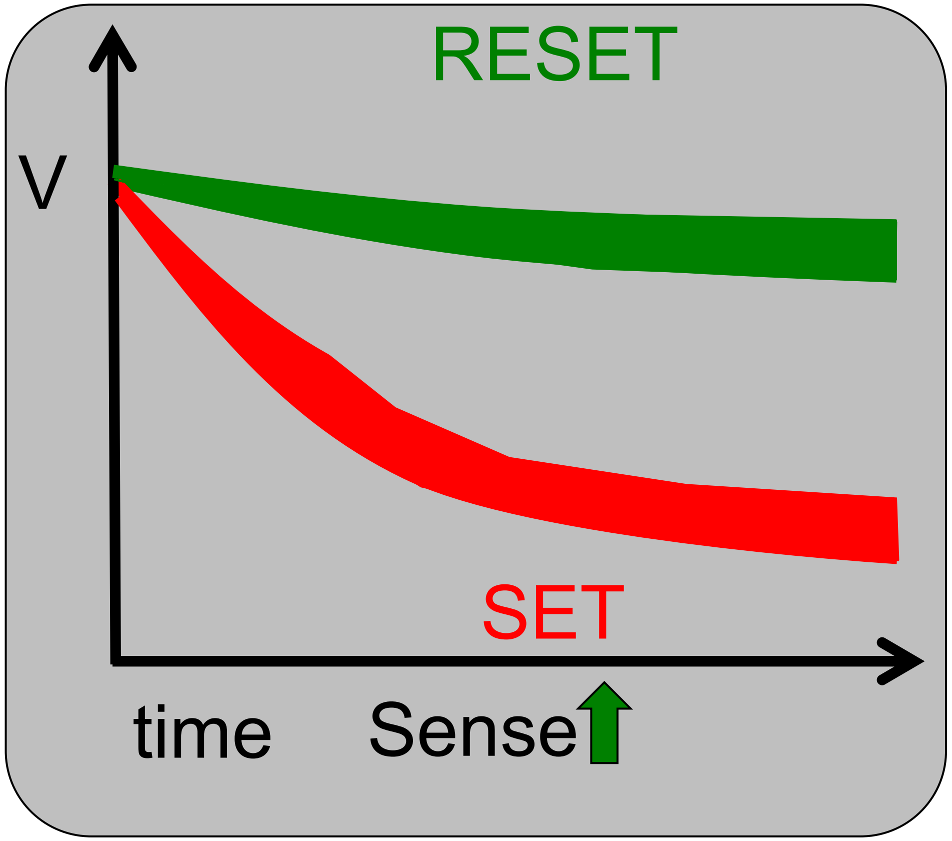

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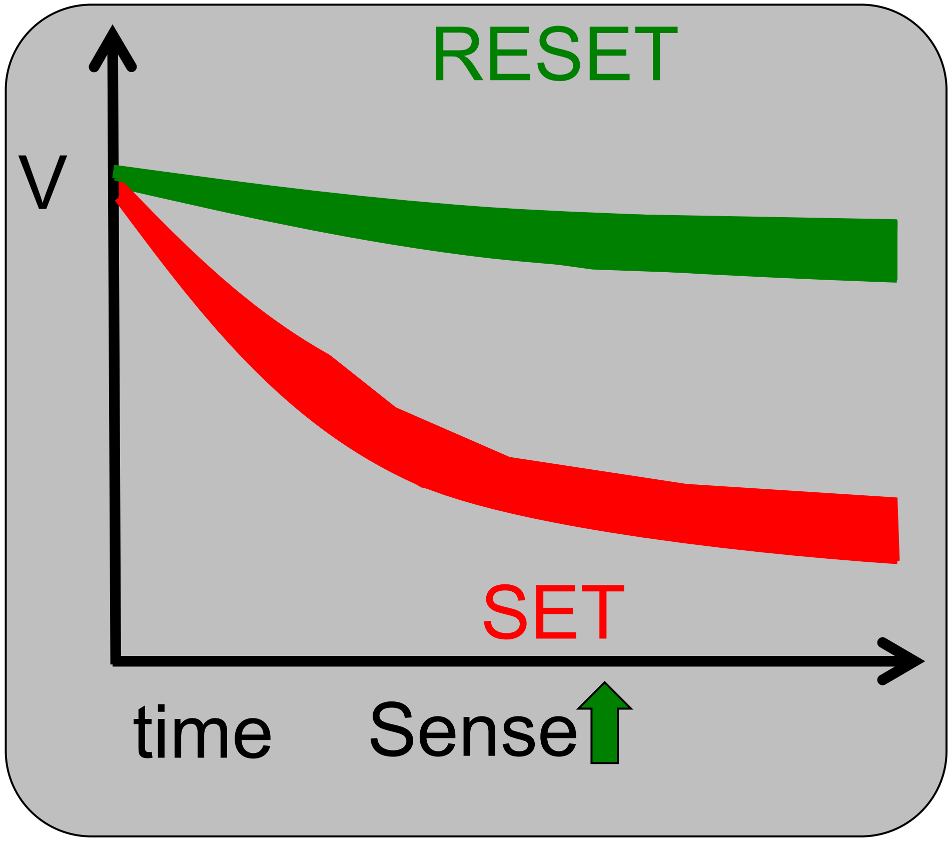
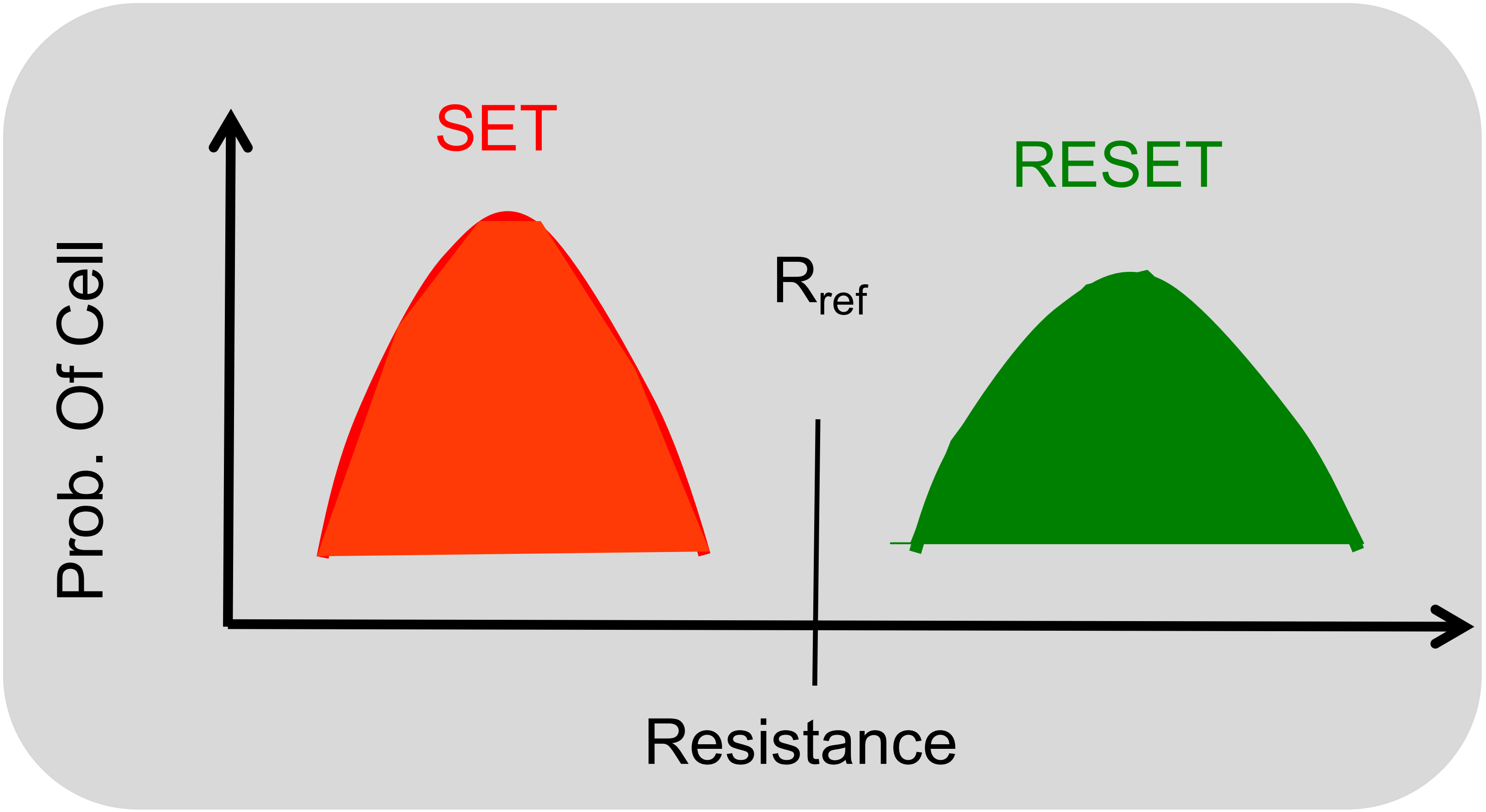


Reduce time to sense by lowering the RC time

EFFECT OF SENSING EARLIER



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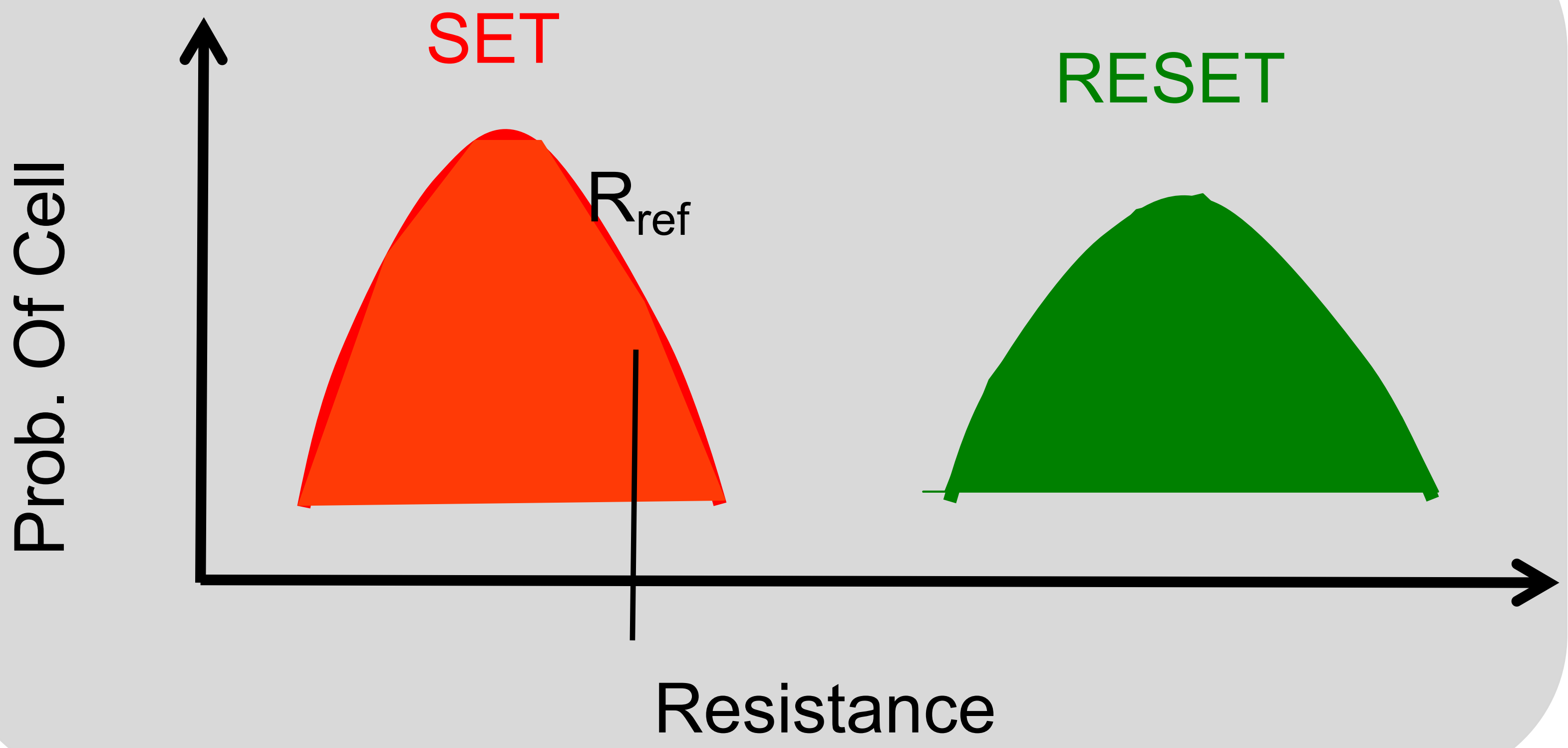

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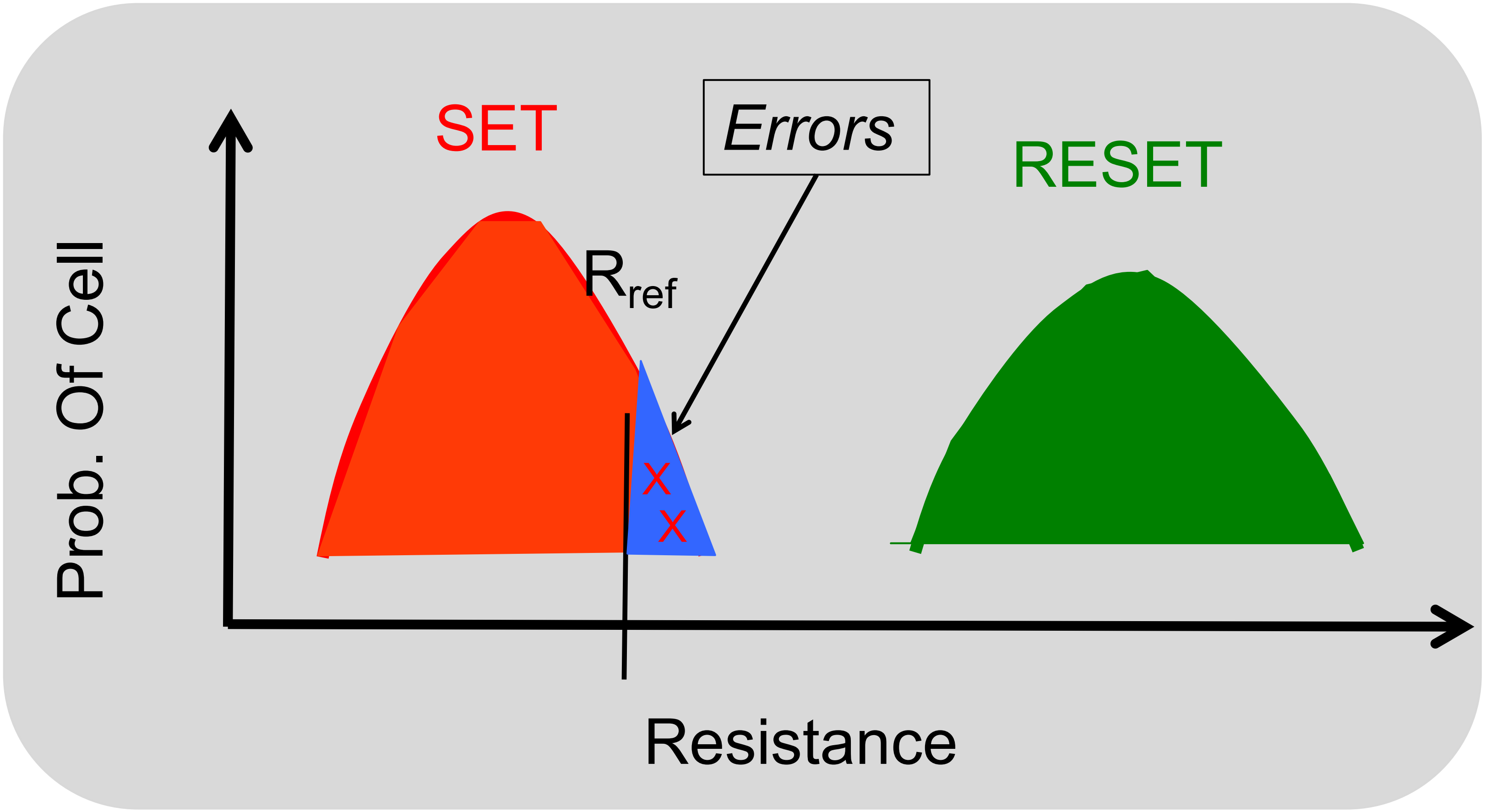

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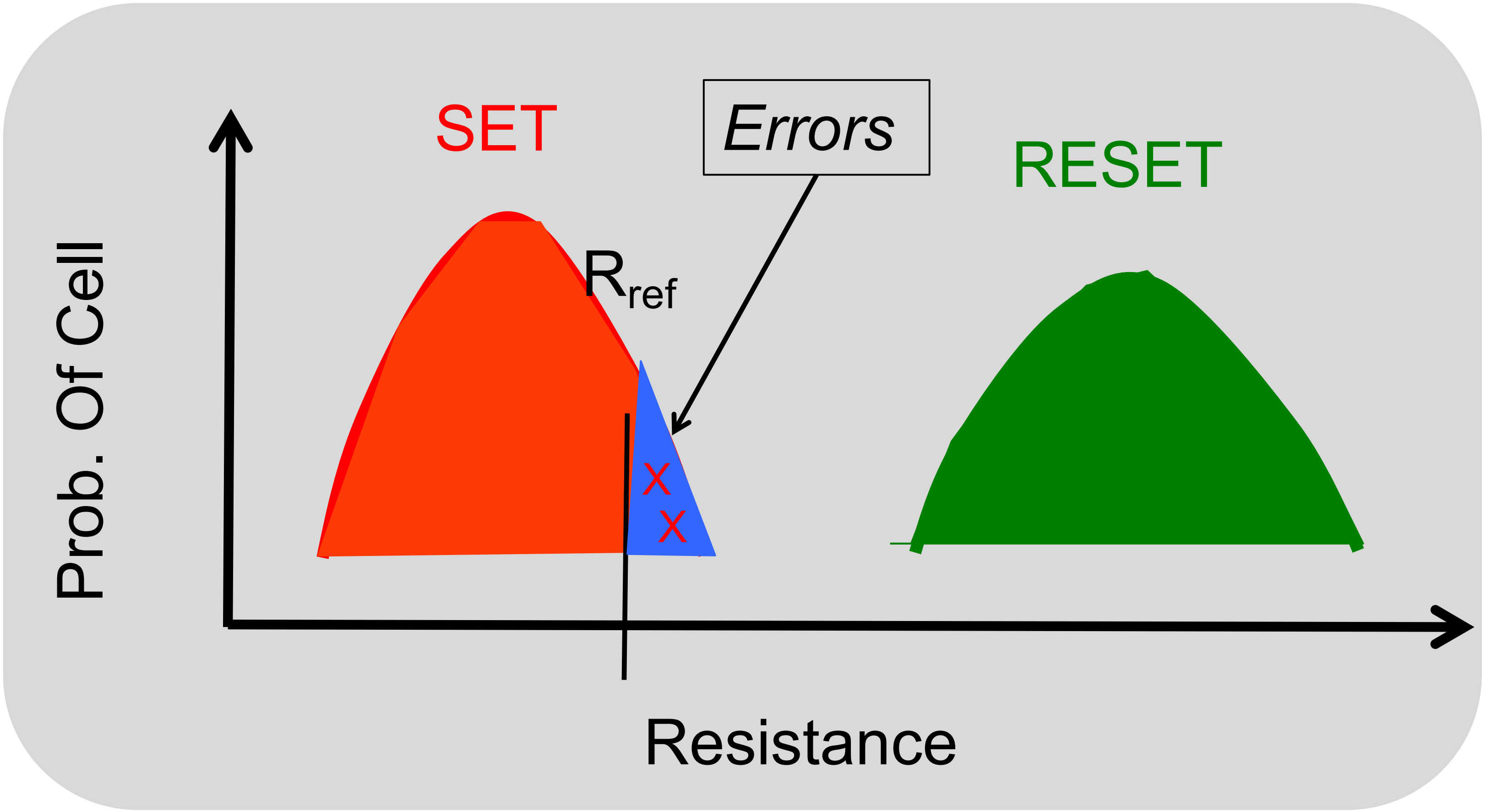
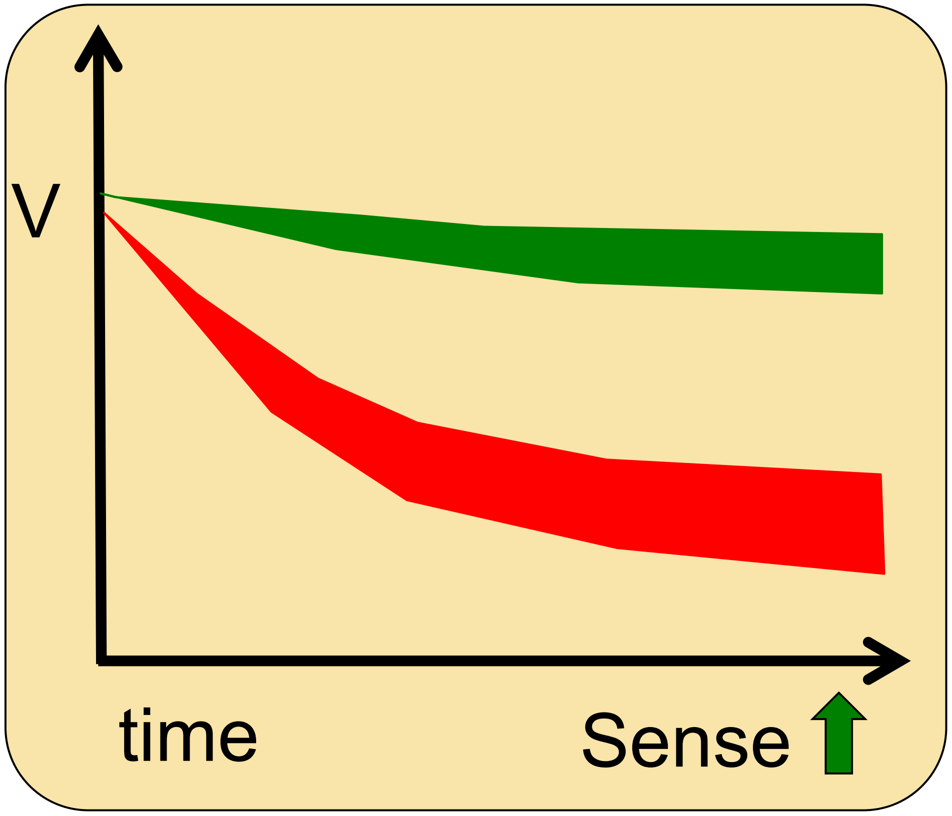


Sensing earlier causes errors while reading higher resistances

REDUCE READ LATENCY: HIGHER VOLTAGE

- Increase bitline voltage more than the provisioned value



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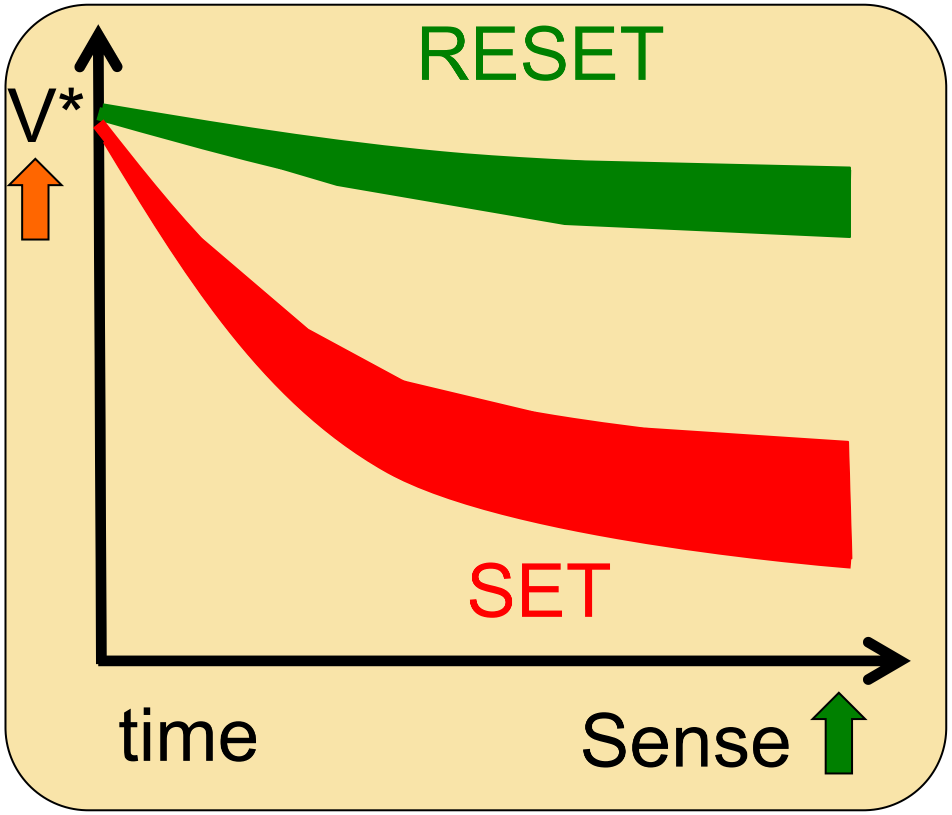

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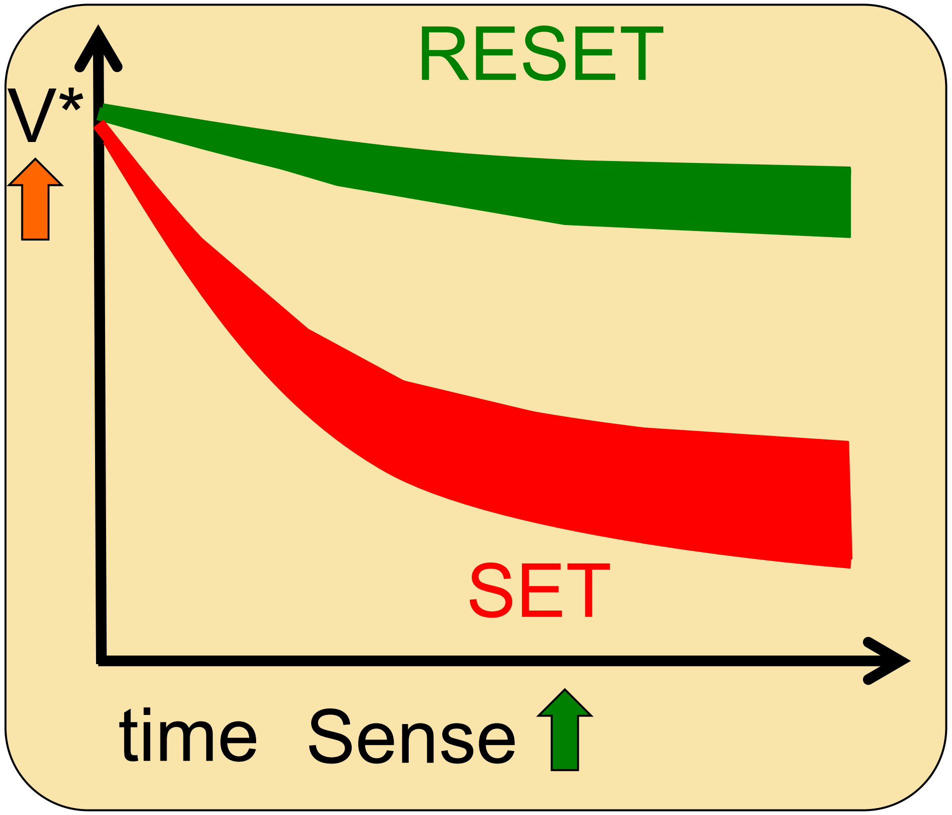

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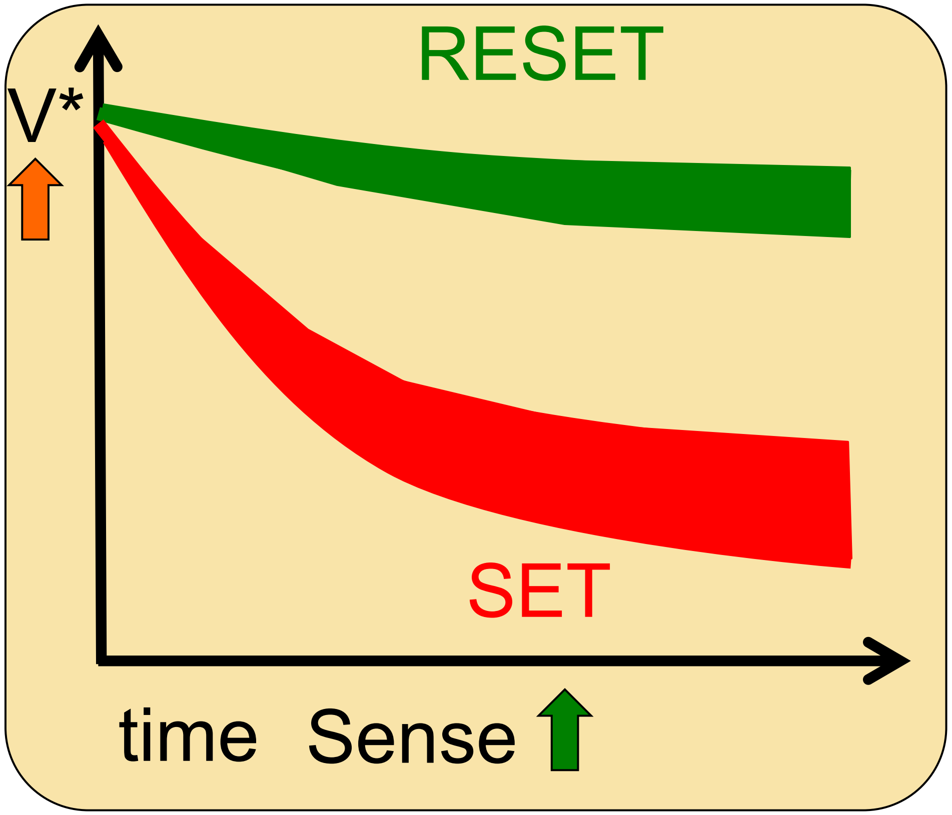
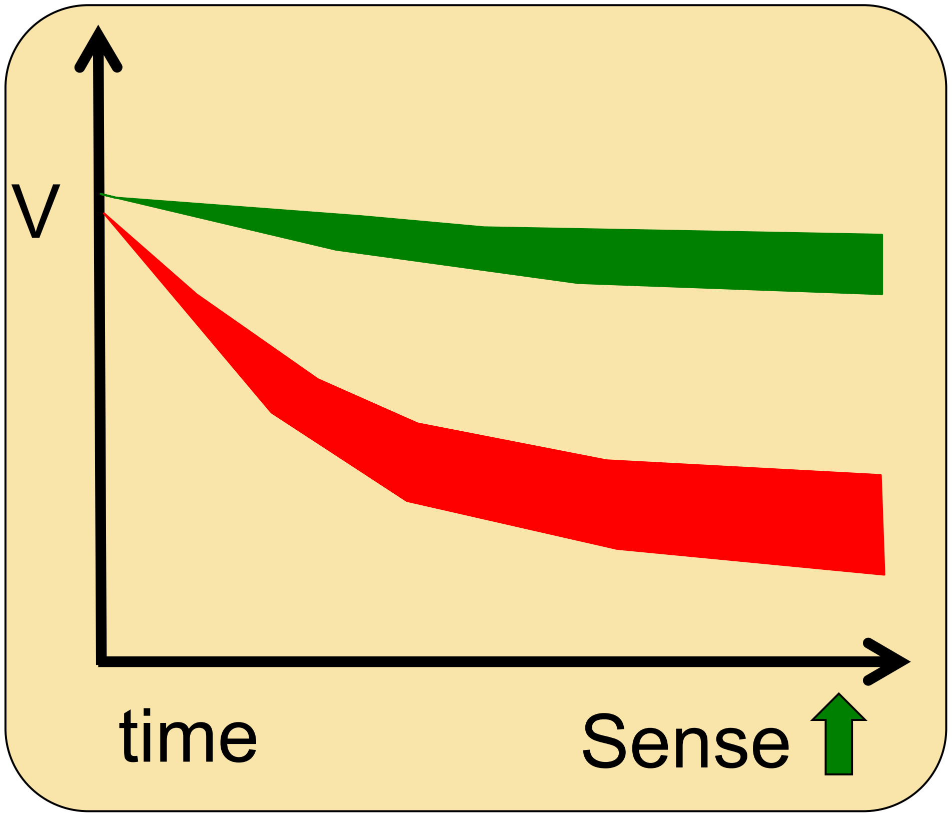
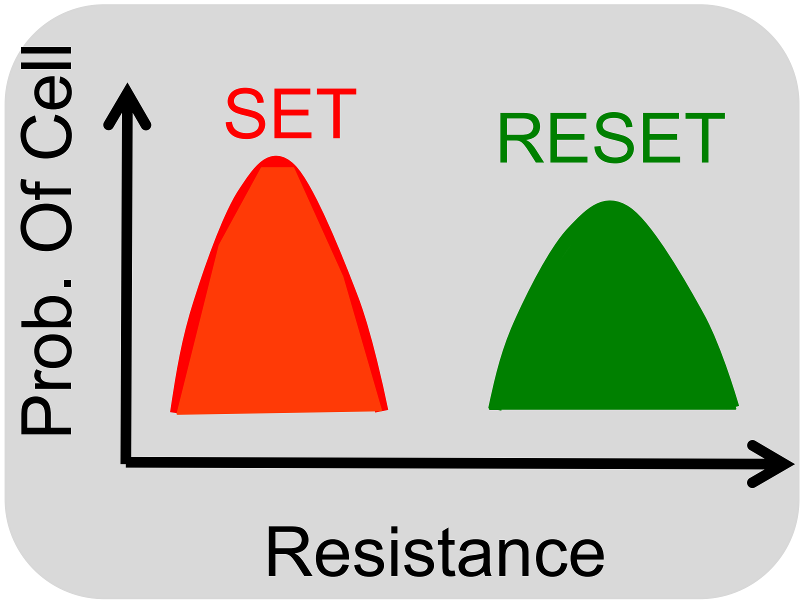


Increase bitline voltage and reduce sensing time

EFFECT OF HIGH BITLINE VOLTAGE





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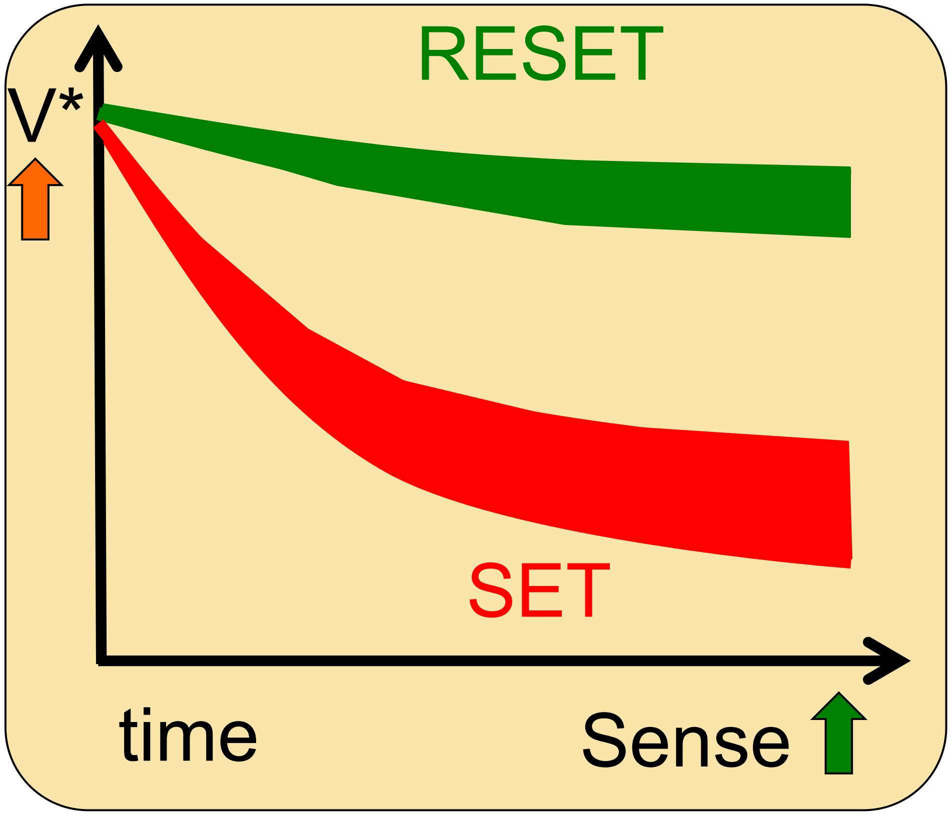

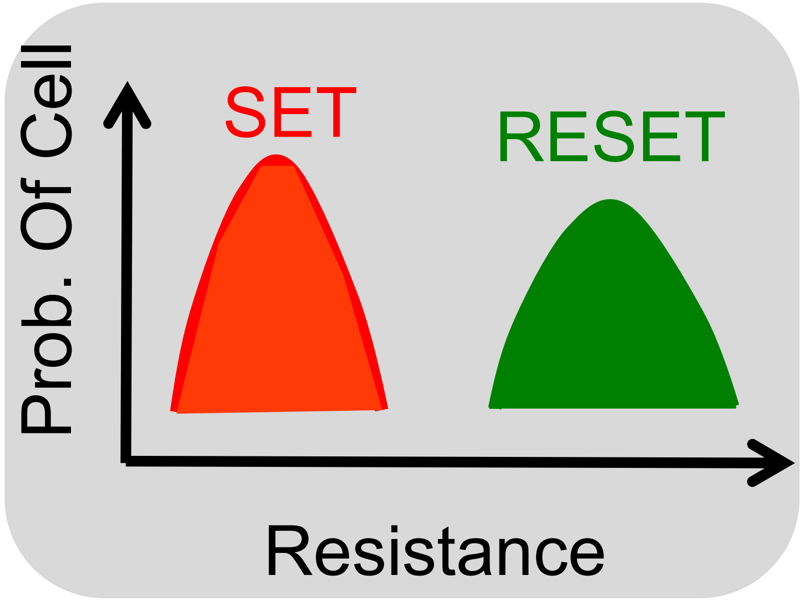

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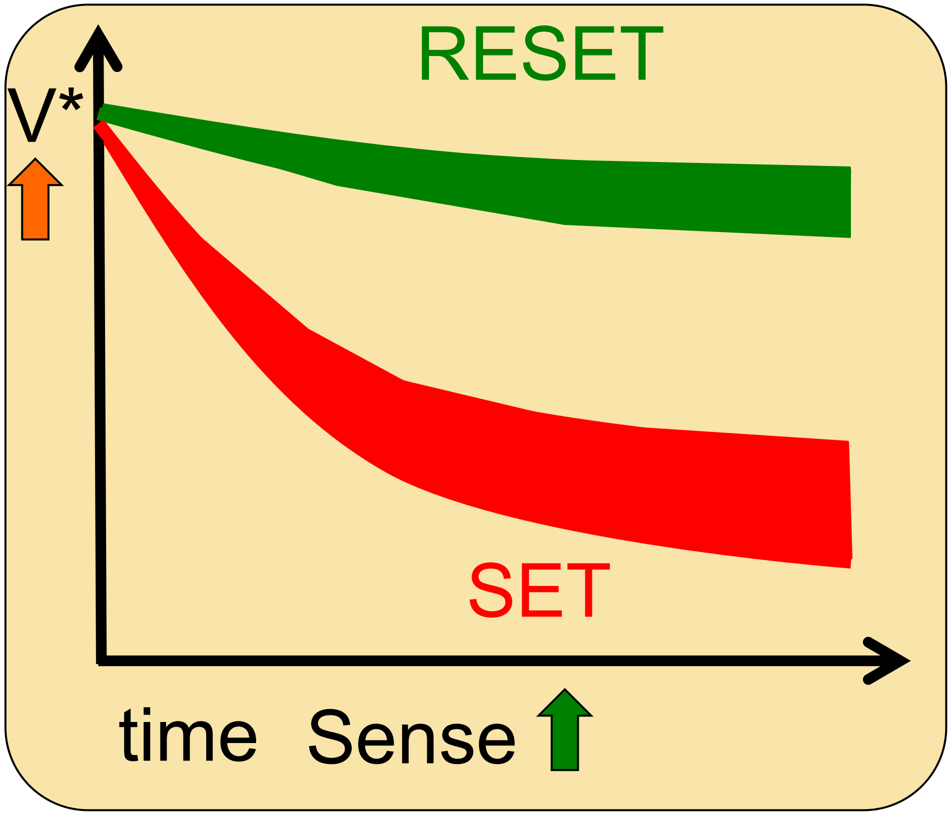

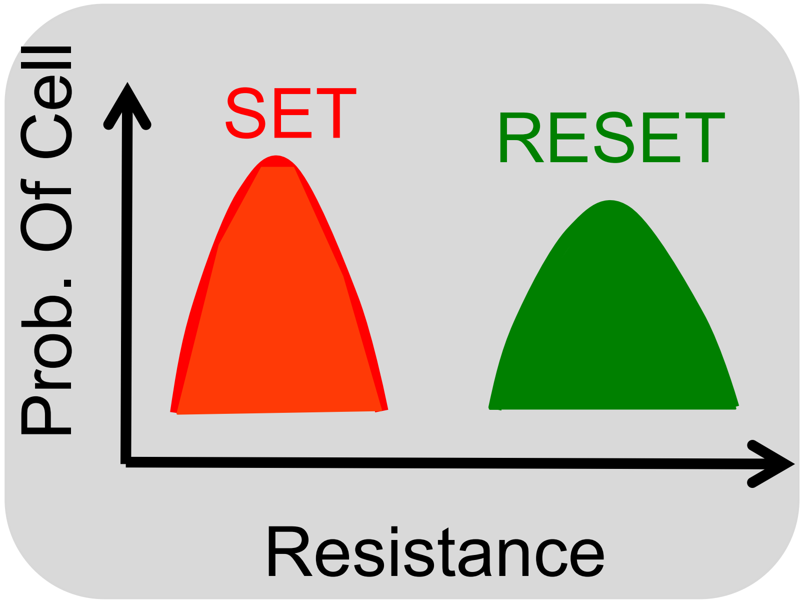

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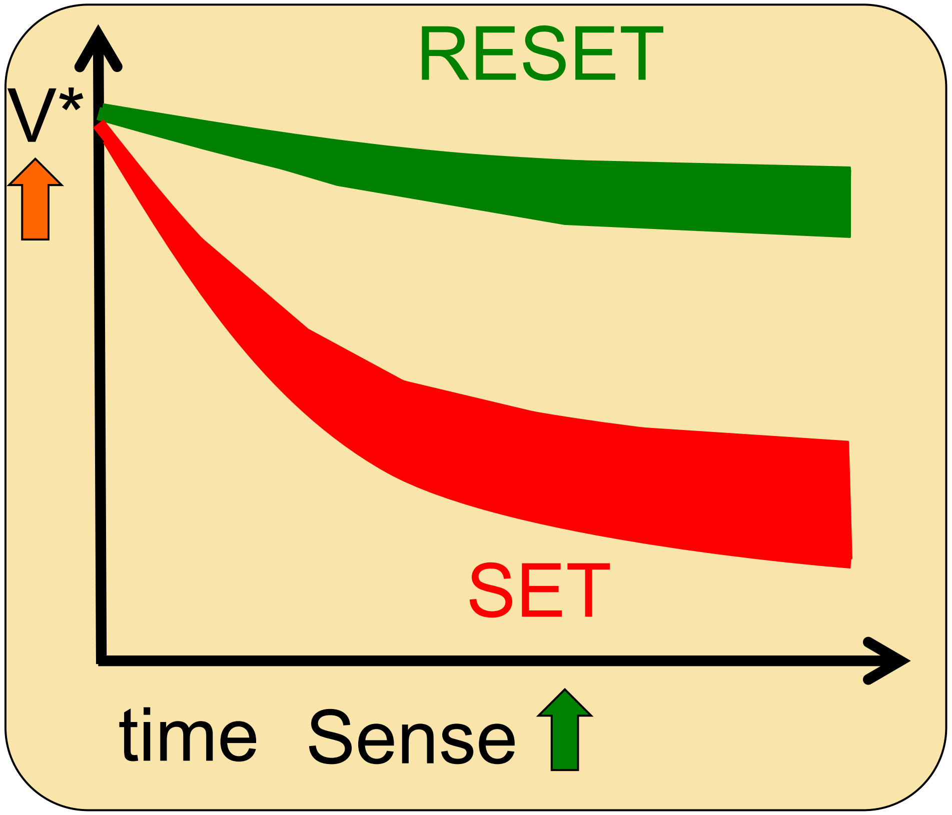

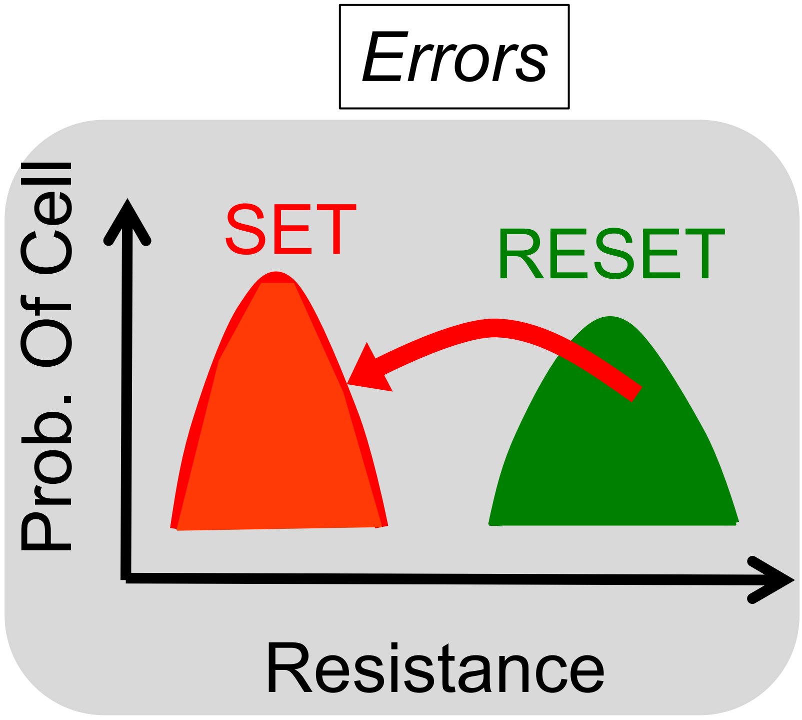

Increasing bitline voltage causes errors

GOAL

Reduce read latency by

1. Exploiting variability in PCM cells → Early Read
2. Higher voltage to read PCM cells → Turbo Read

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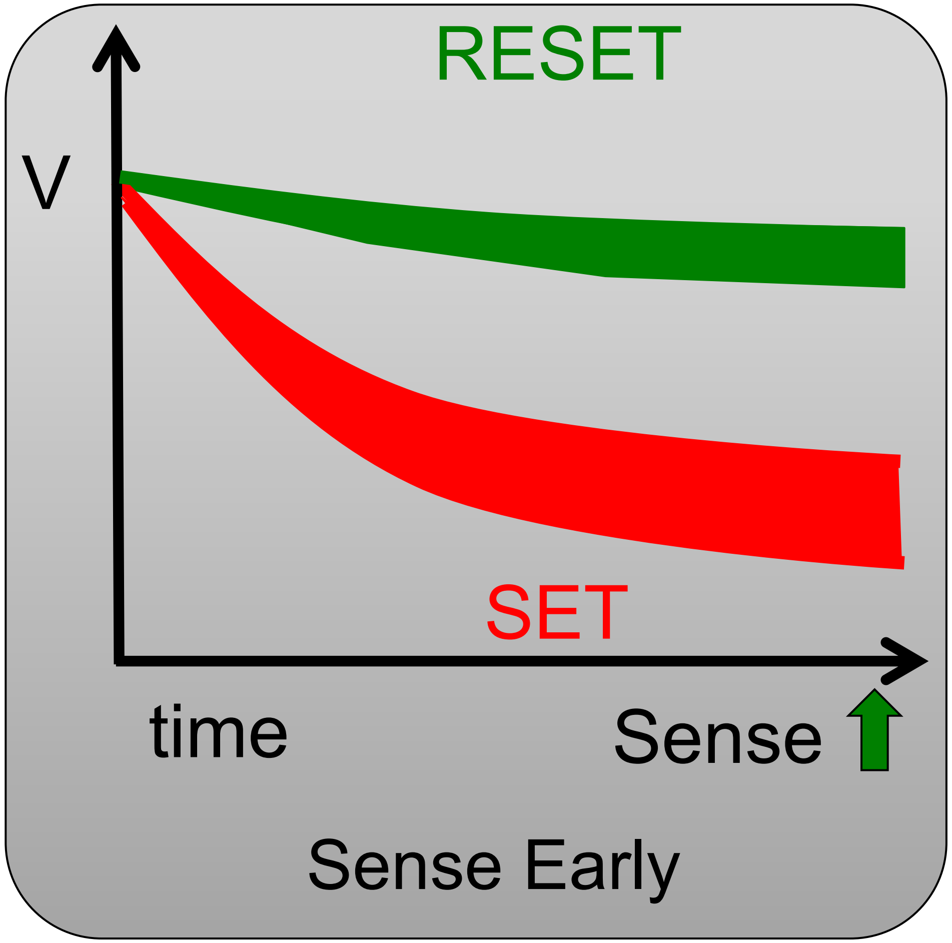

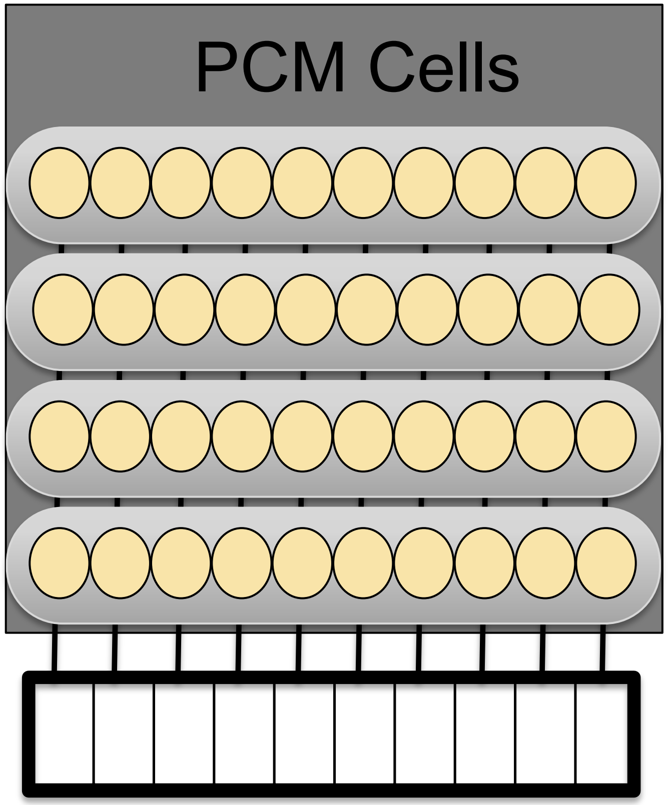

Sense Amplifiers

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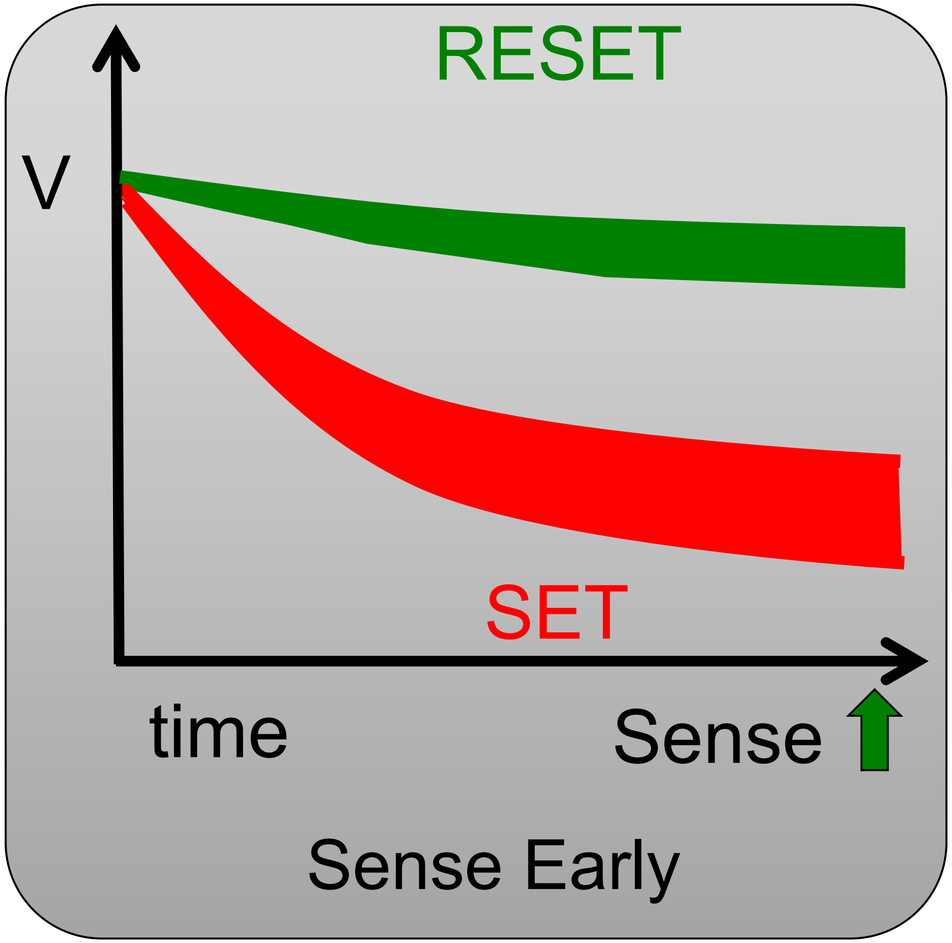

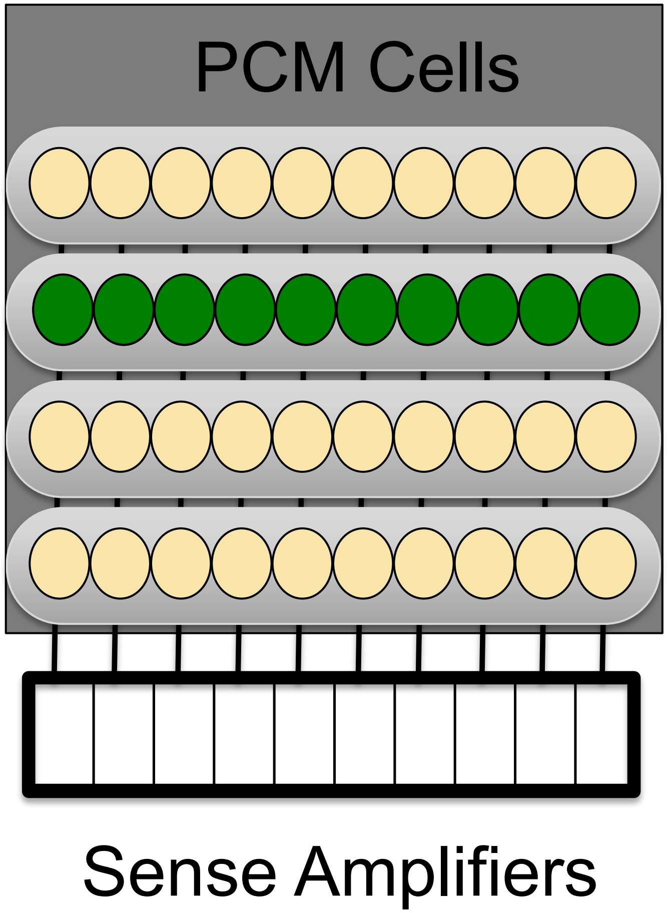

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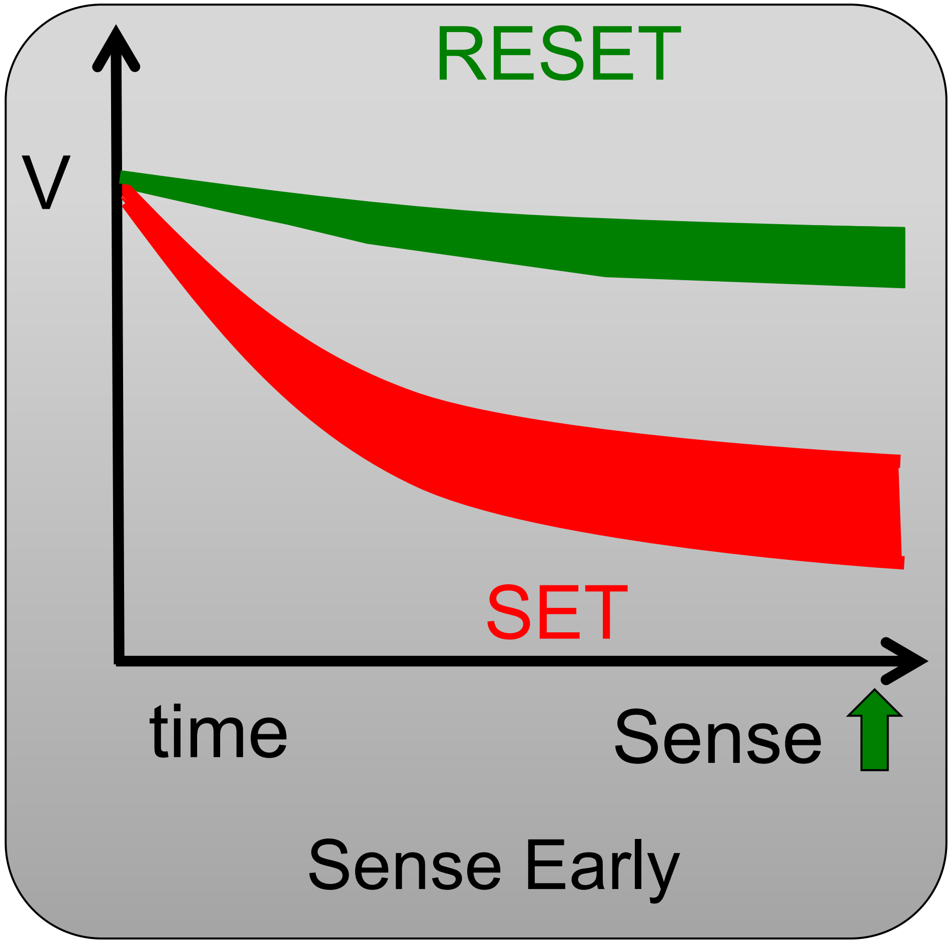

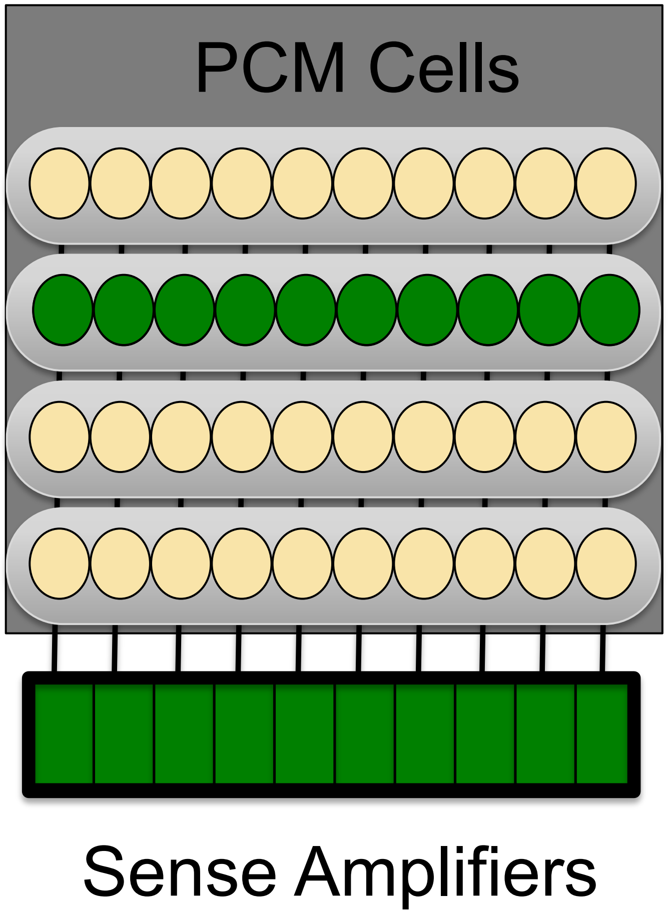

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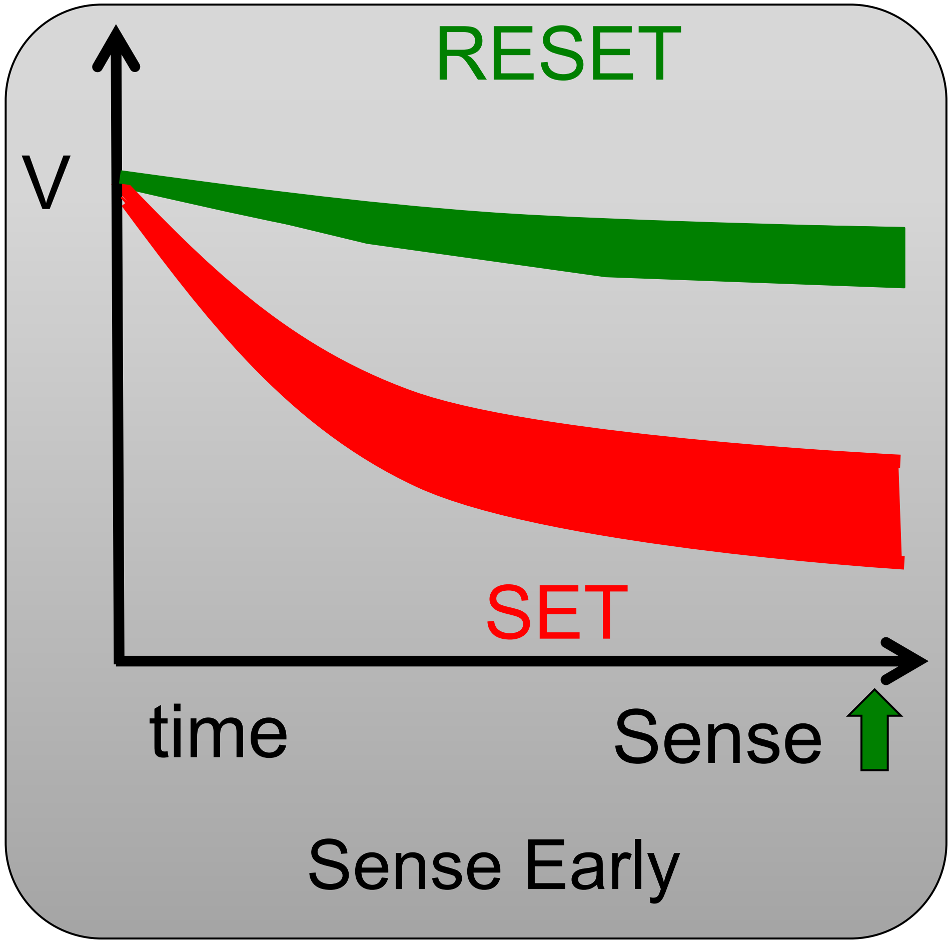

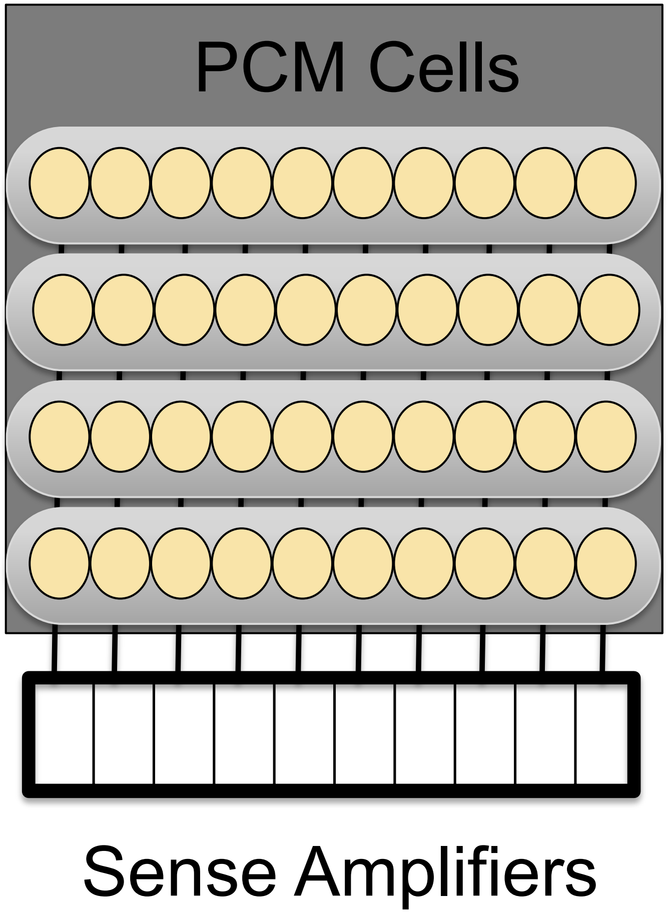

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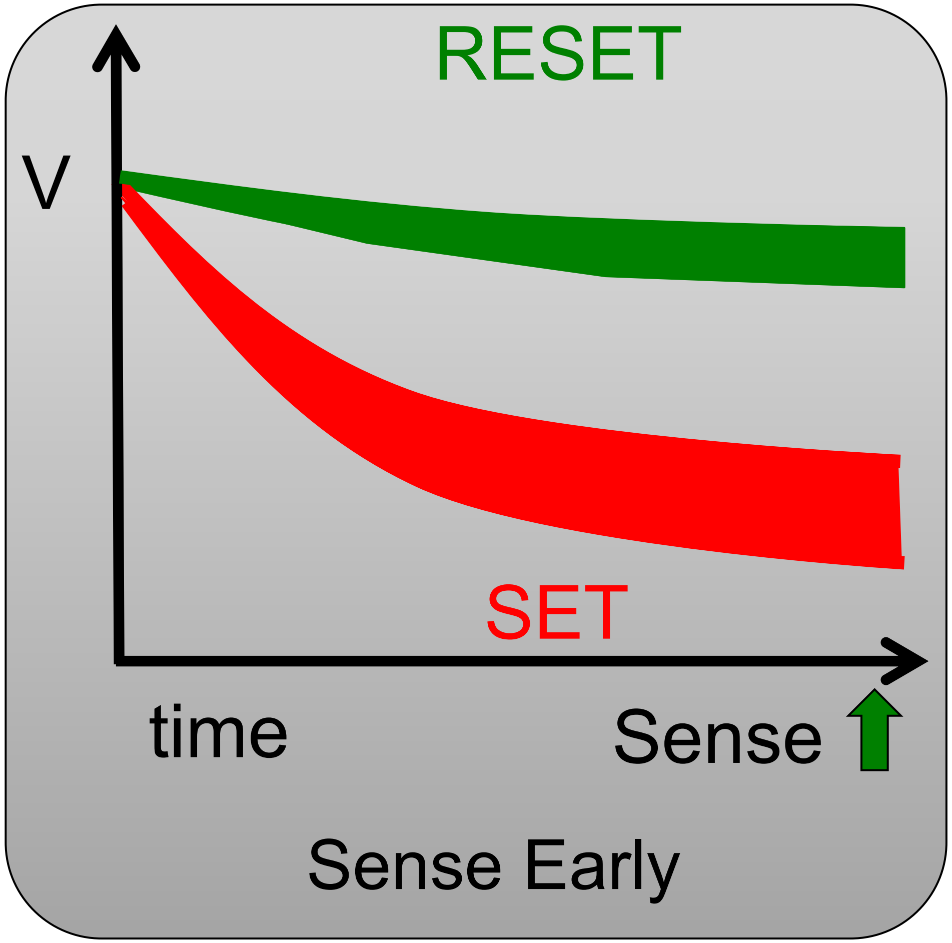

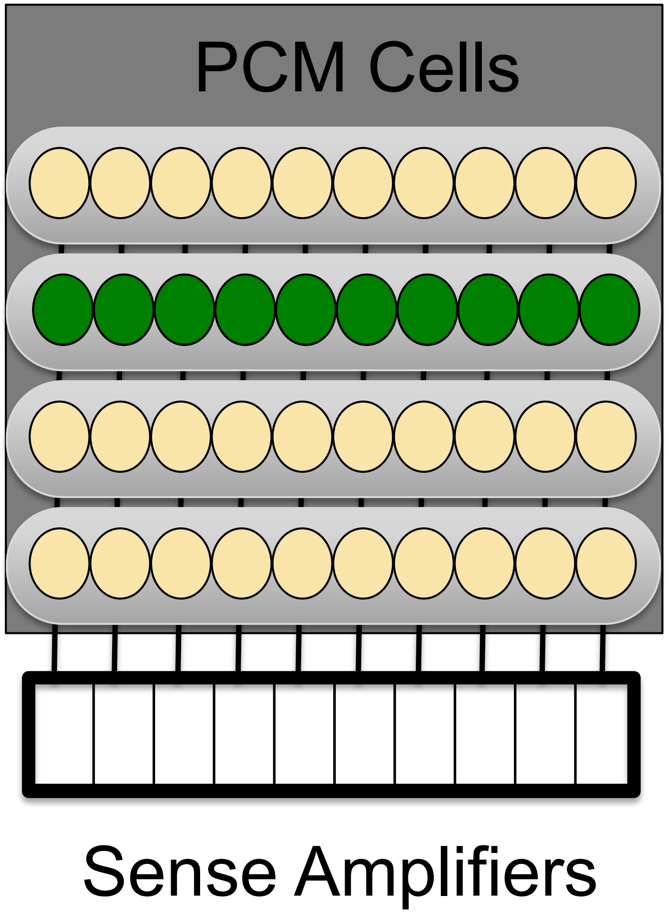

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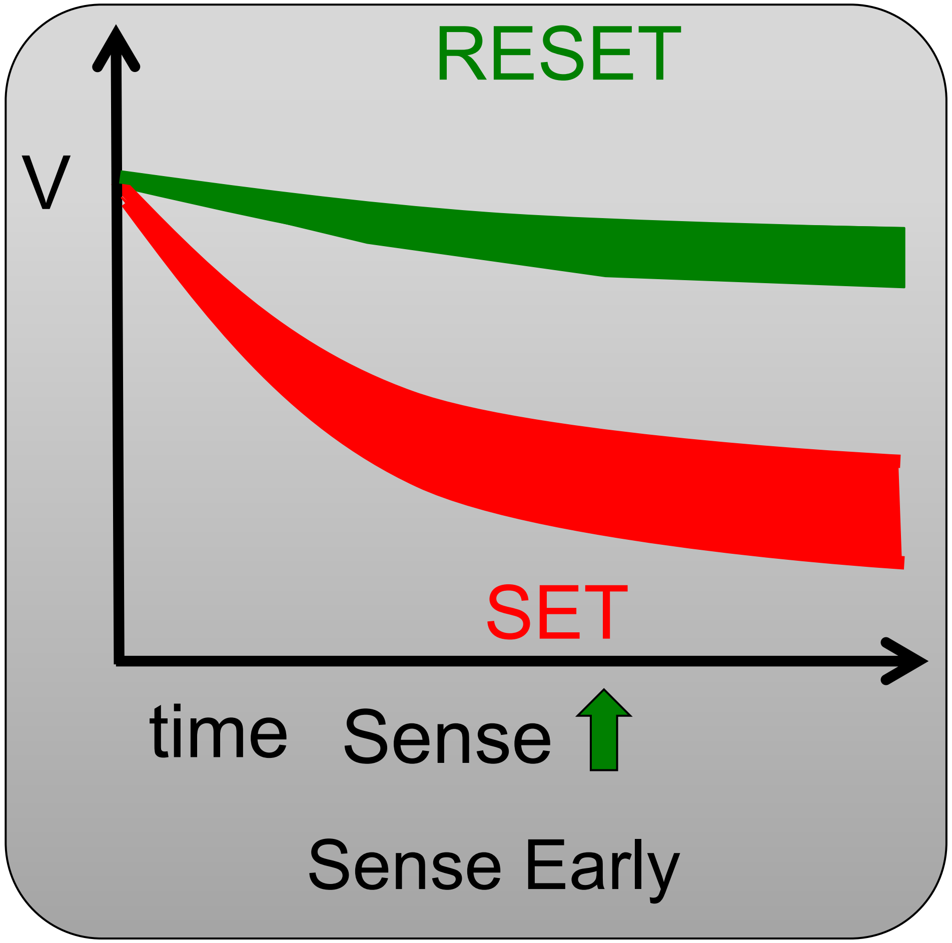

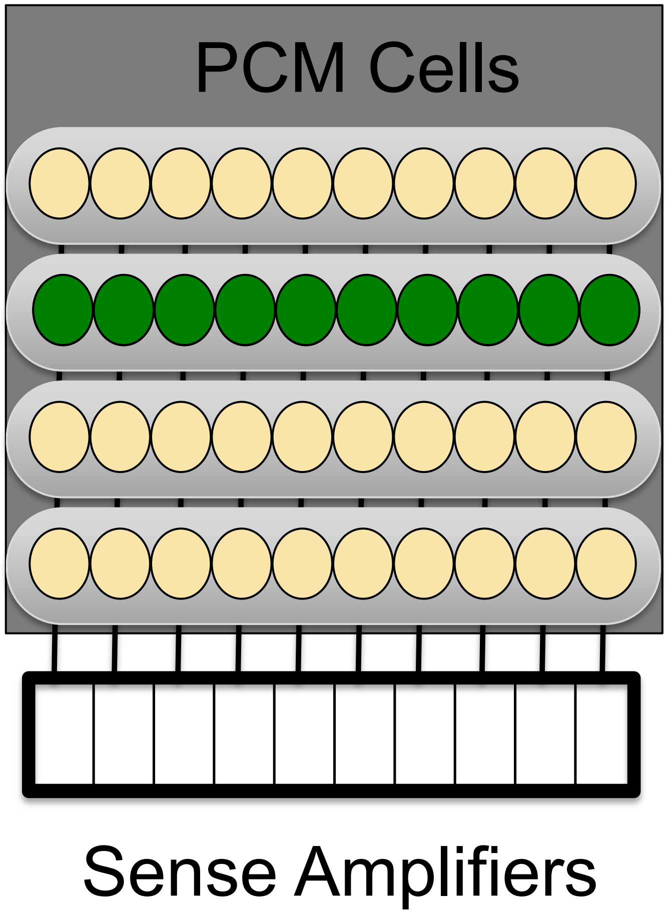

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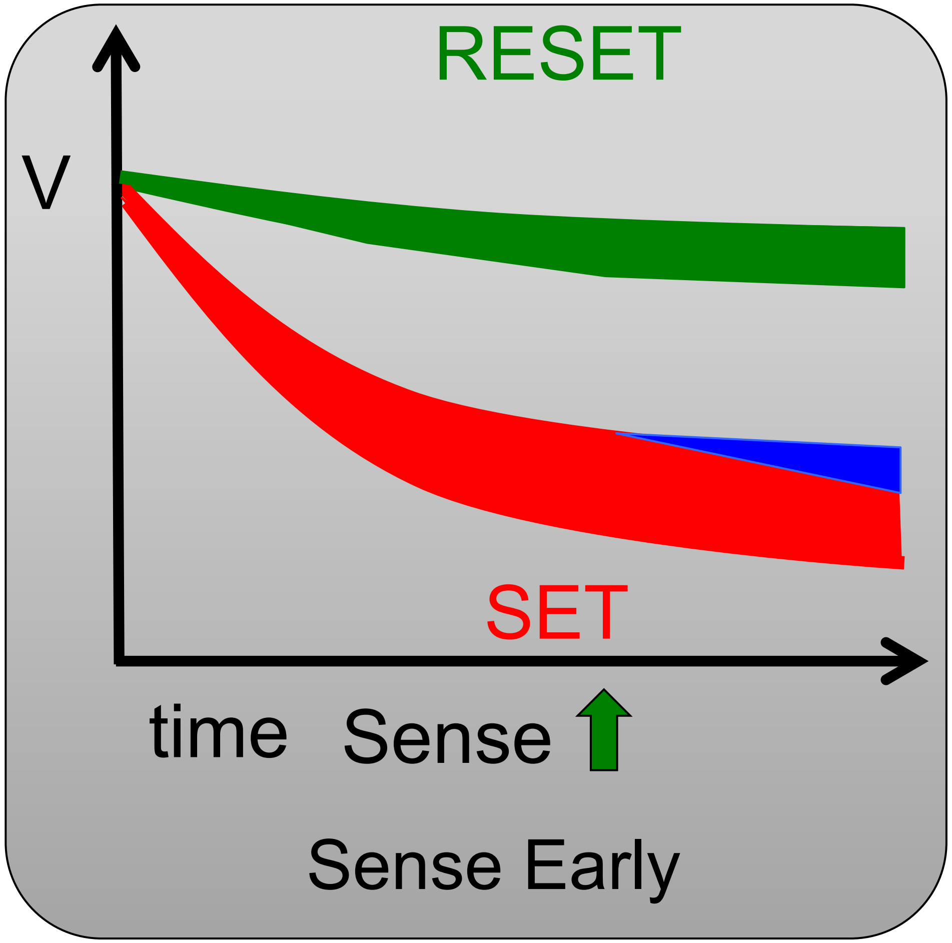

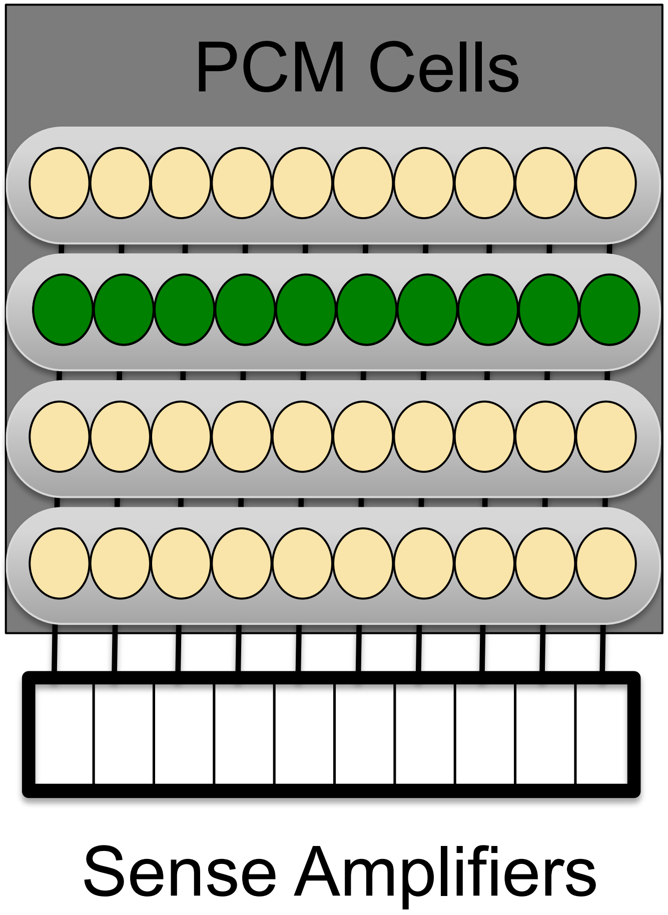

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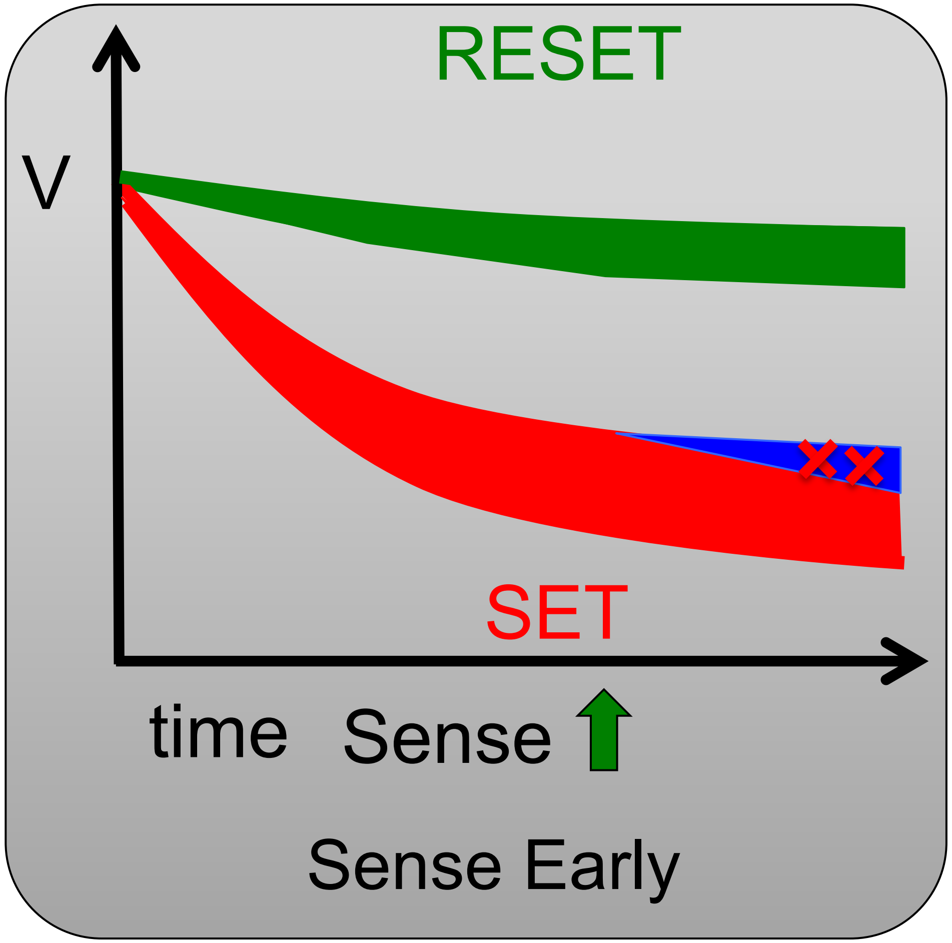

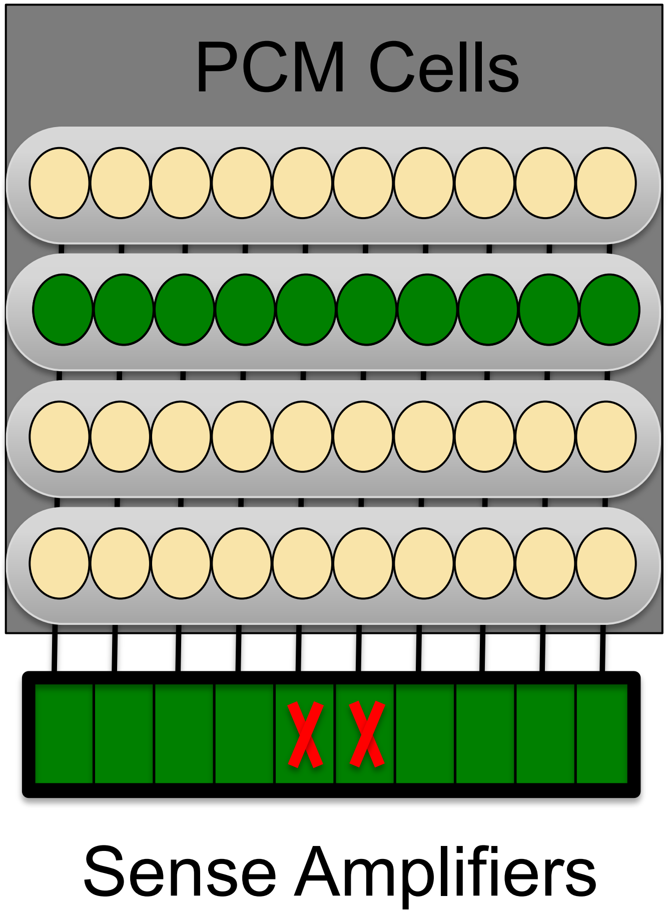

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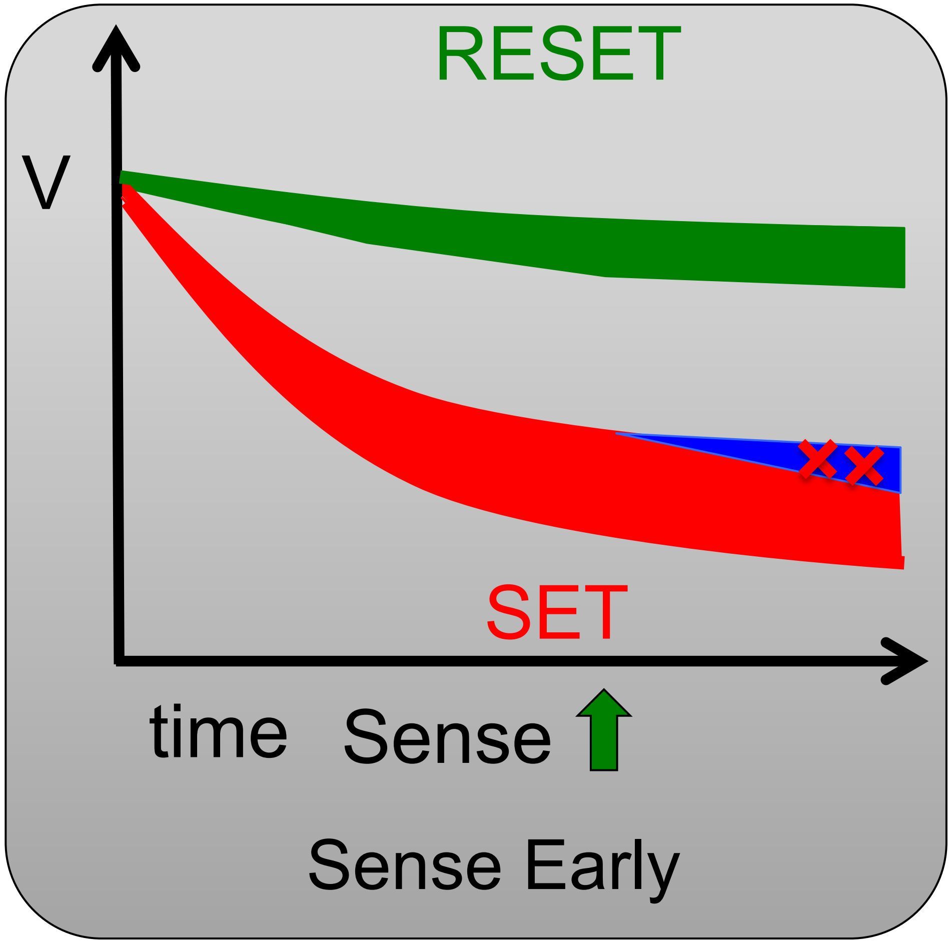
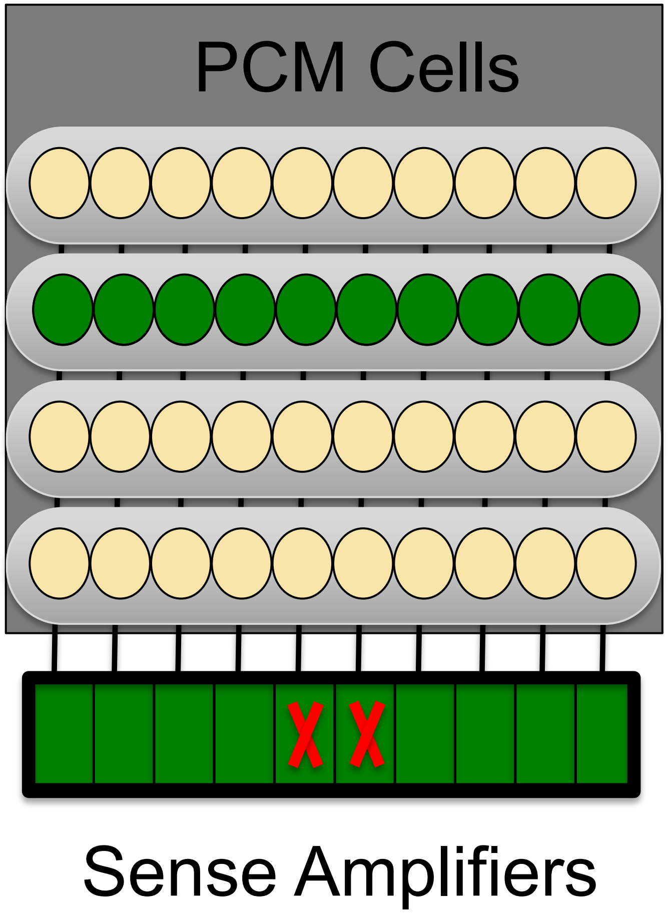
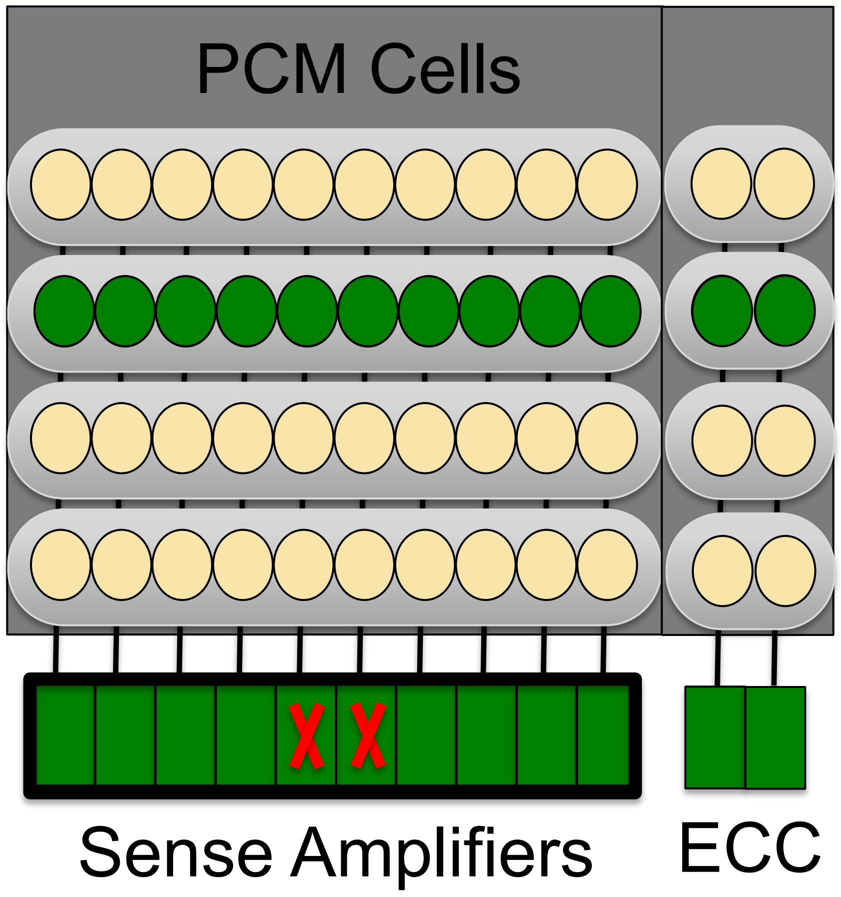




1. Sensing early causes errors in sense amplifiers
2. The cells in PCM substrate have no error

ECC TO CORRECT LATCHING ERRORS



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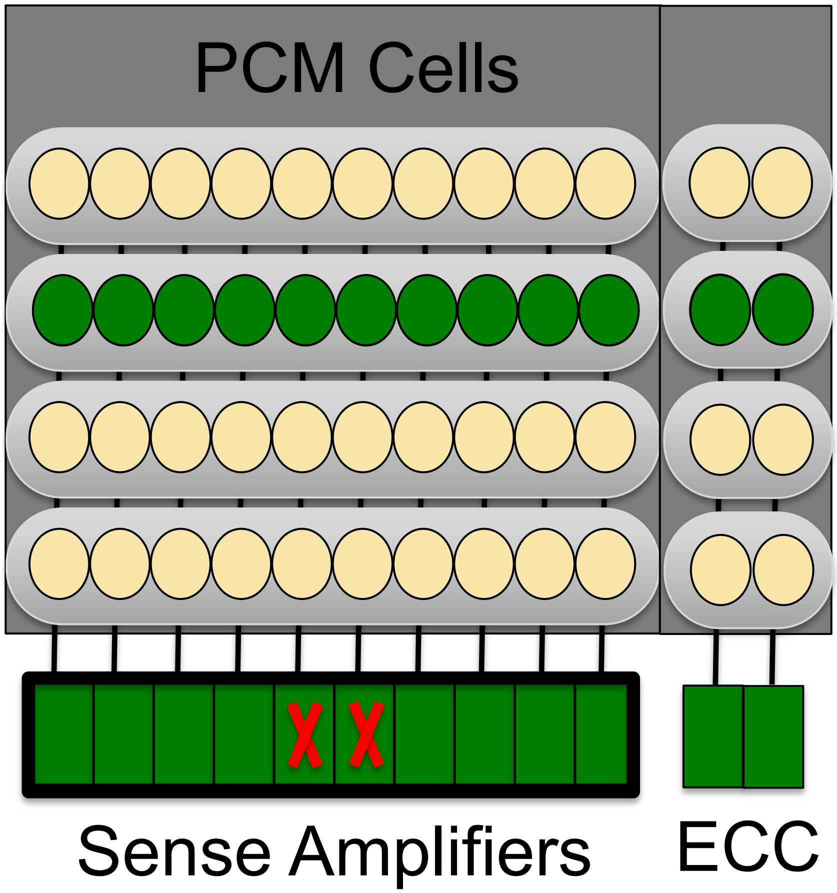
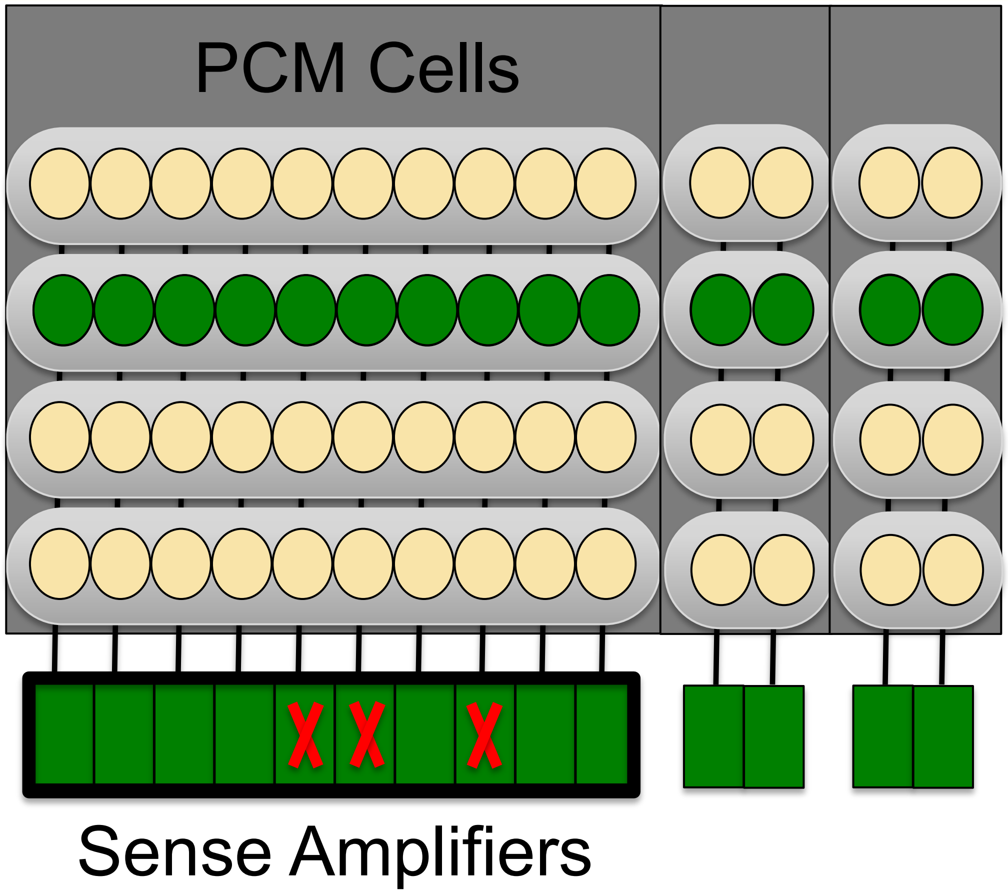


Lower sensing time ➔ more errors ➔ stronger ECC

ECC TO CORRECT LATCHING ERRORS



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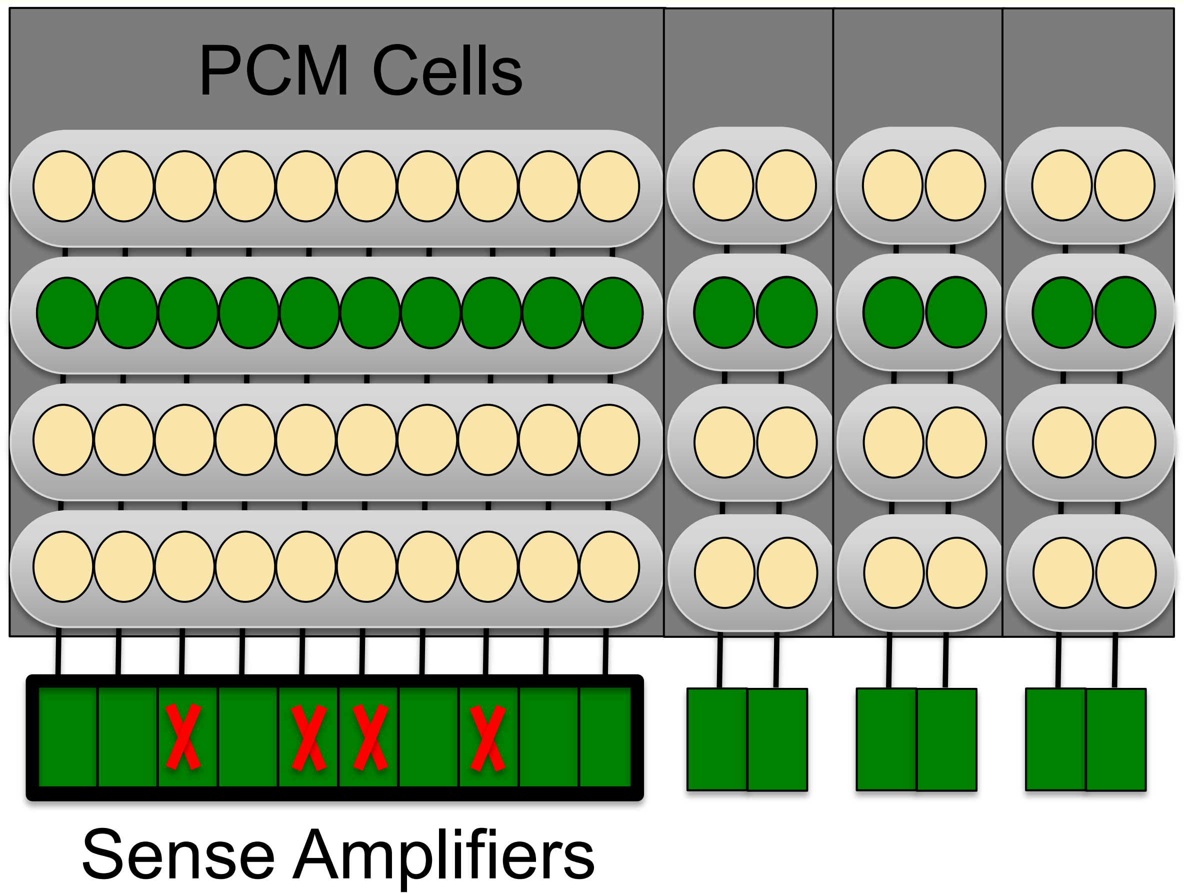

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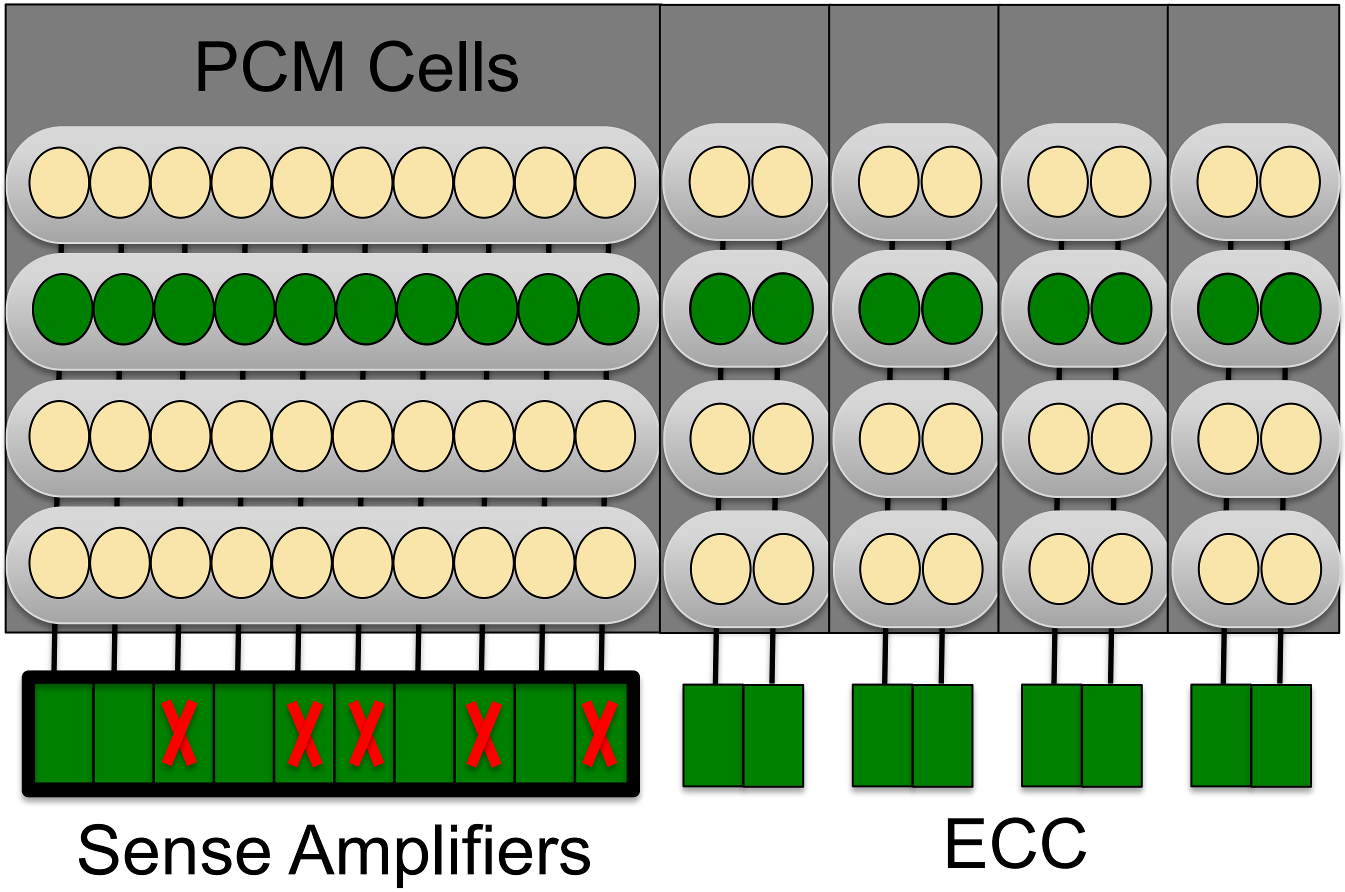

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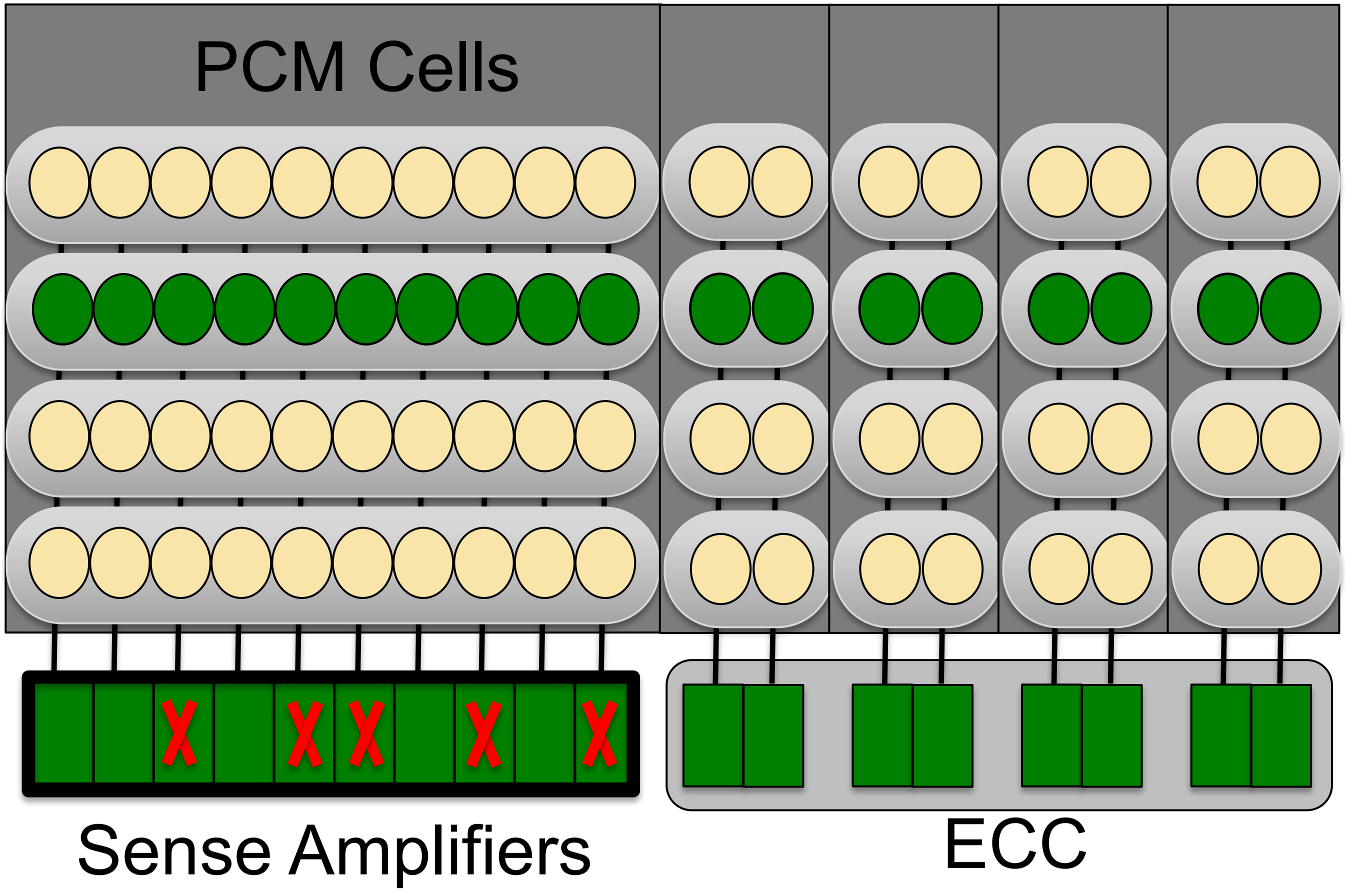
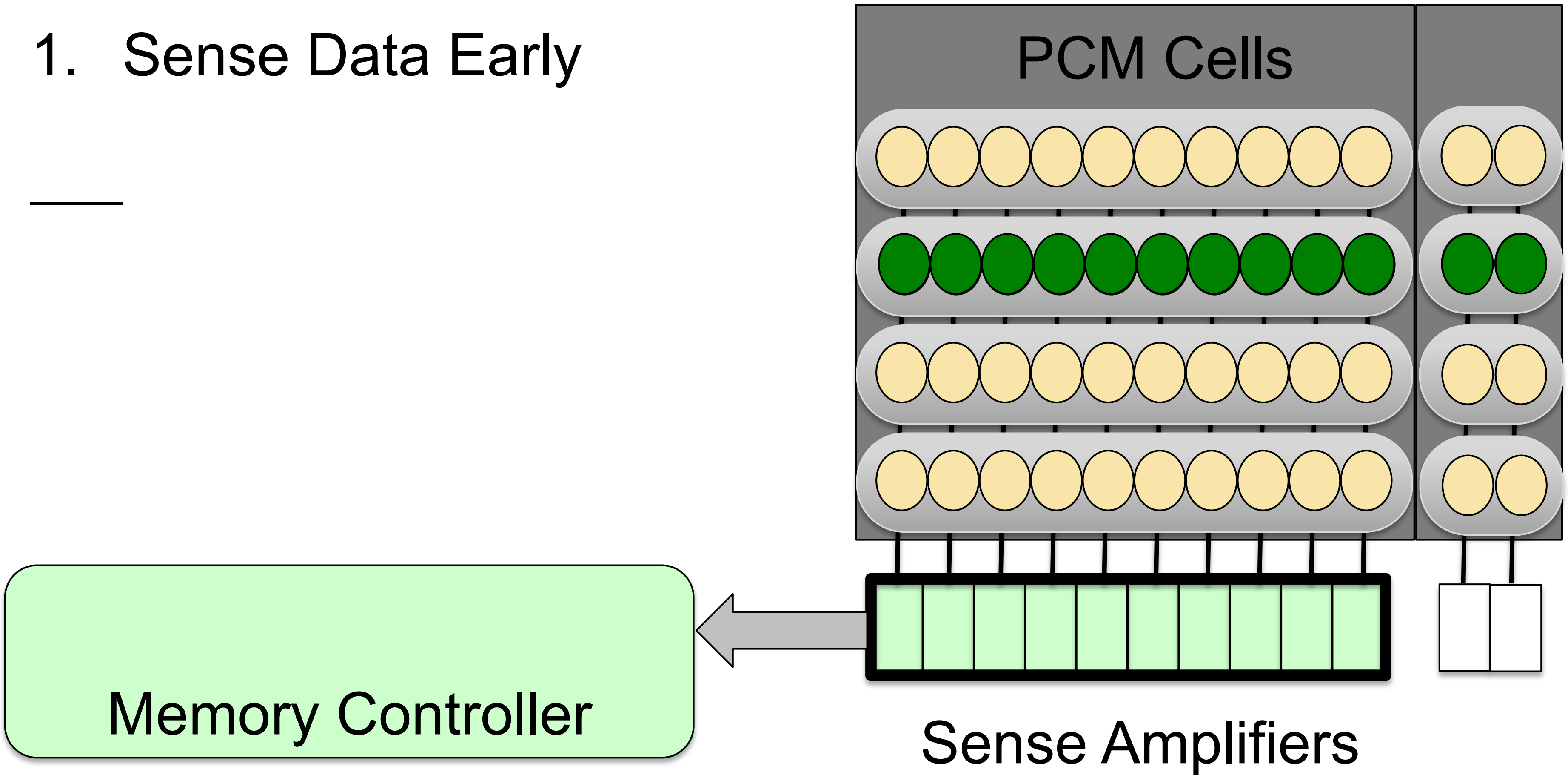


Lower sensing time → more errors → stronger ECC

Strong ECC → Huge area overheads

INSIGHT: USE RETRY FOR CORRECTION

1. Sense Data Early



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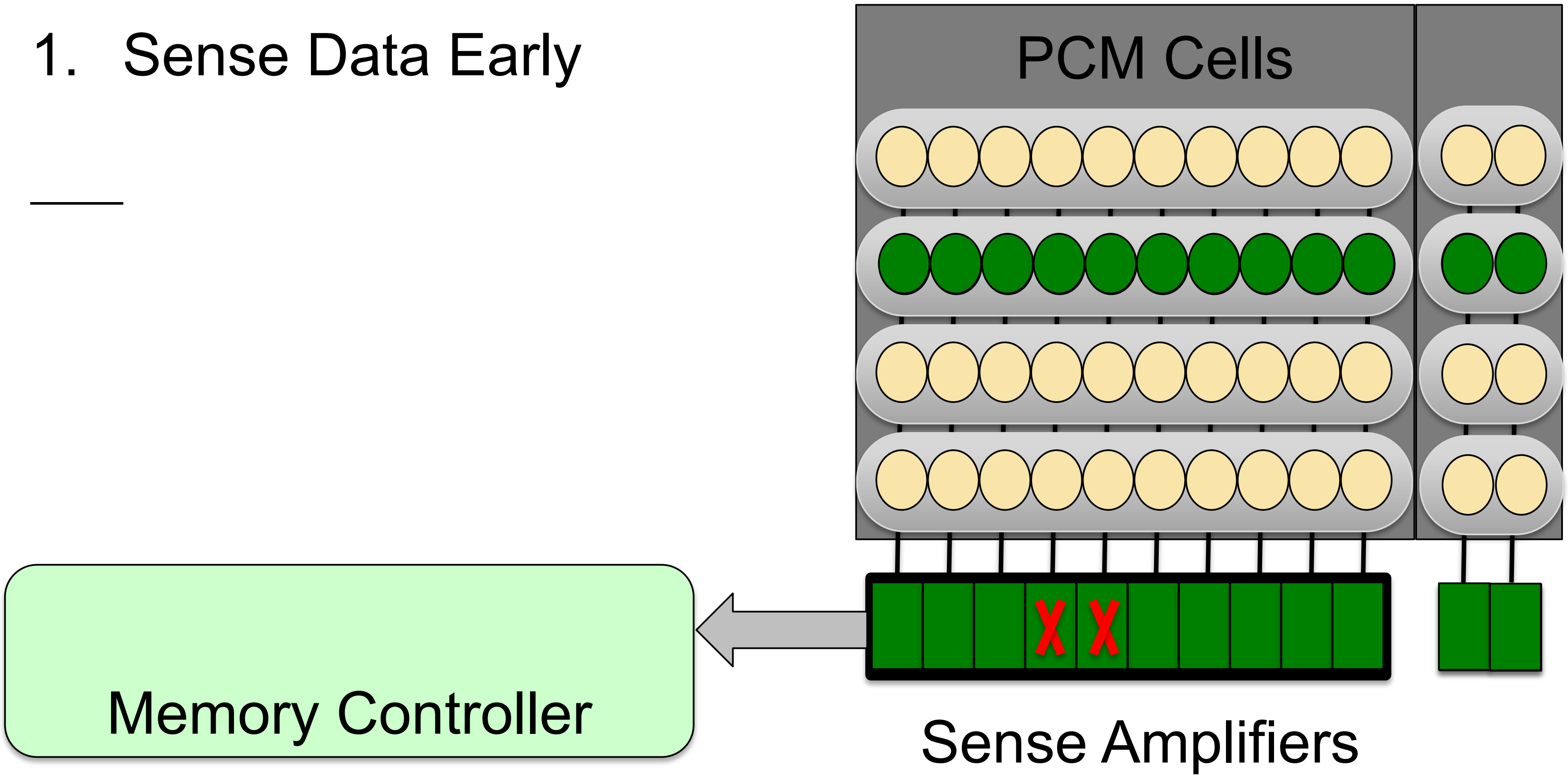
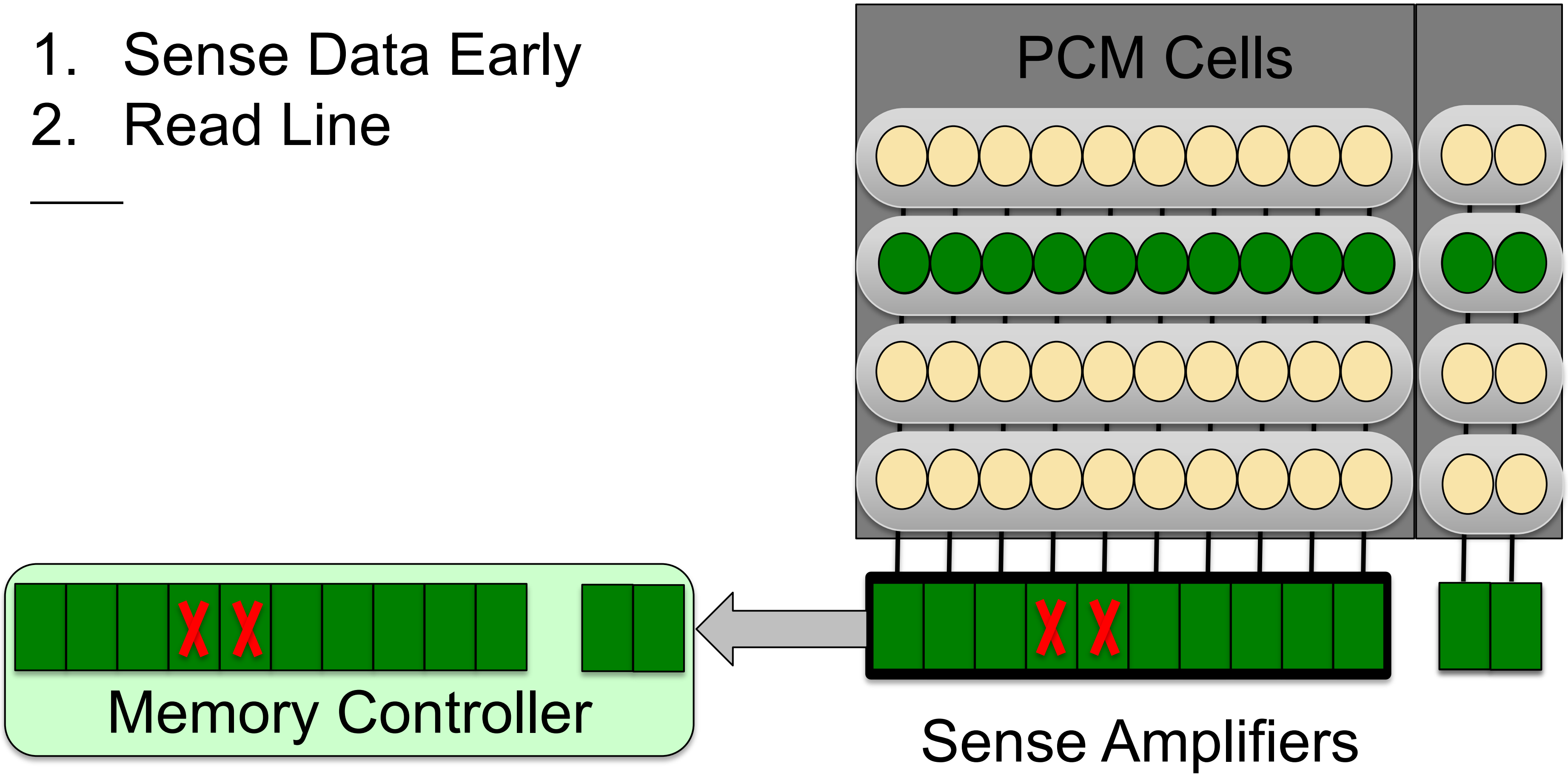


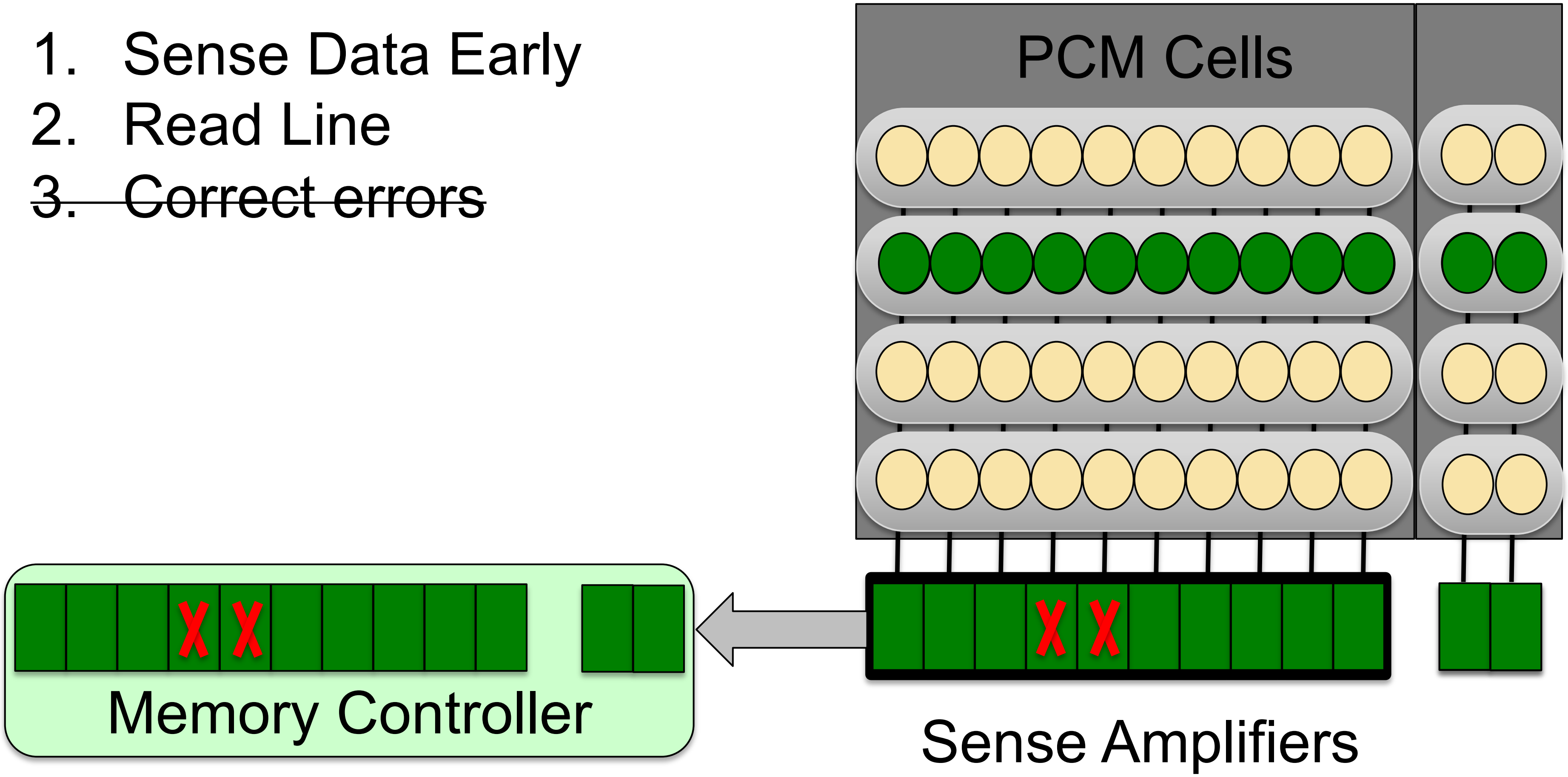
INSIGHT: USE RETRY FOR CORRECTION

1. Sense Data Early
2. Read Line



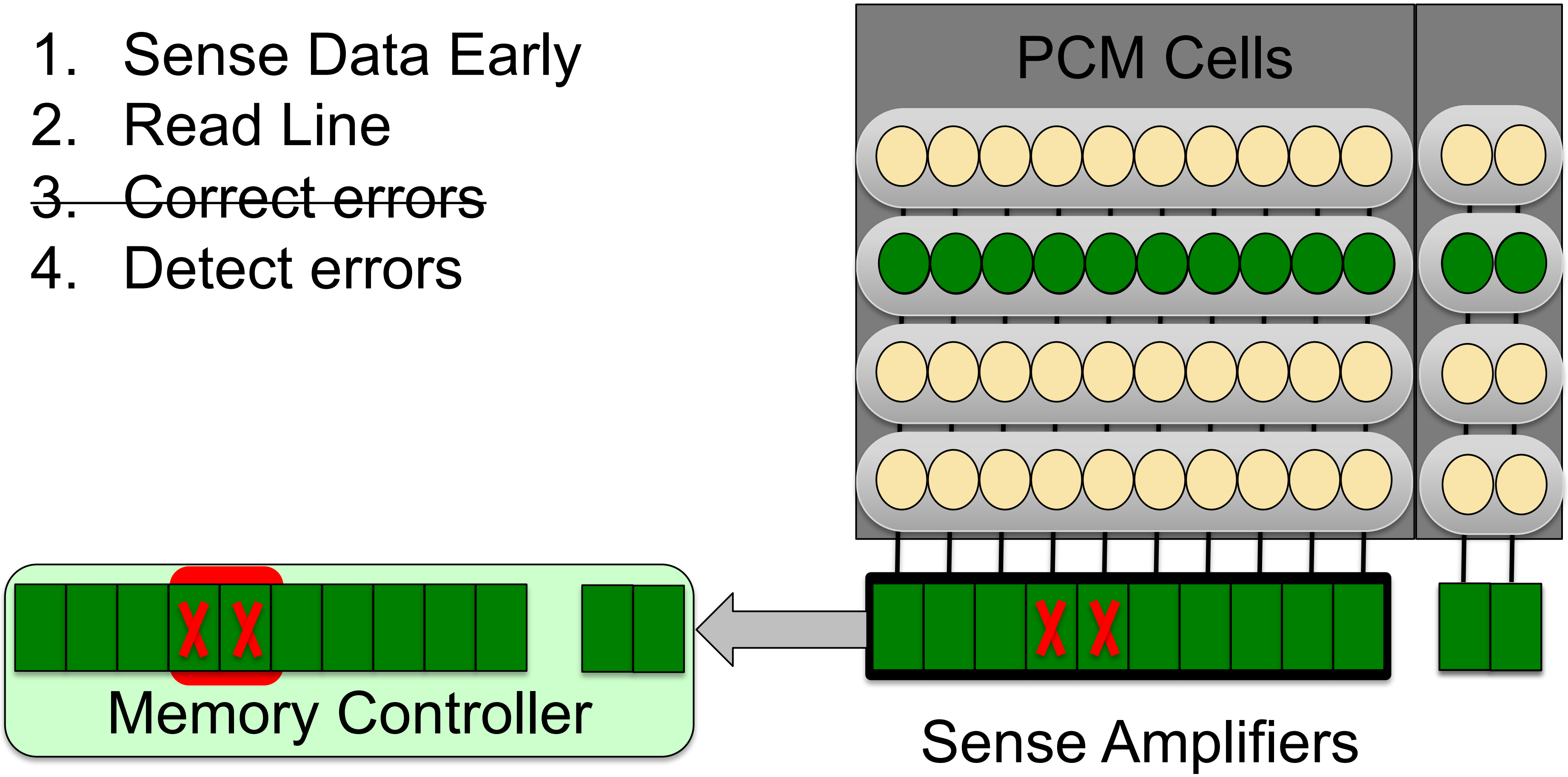
INSIGHT: USE RETRY FOR CORRECTION

1. Sense Data Early
2. Read Line
3. ~~Correct errors~~



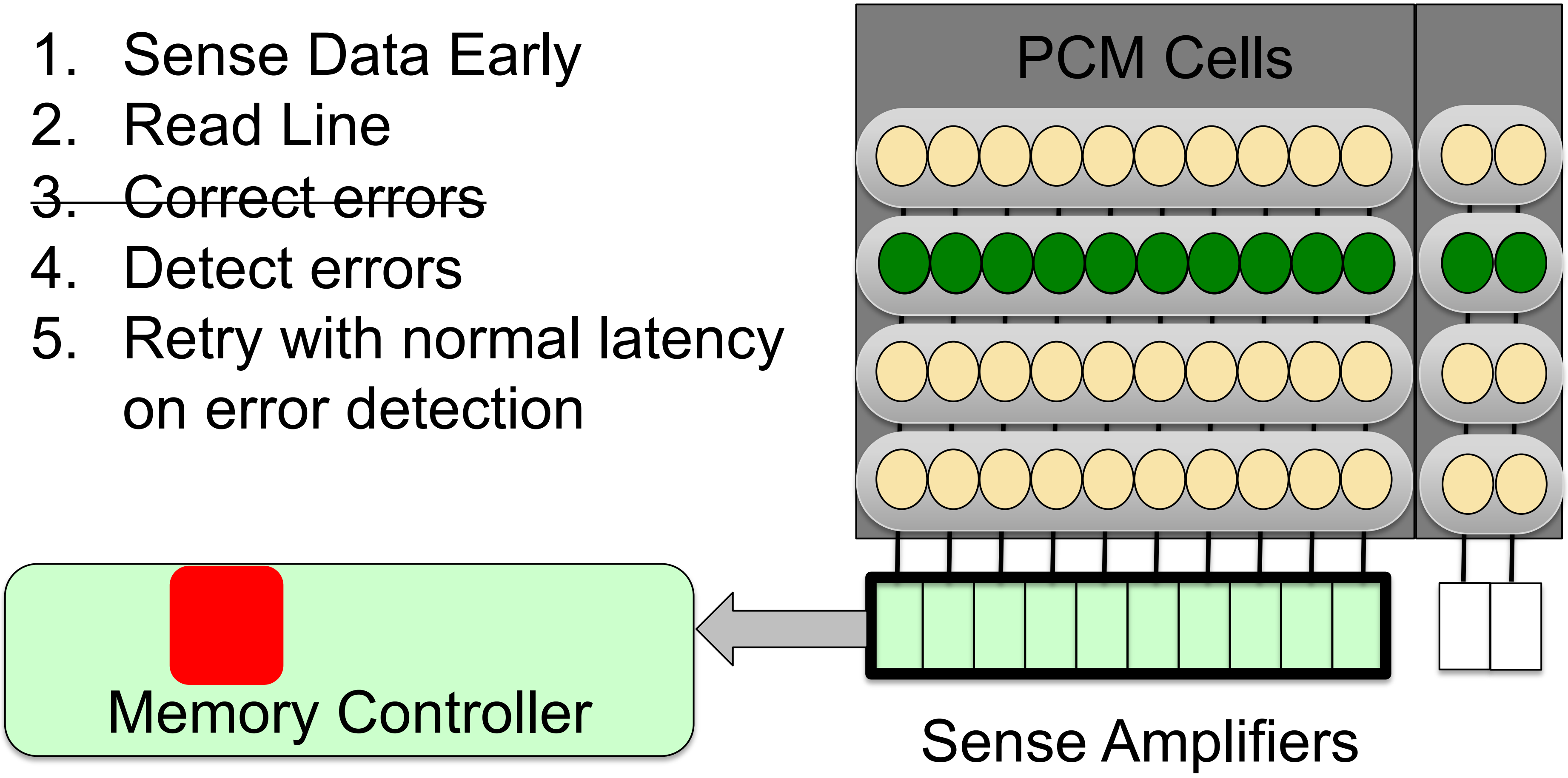
INSIGHT: USE RETRY FOR CORRECTION

1. Sense Data Early
2. Read Line
3. ~~Correct errors~~
4. Detect errors



INSIGHT: USE RETRY FOR CORRECTION

1. Sense Data Early
2. Read Line
3. ~~Correct errors~~
4. Detect errors
5. Retry with normal latency on error detection



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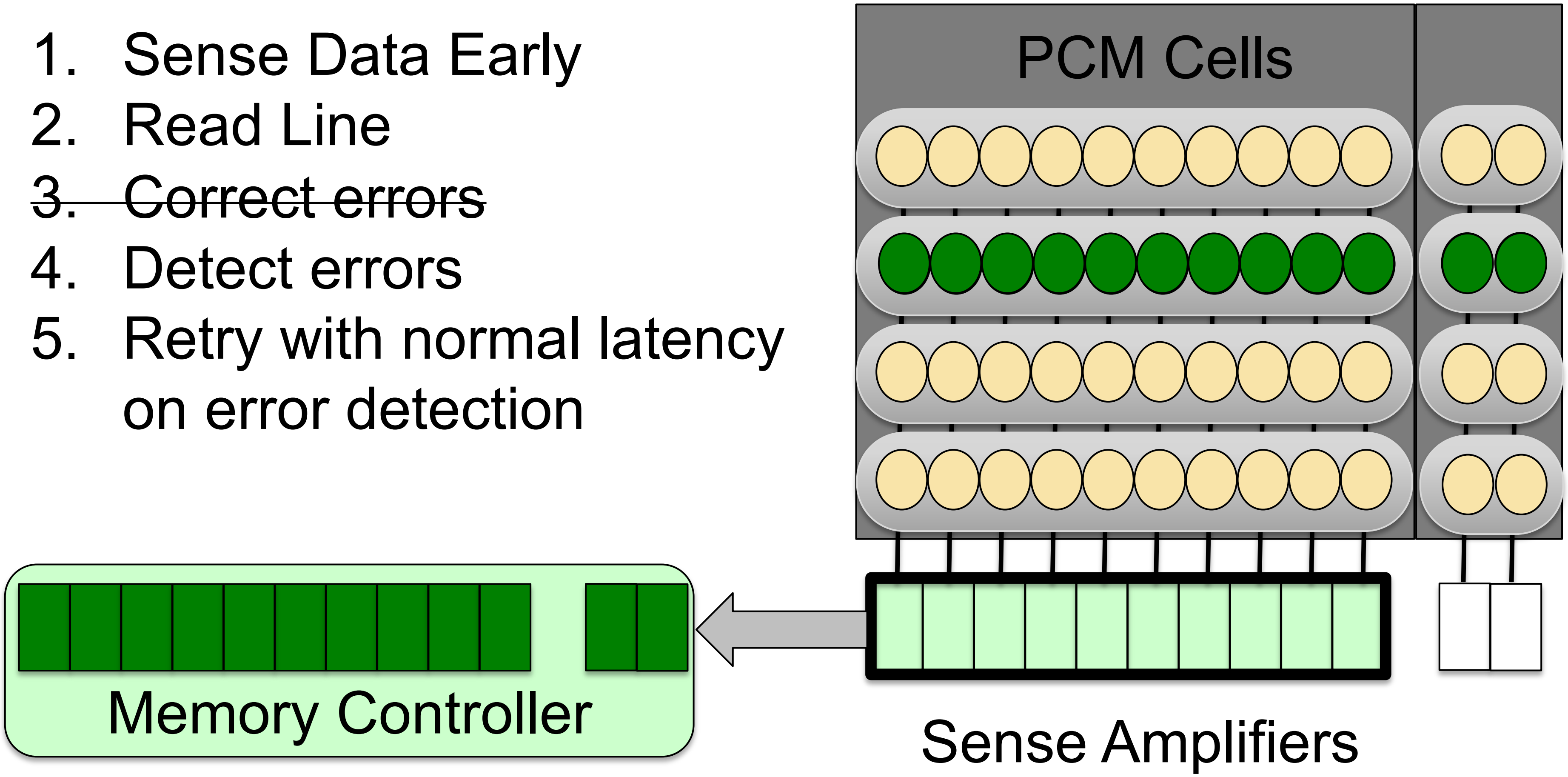

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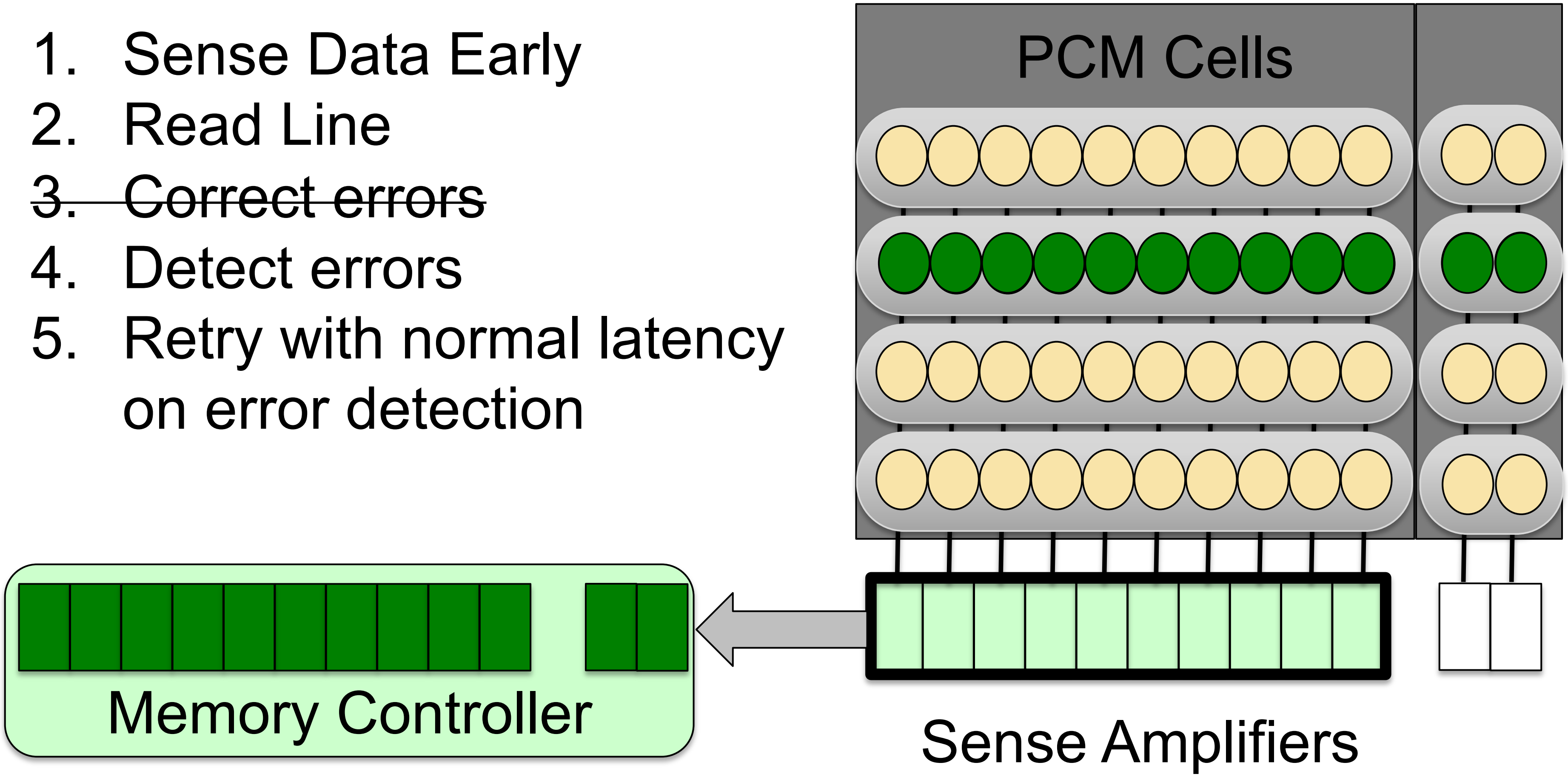
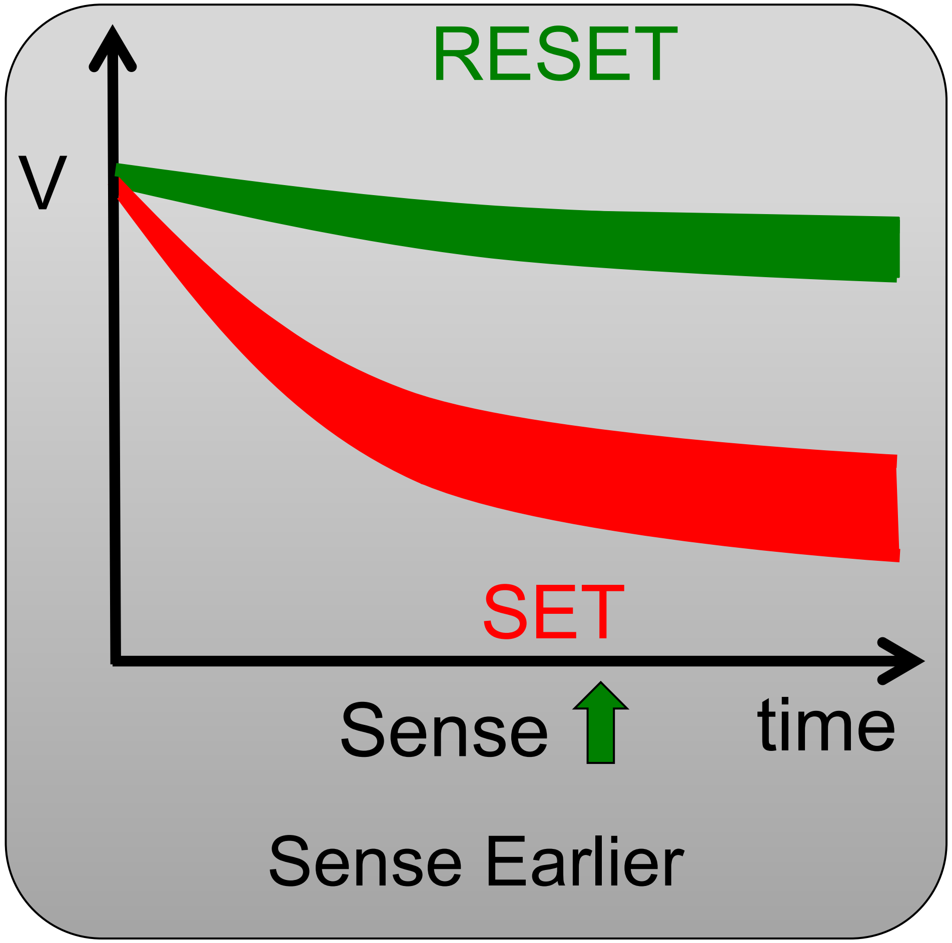
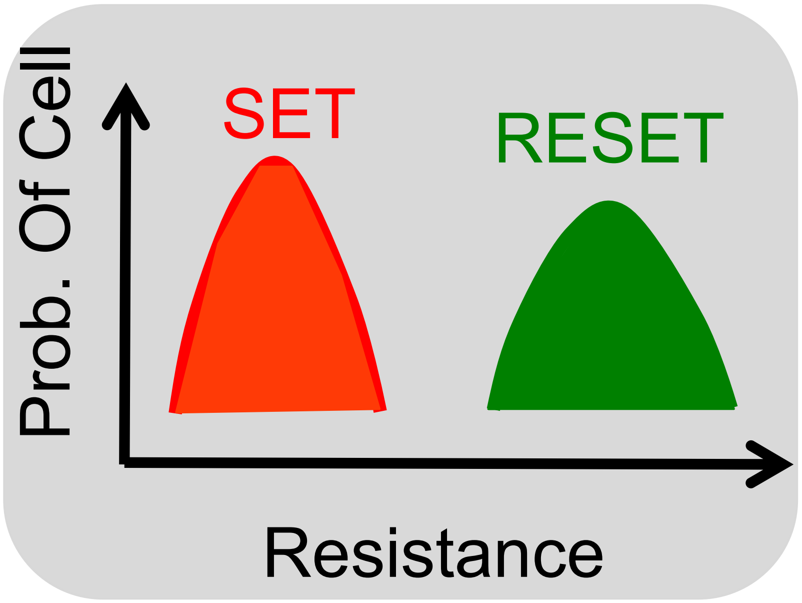


Early Read ➔ detect and retry to read correctly at lower latency

INSIGHT: ERRORS ARE UNIDIRECTIONAL





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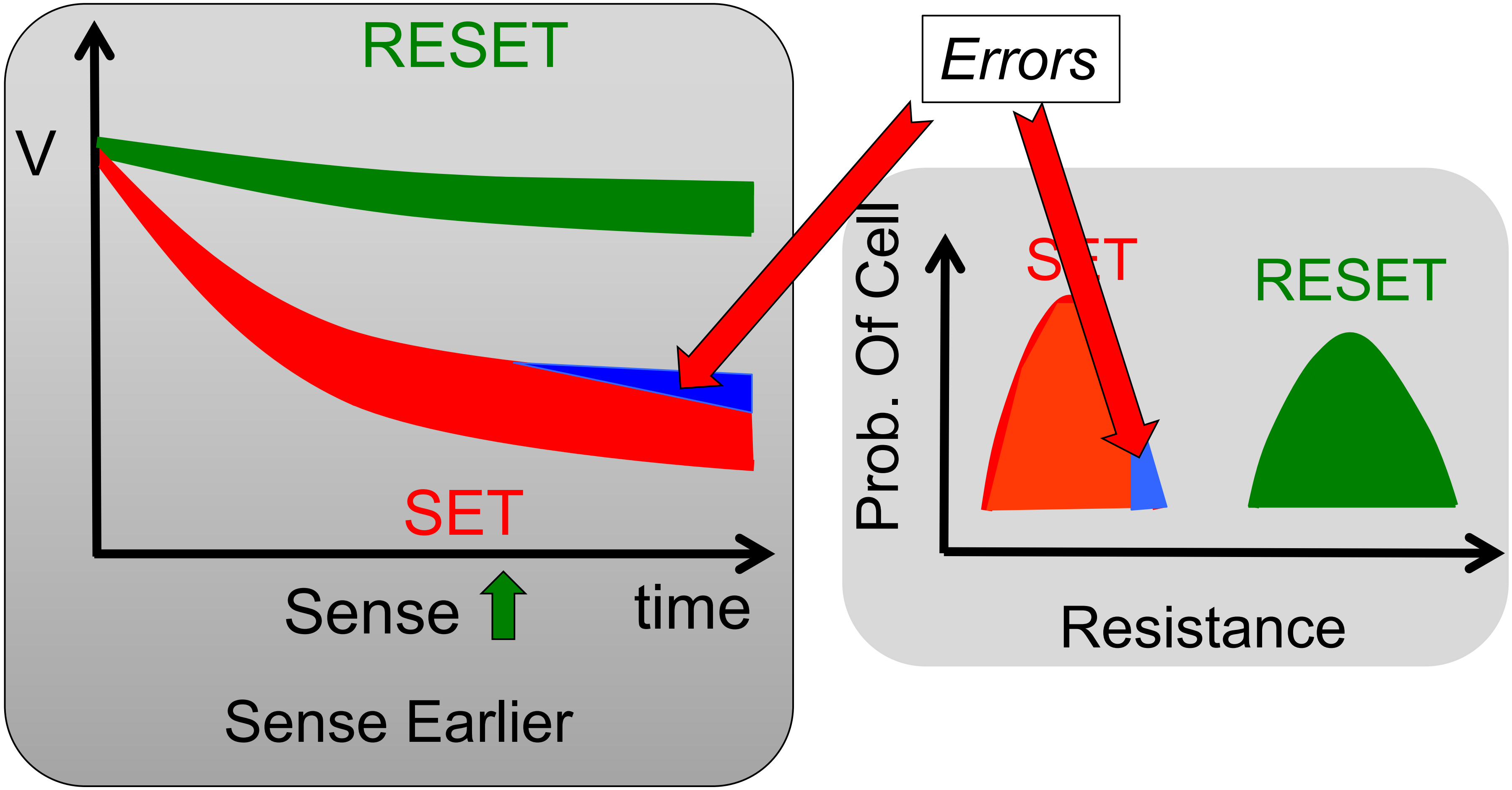

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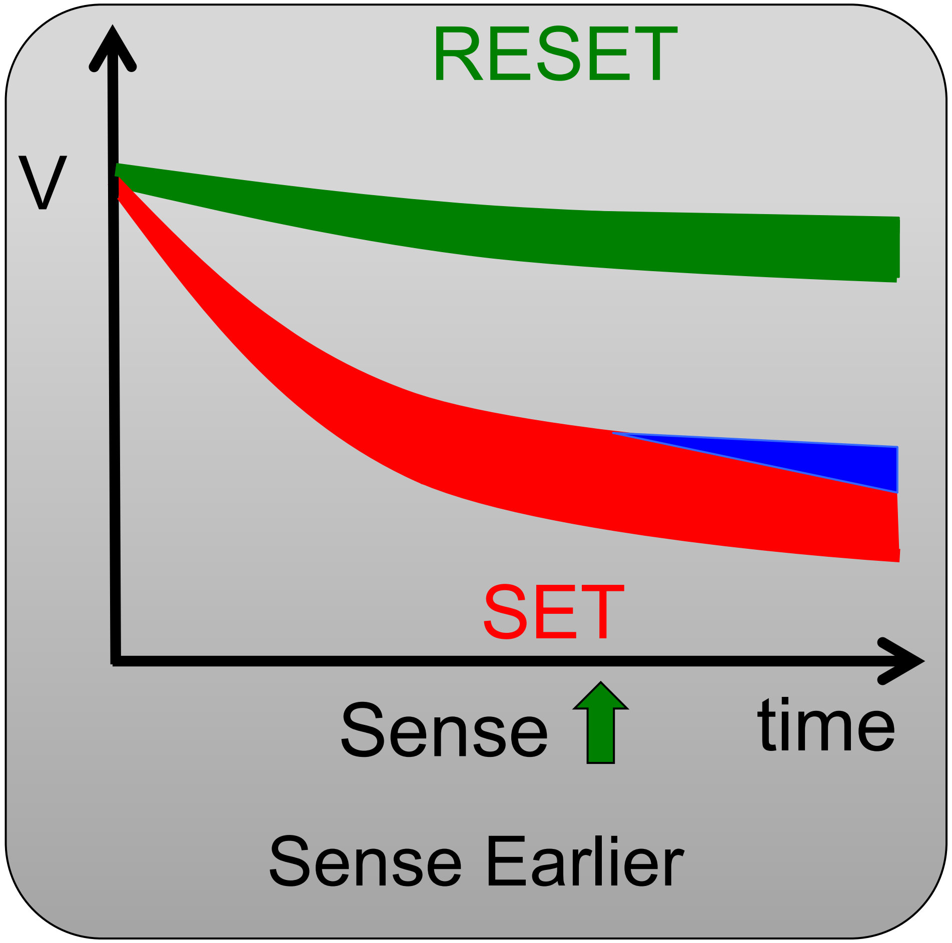

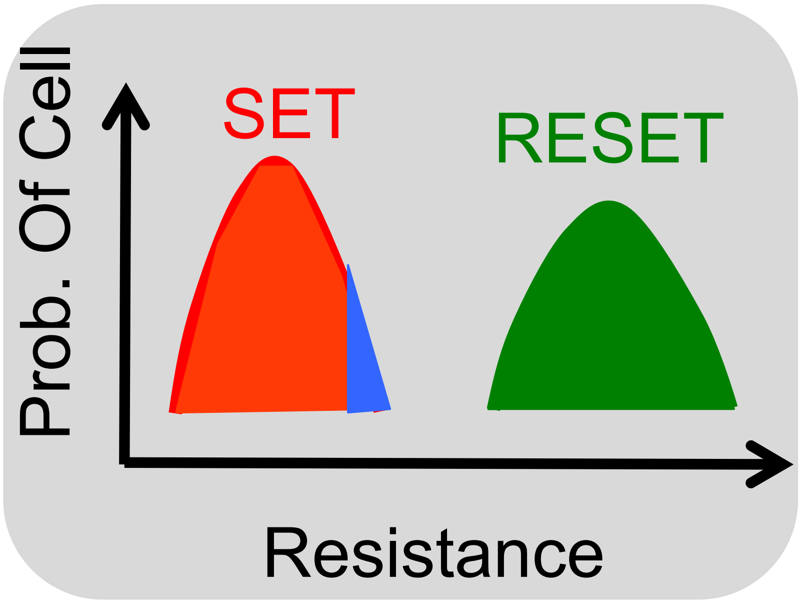

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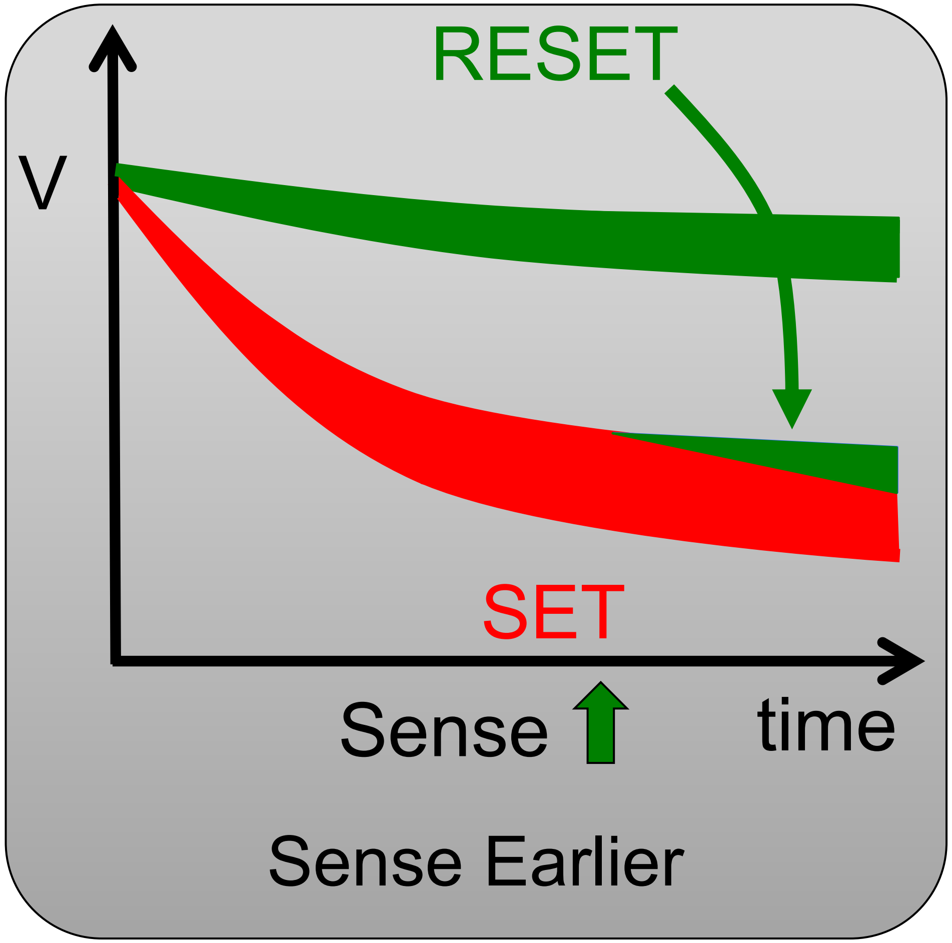
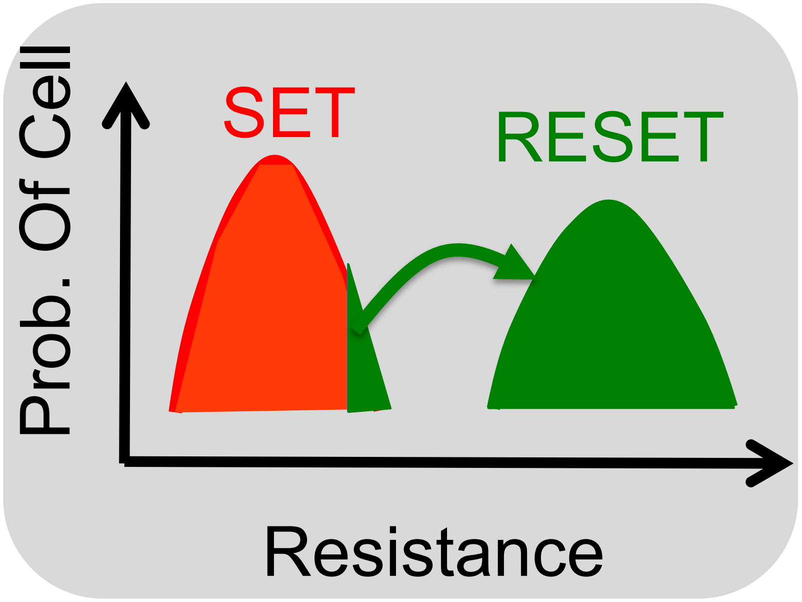
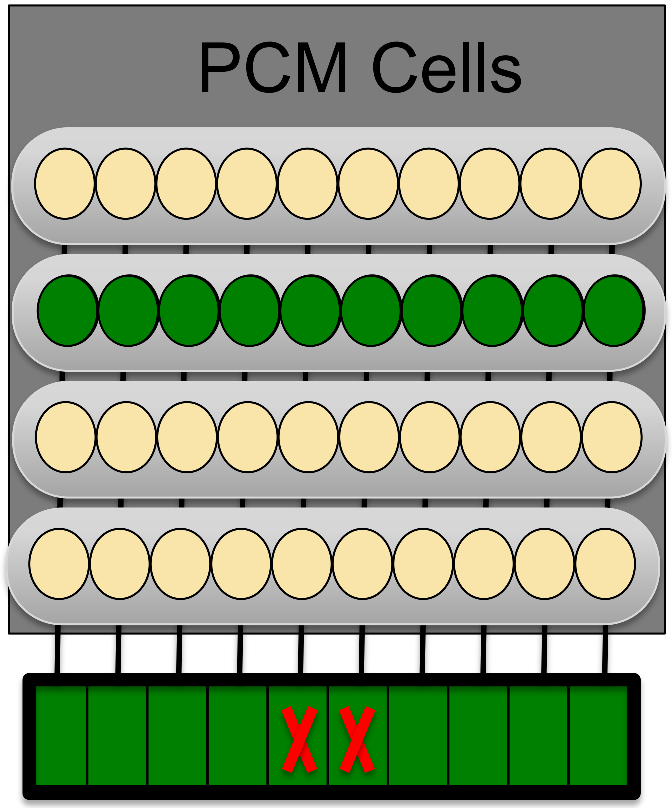




Sensing errors→Unidirectional→SET classified as RESET

UNIDIRECTIONAL ERROR DETECTION

- All unidirectional errors can be detected using Berger Code

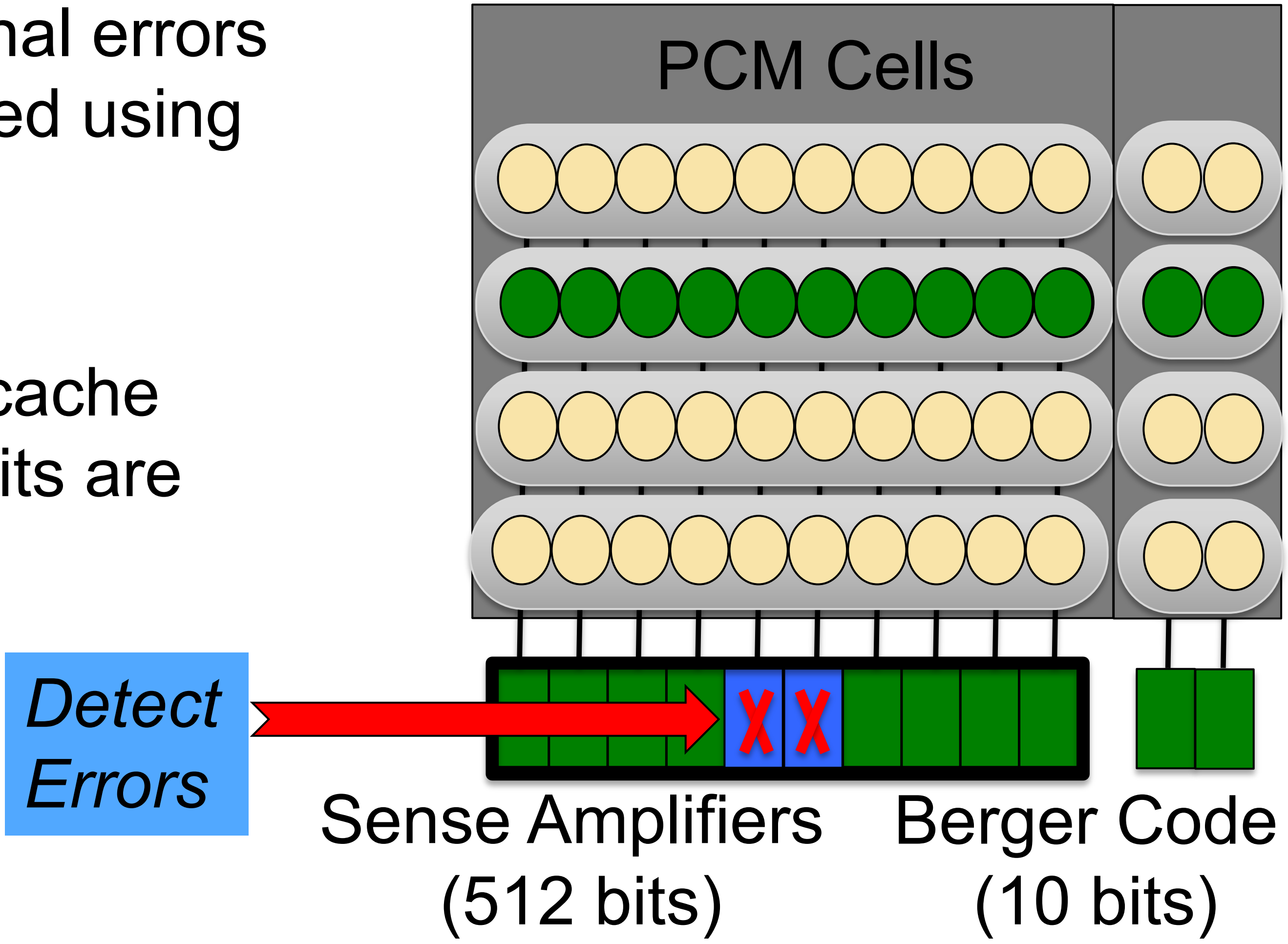


Sense Amplifiers
(512 bits)

UNIDIRECTIONAL ERROR DETECTION

- All unidirectional errors can be detected using Berger Code

- For a 512 bit cache line, only 10 bits are needed



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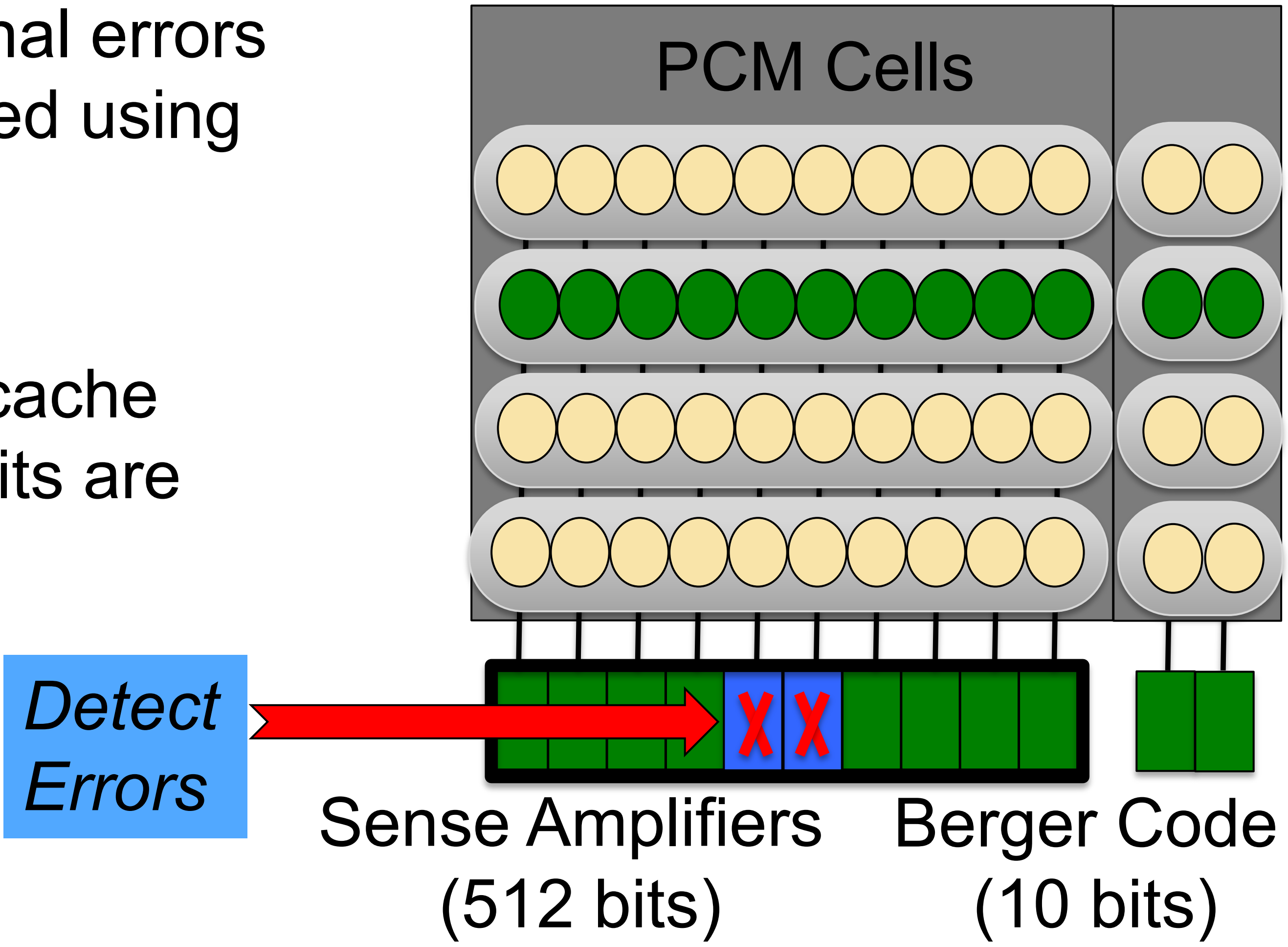
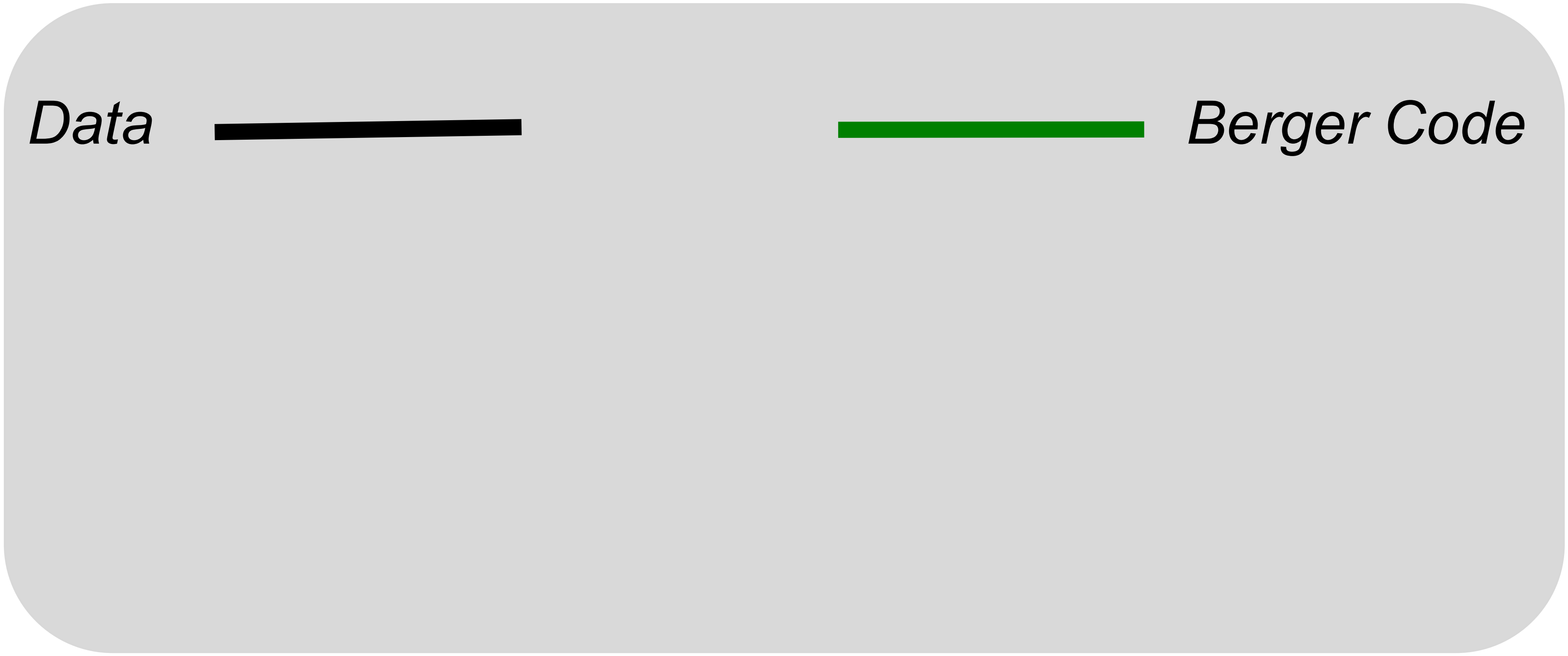


Berger Code detects unidirectional errors with low cost

BERGER CODES: HOW AND WHY

Sum the number of 1’s in data, invert and store



Berger code provides guaranteed detection of all unidirectional errors

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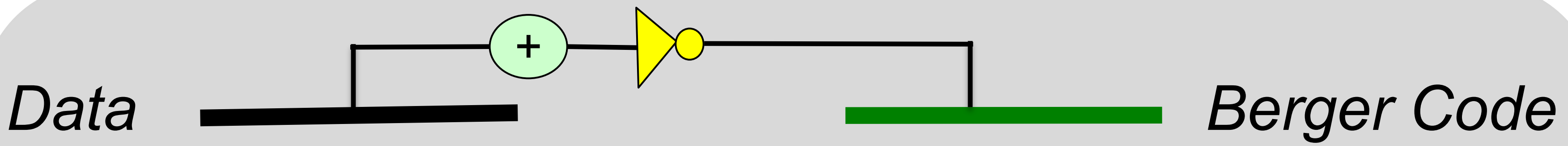

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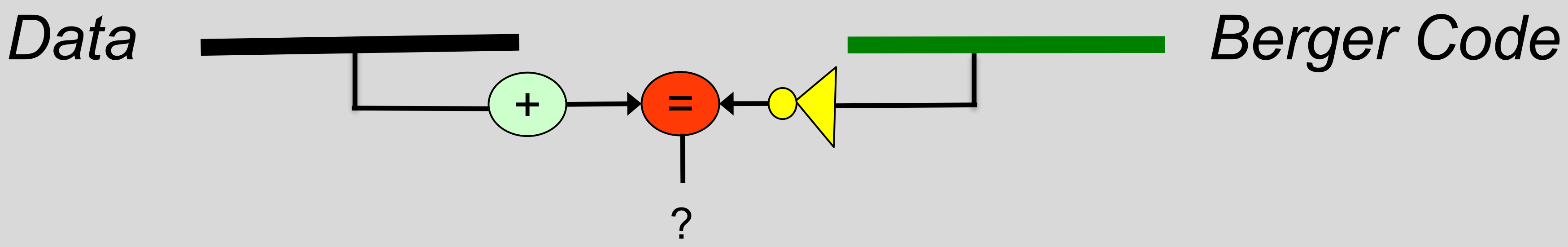

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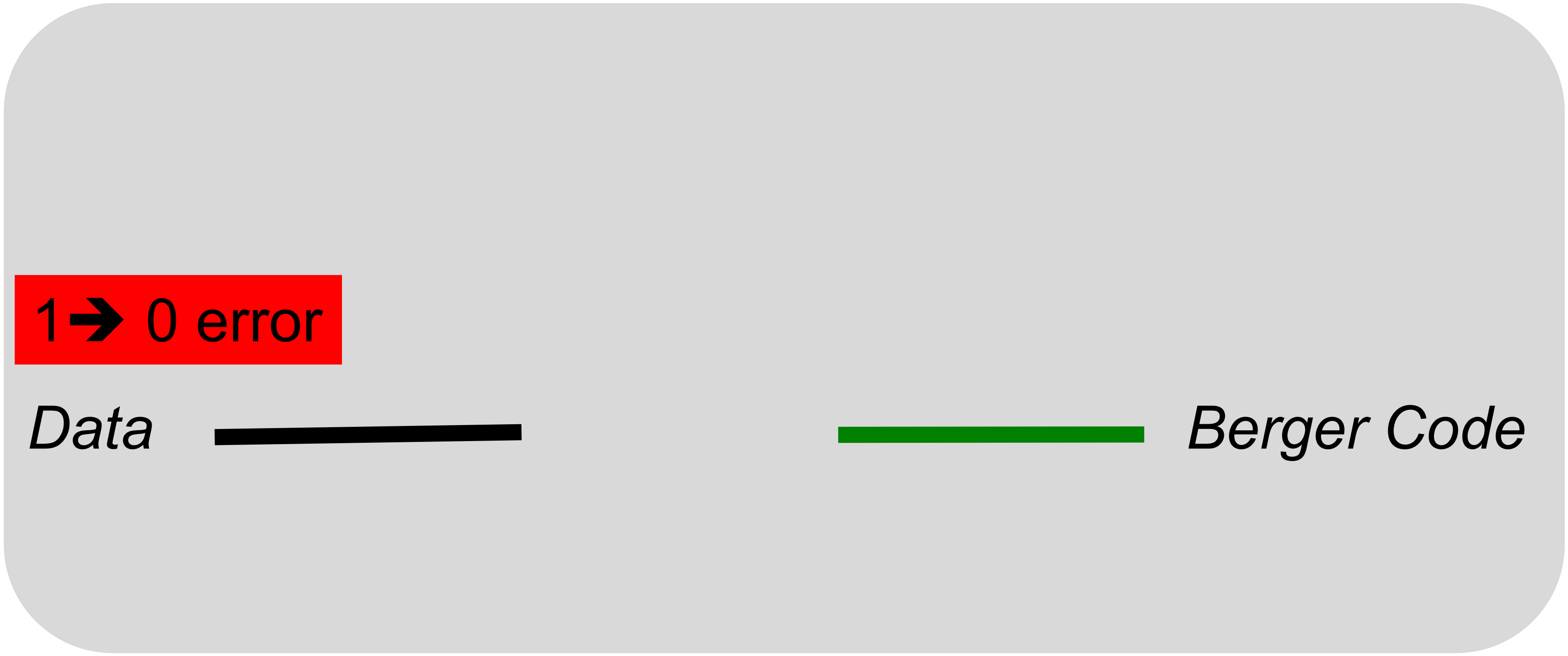

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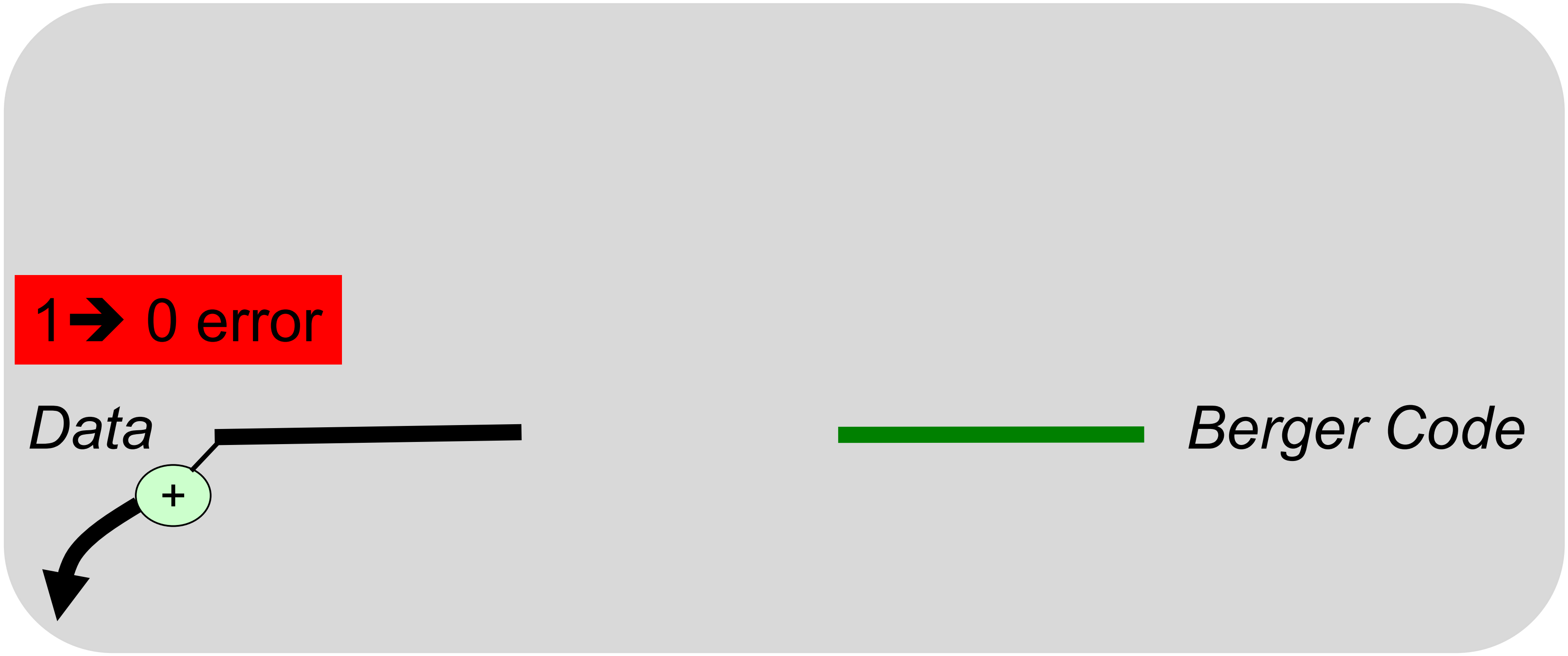

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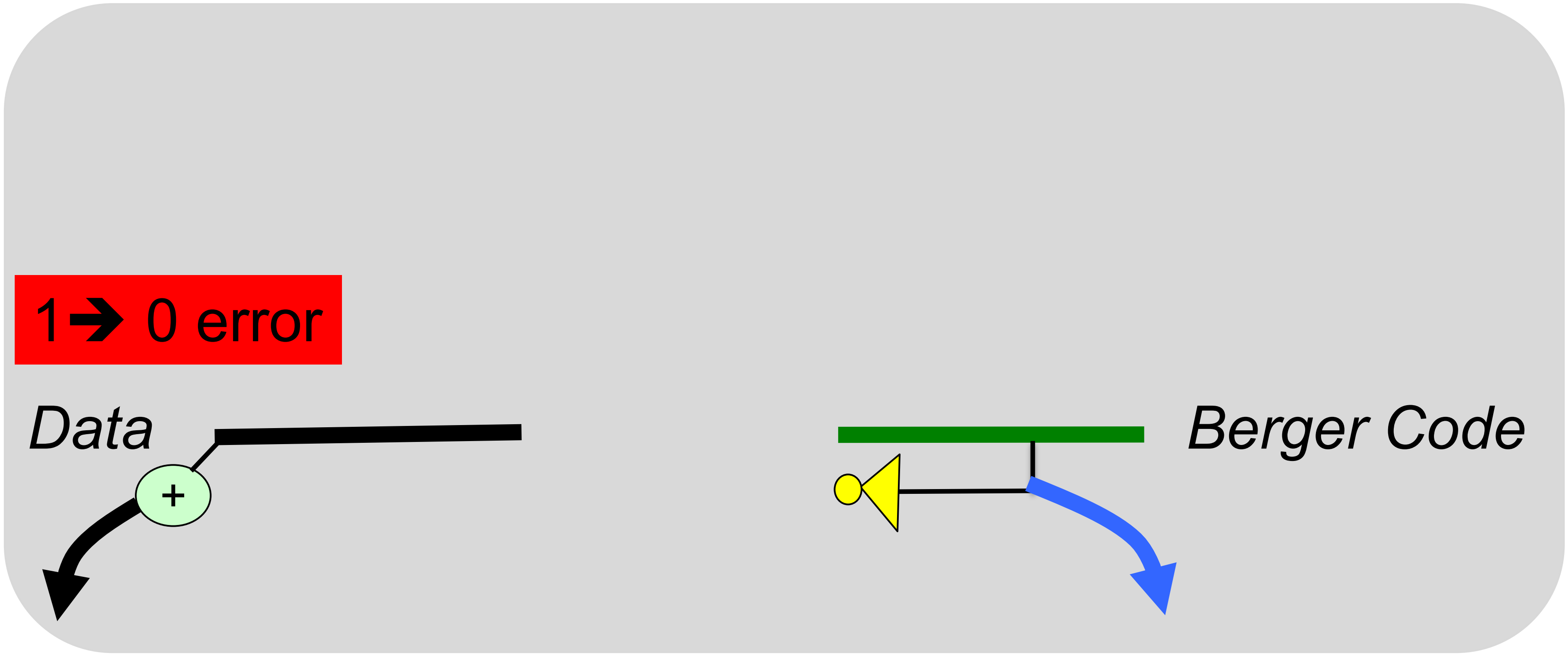

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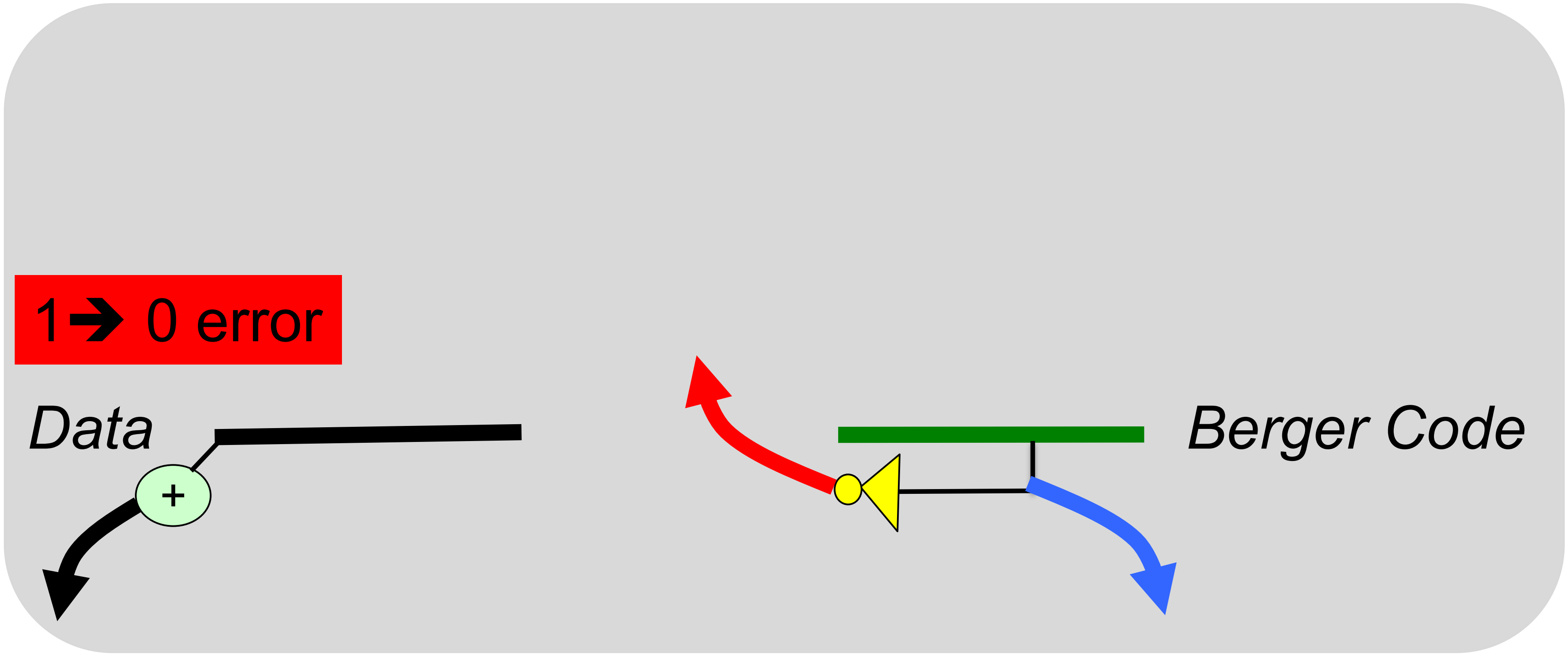

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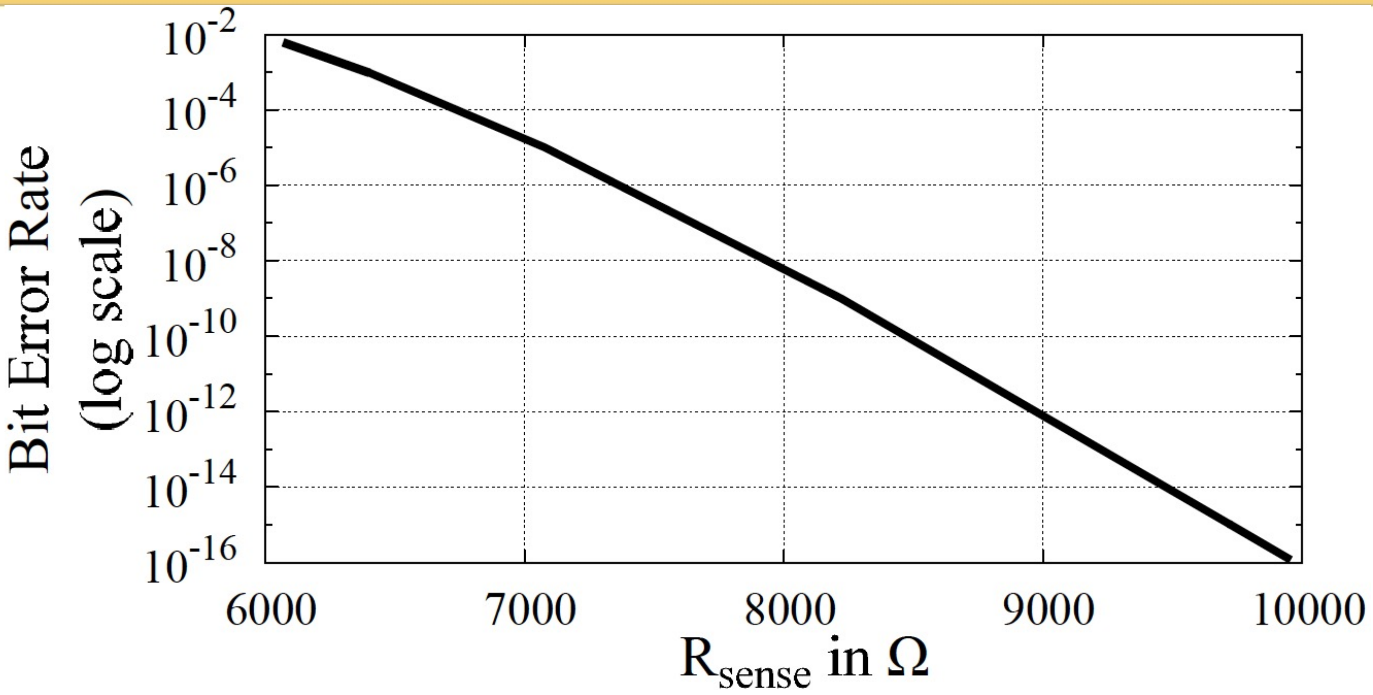
EARLY READ: DESIGN



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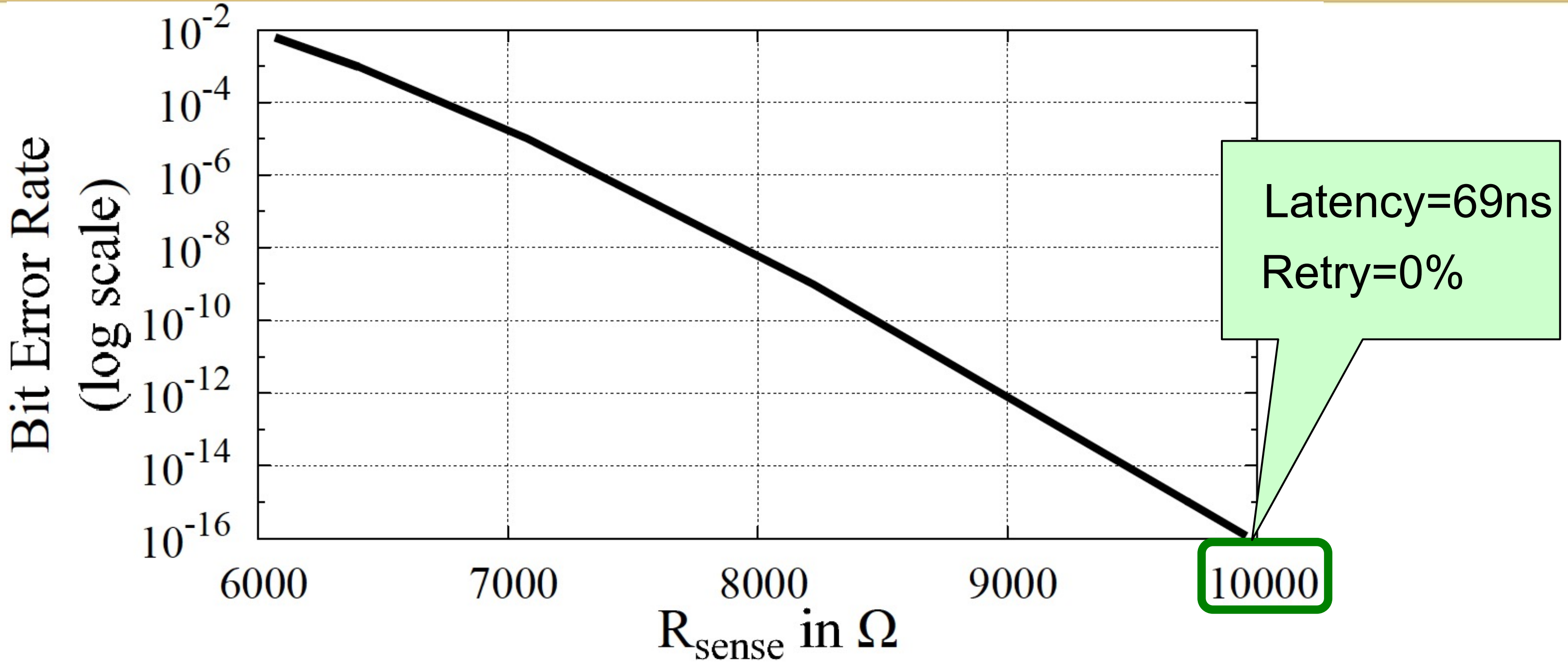

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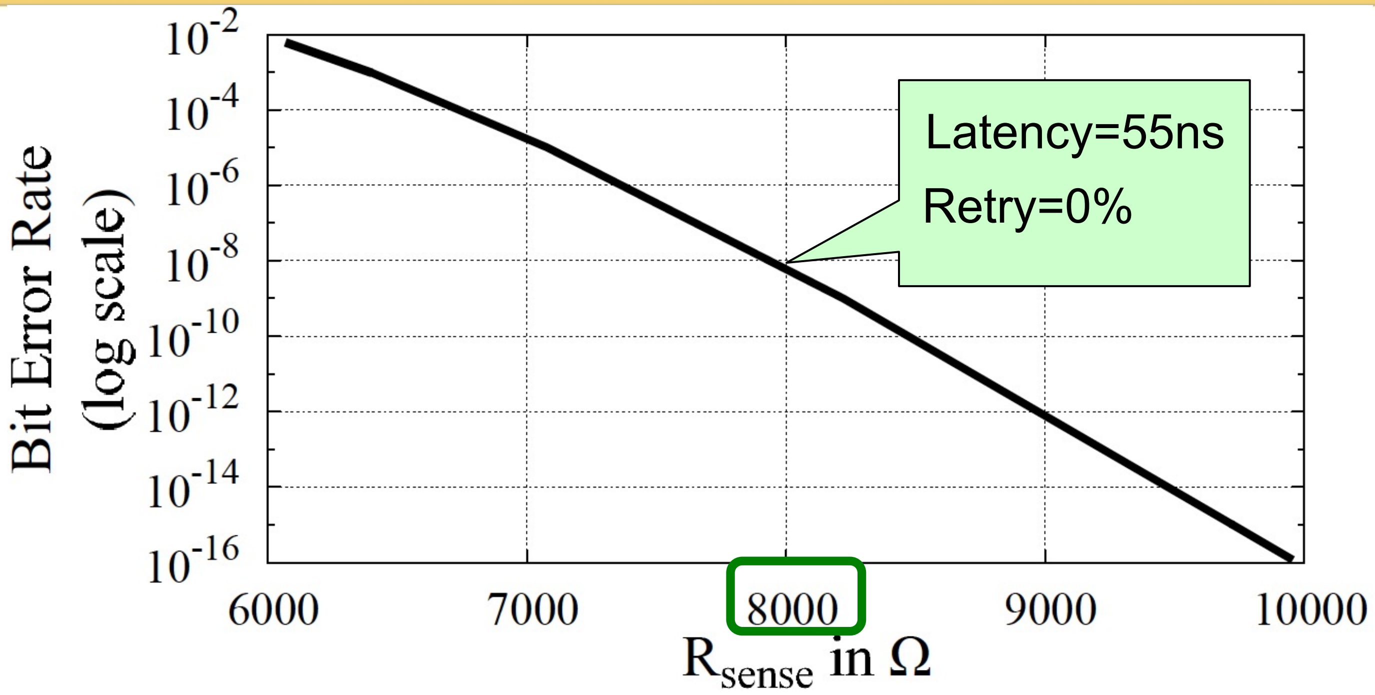

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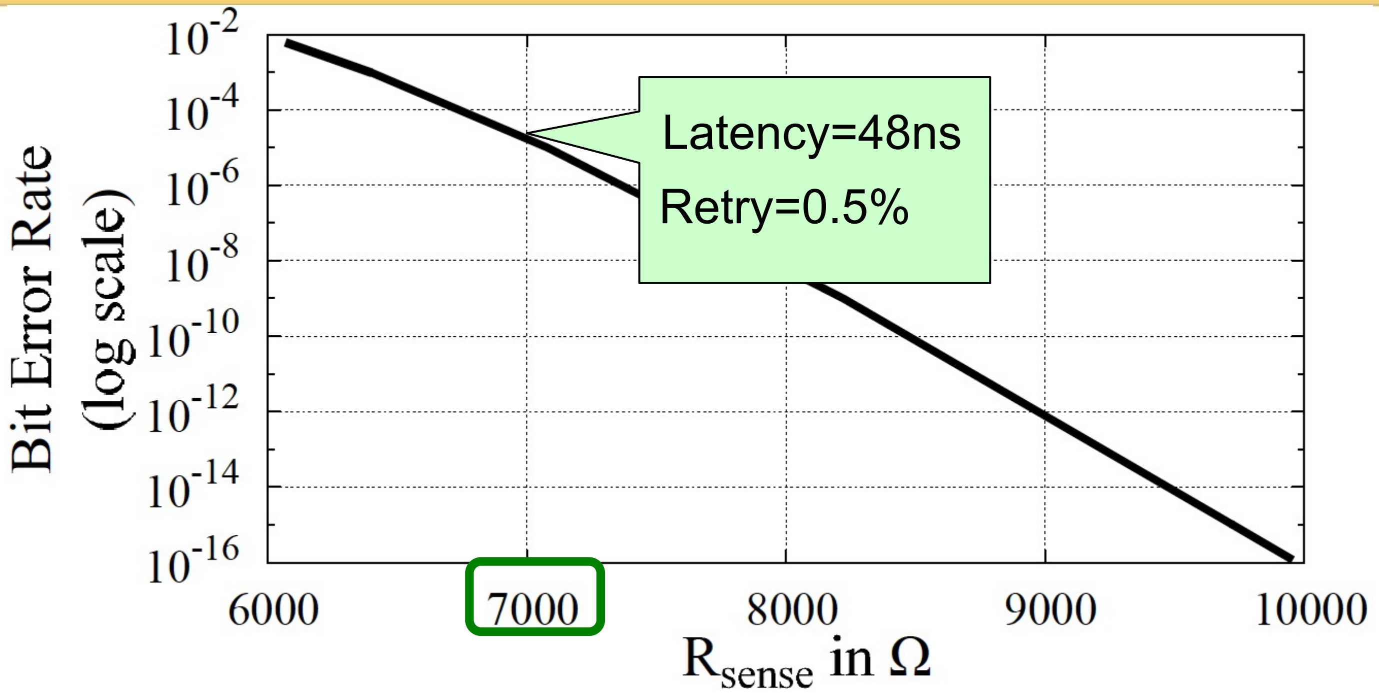

- Early Read reduces R_{sense} from 10KΩ to 7KΩ

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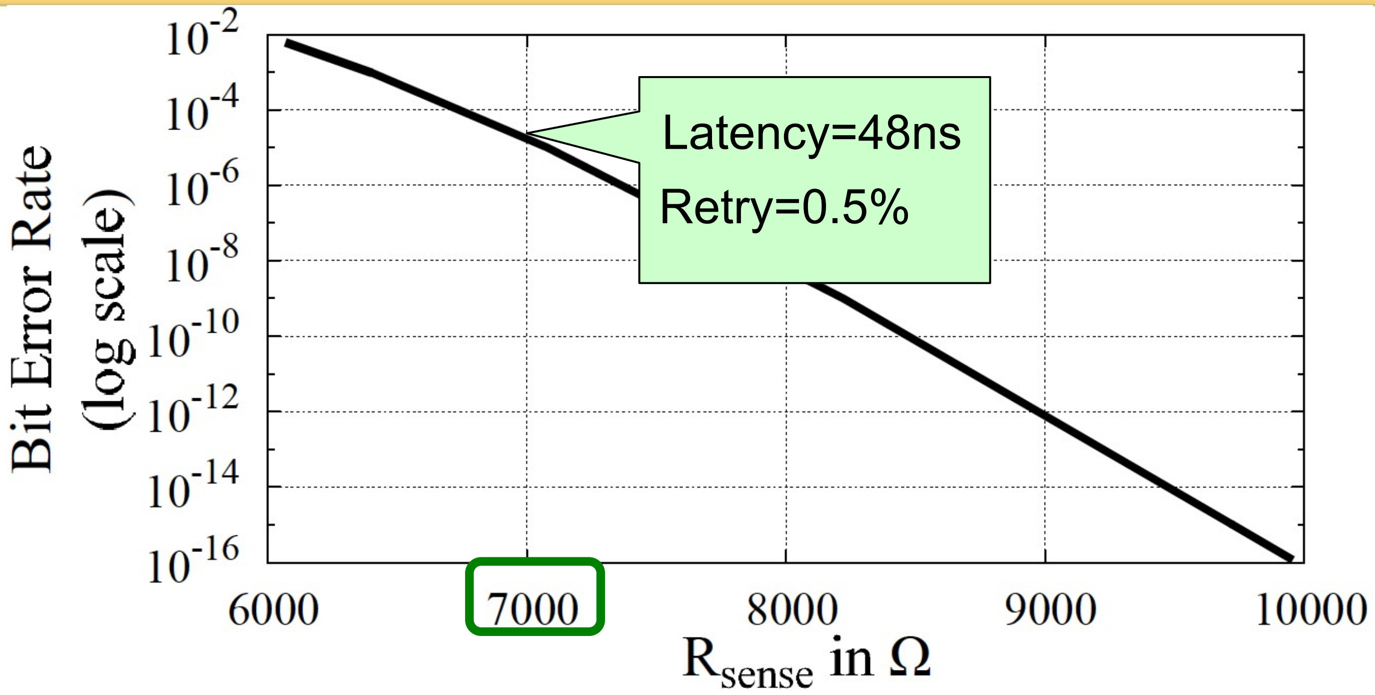

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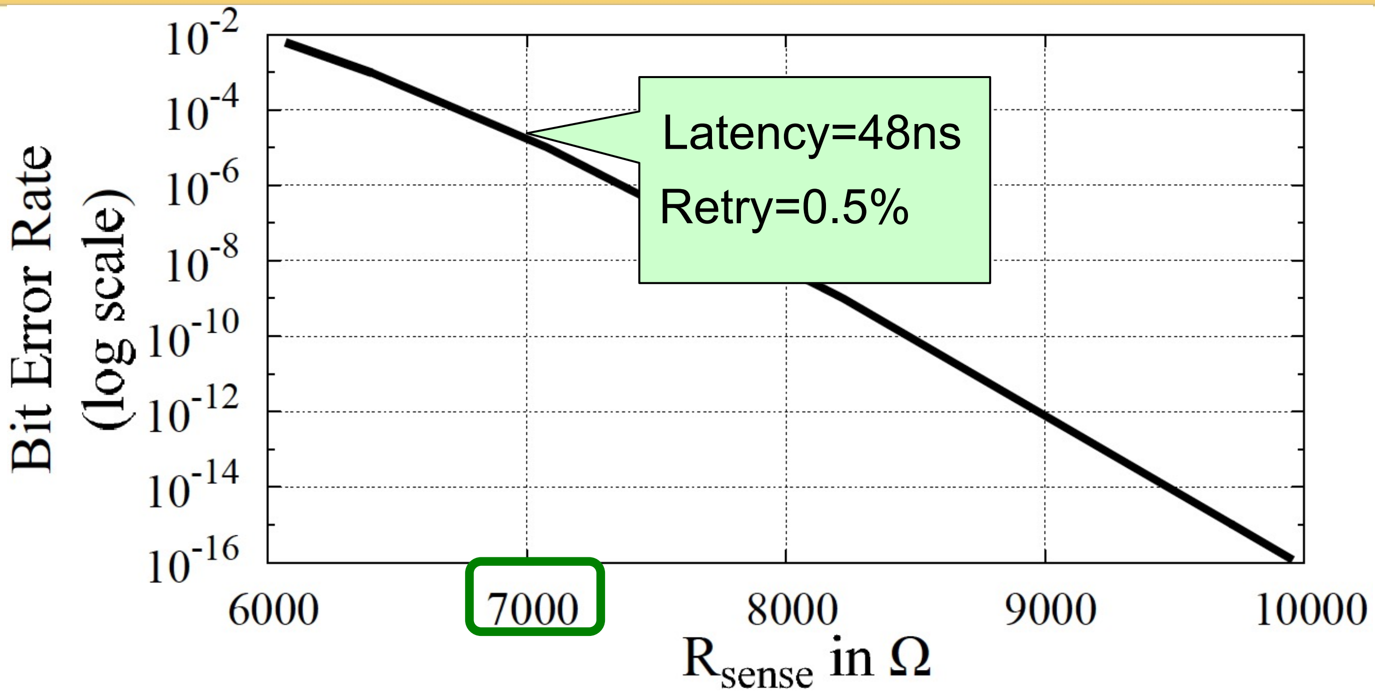

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- Detect using Berger Code, retrying 0.5% times

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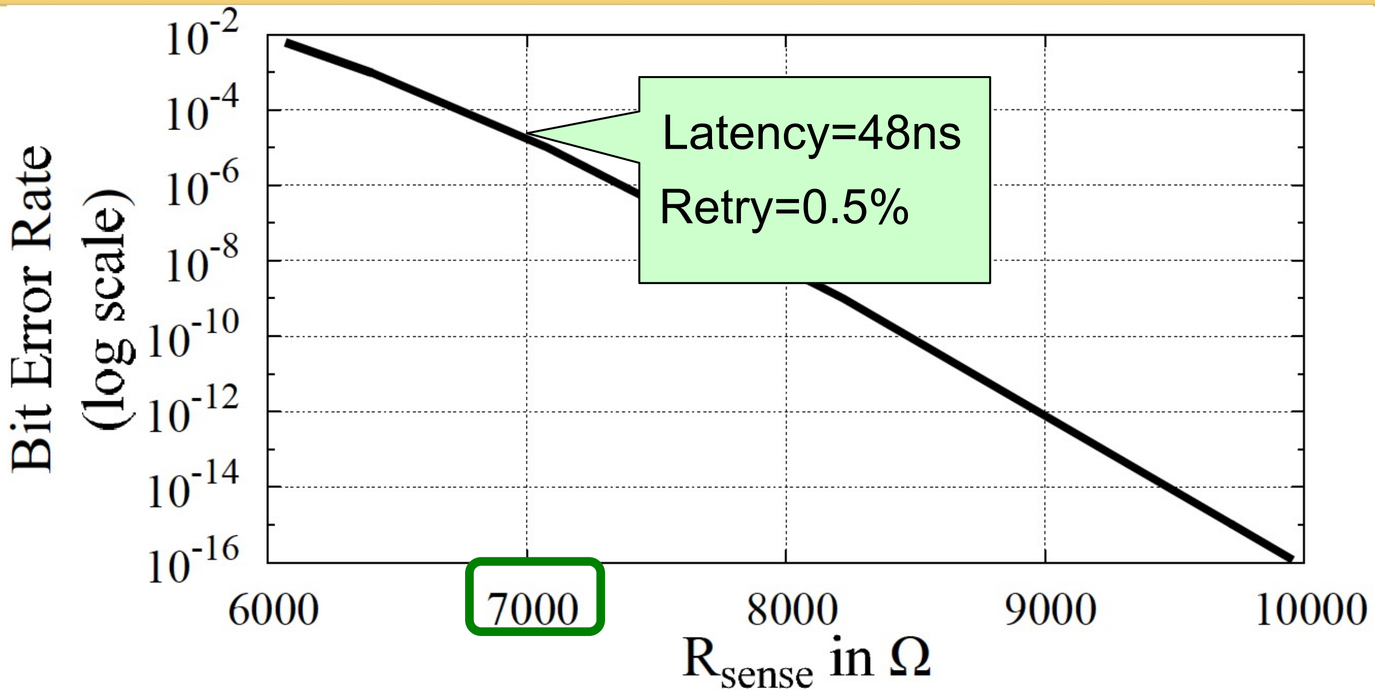

- Early Read reduces R_{sense} from 10KΩ to 7KΩ
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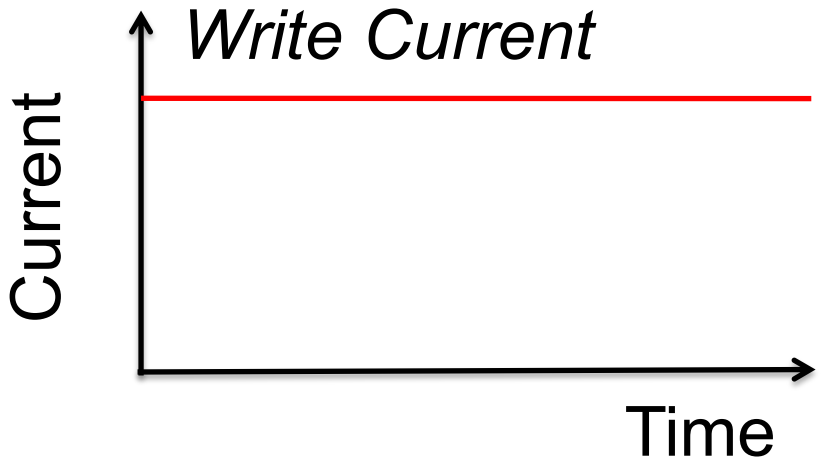
25% reduction in read latency using Early Read

OUTLINE

- Introduction and Background
- Early Read
- Turbo Read
- Early+Turbo Read
- Results
- Summary

READING WITH HIGHER VOLTAGE

- PCM writes data by passing current through cell



READING WITH HIGHER VOLTAGE

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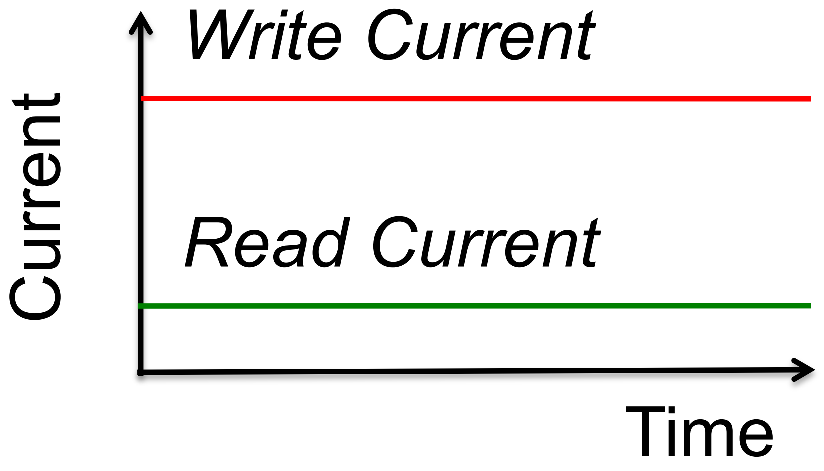

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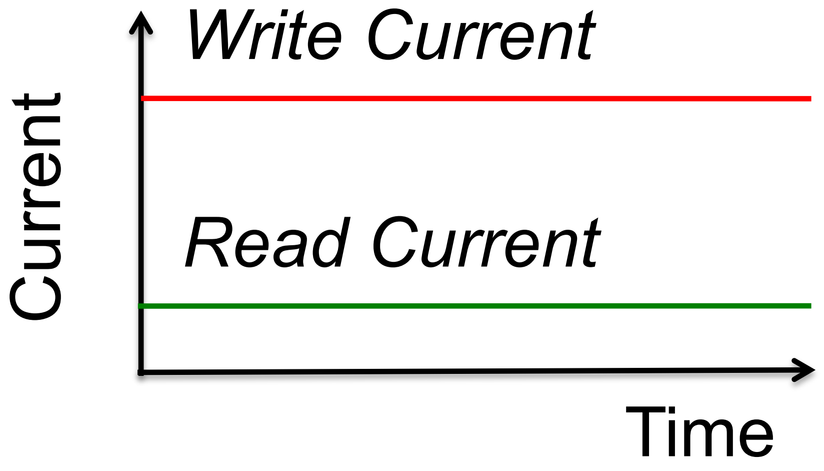

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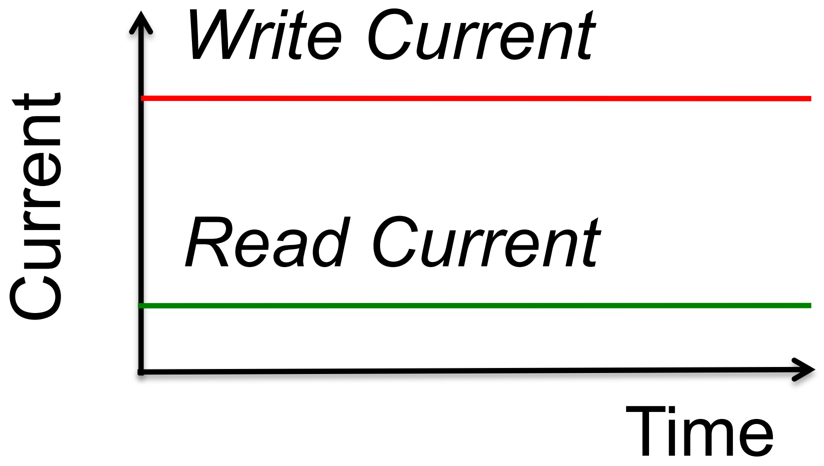
- Higher read current can reduce read latency



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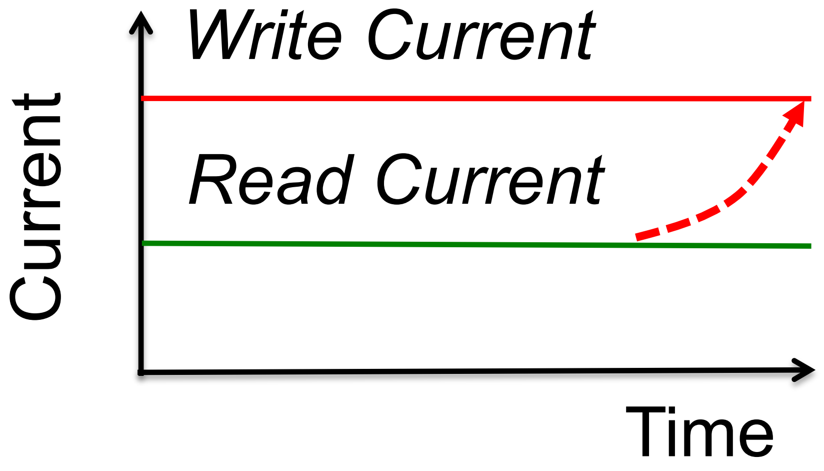

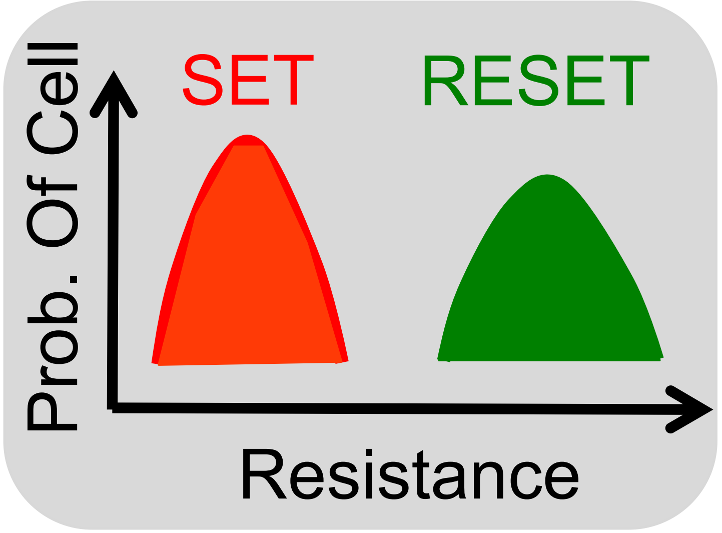

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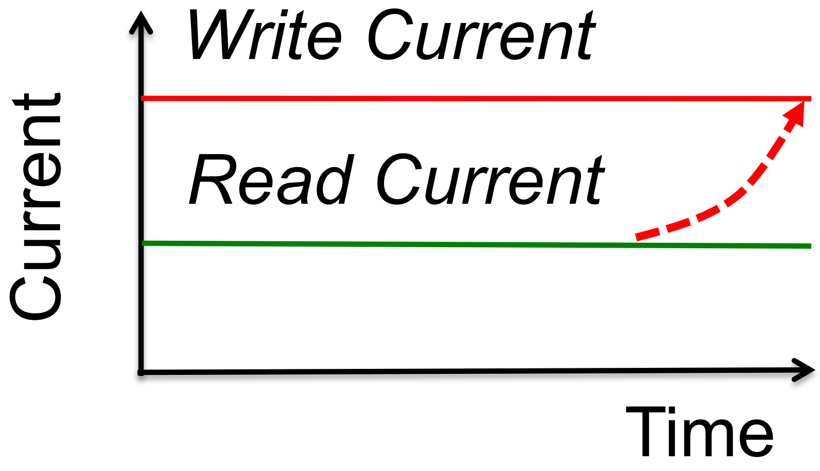

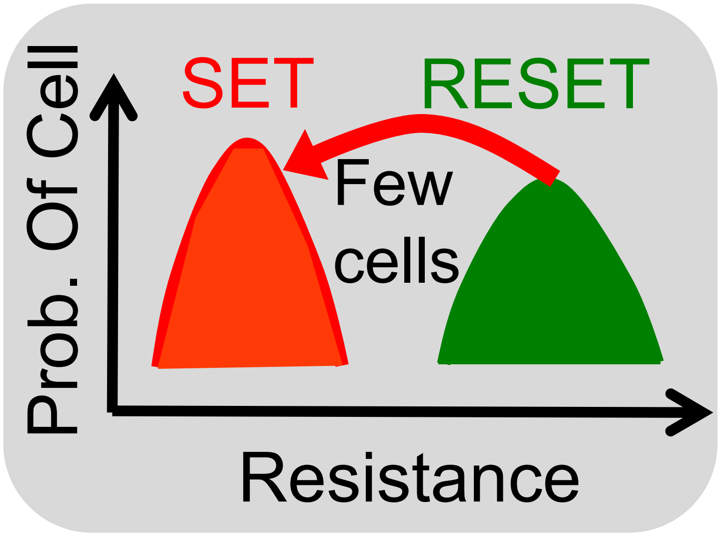

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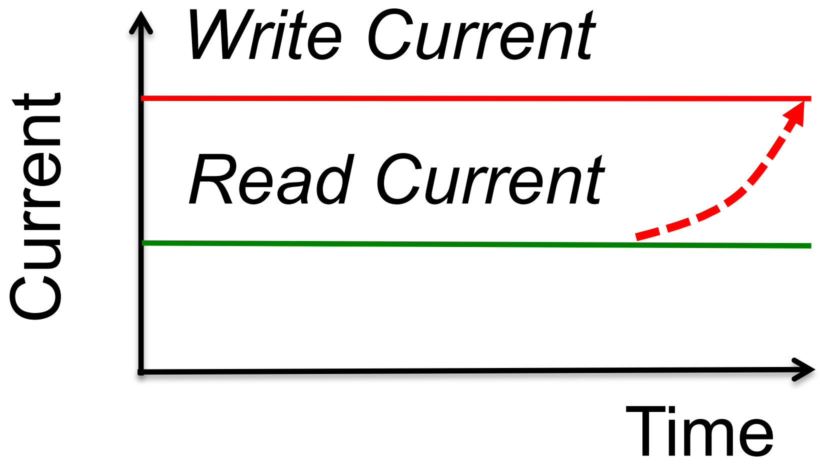
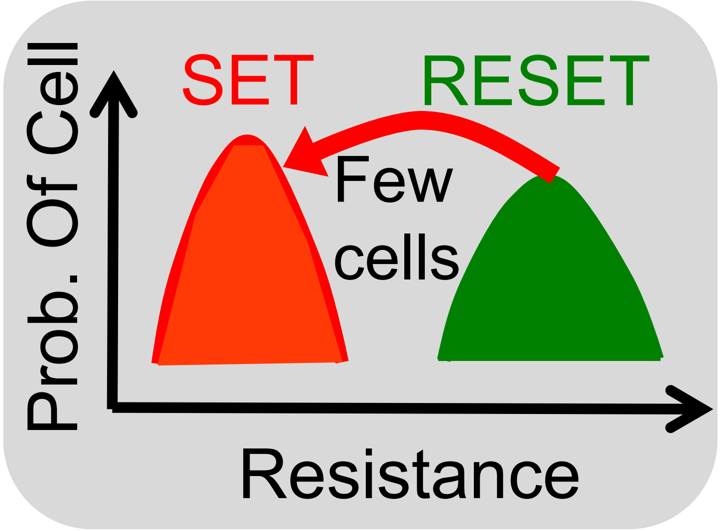
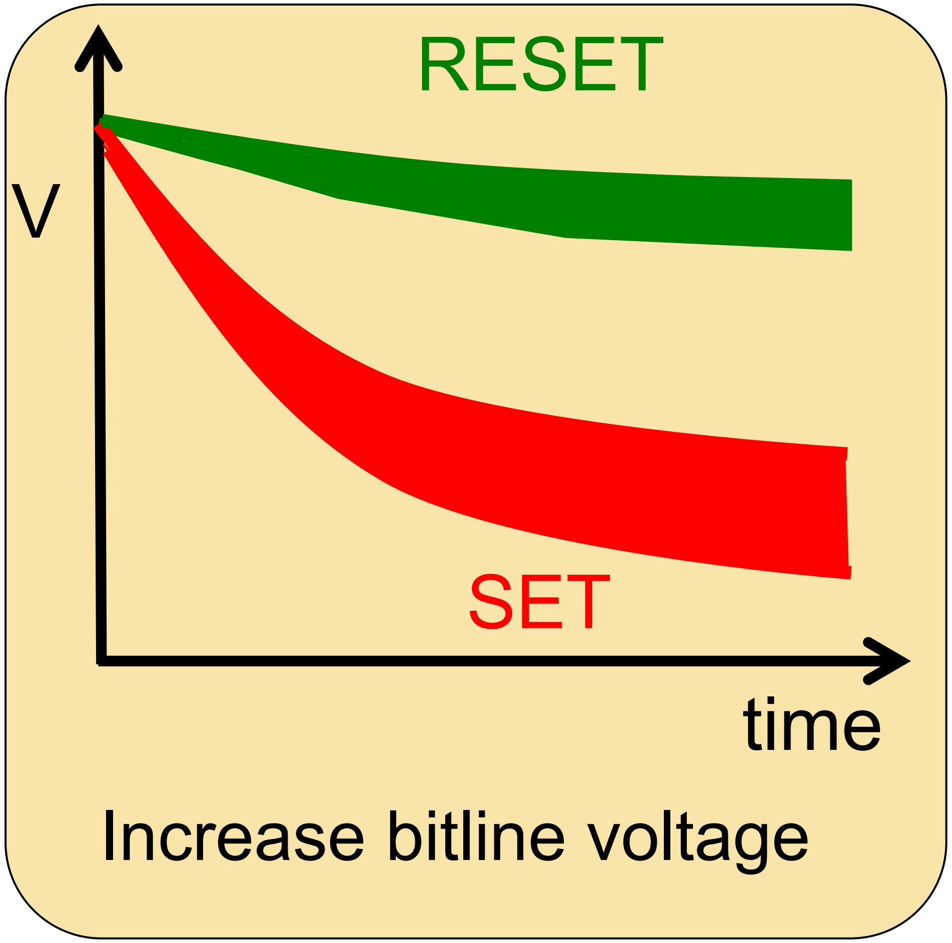


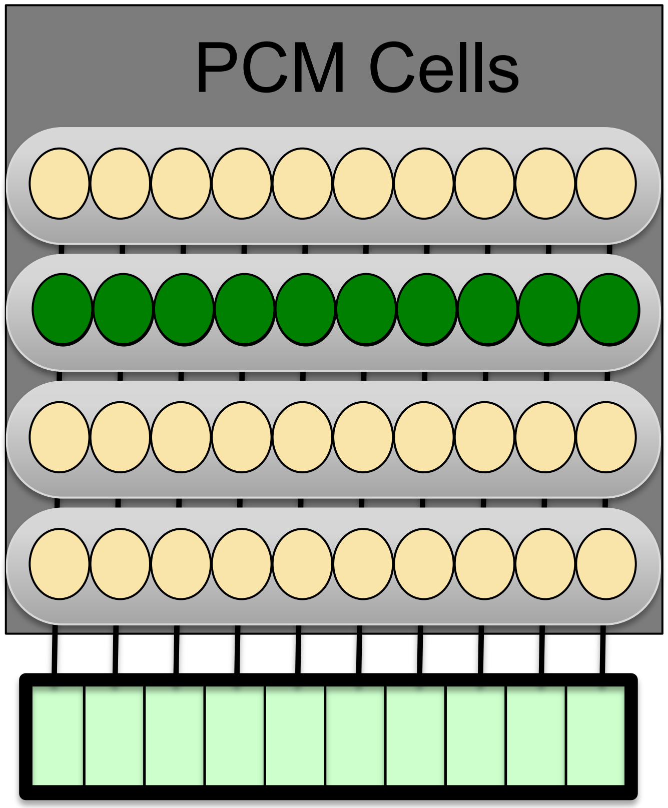


Higher bitline voltage causes Read Disturb

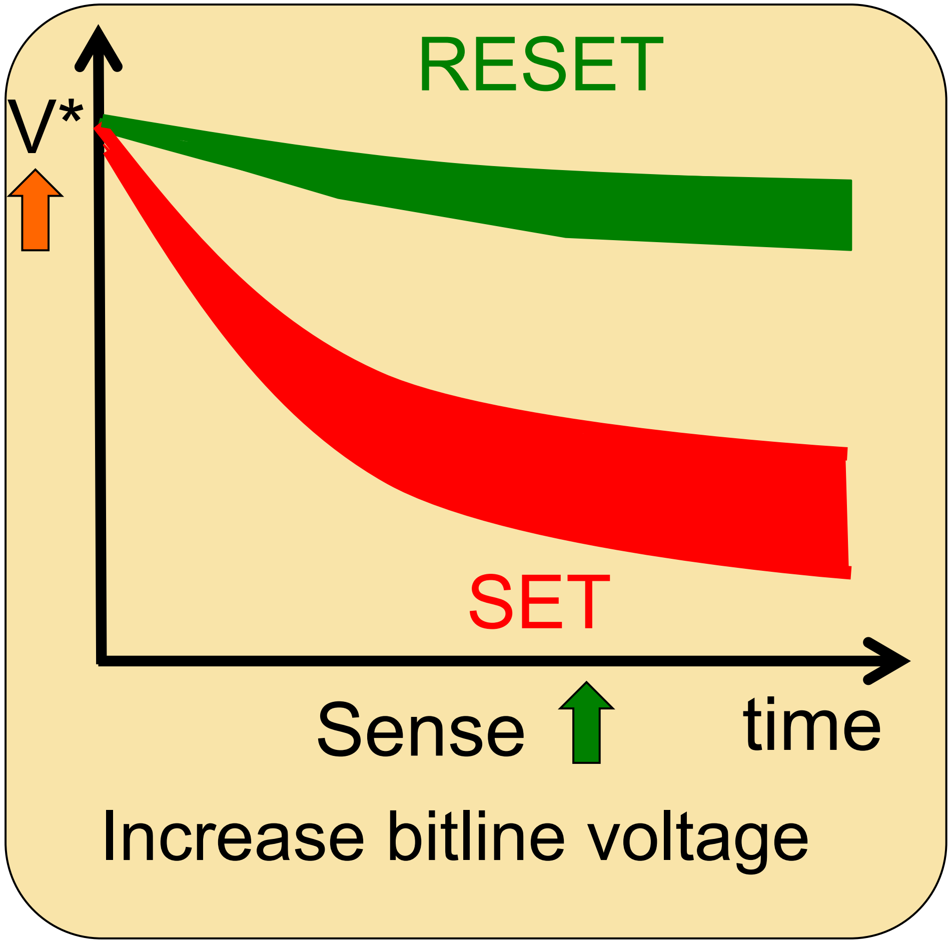
READ DISTURB: OBSERVATION

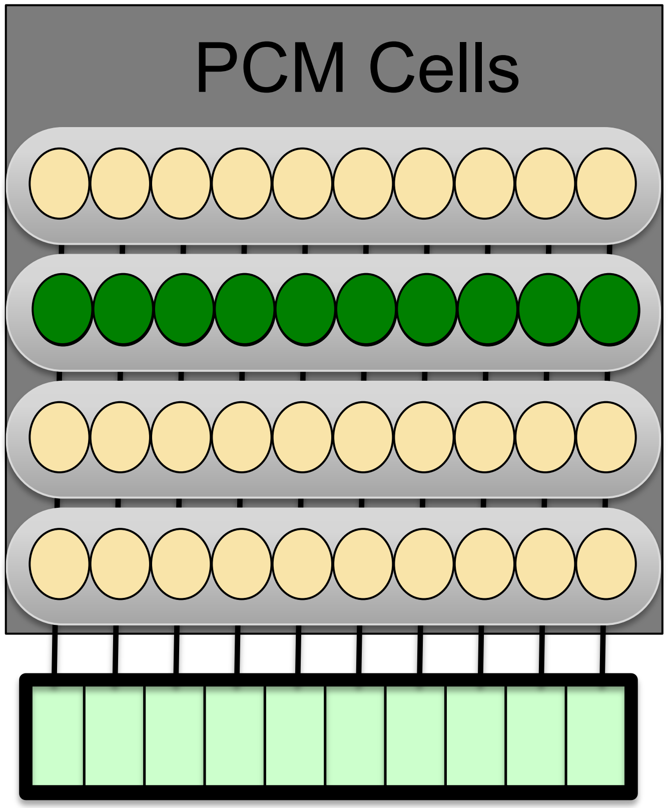


Increase bitline voltage



READ DISTURB: OBSERVATION





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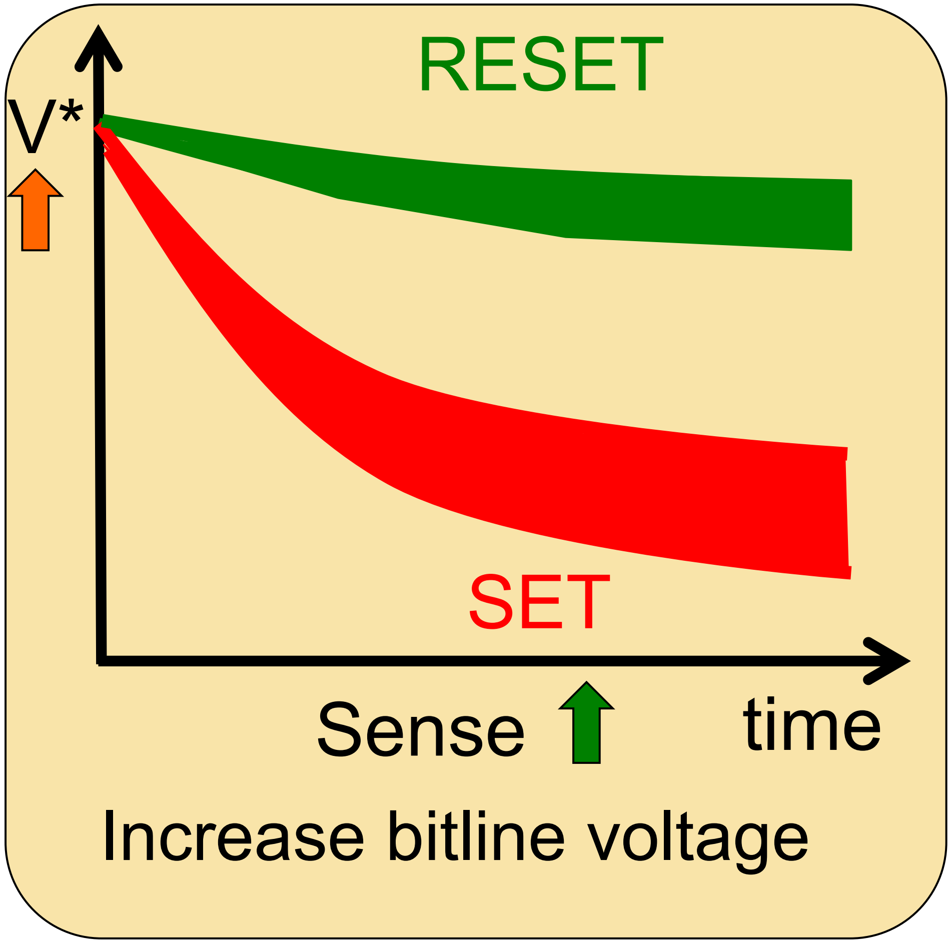

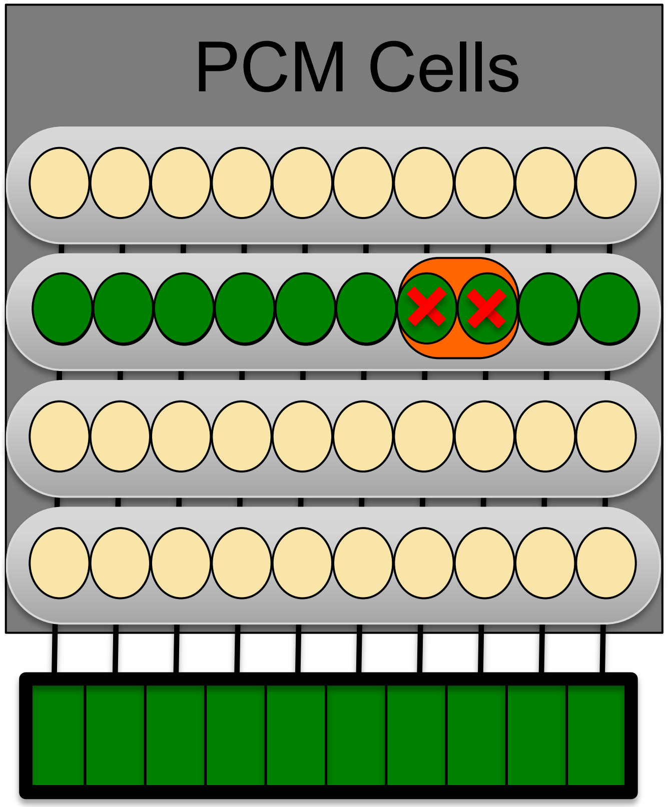

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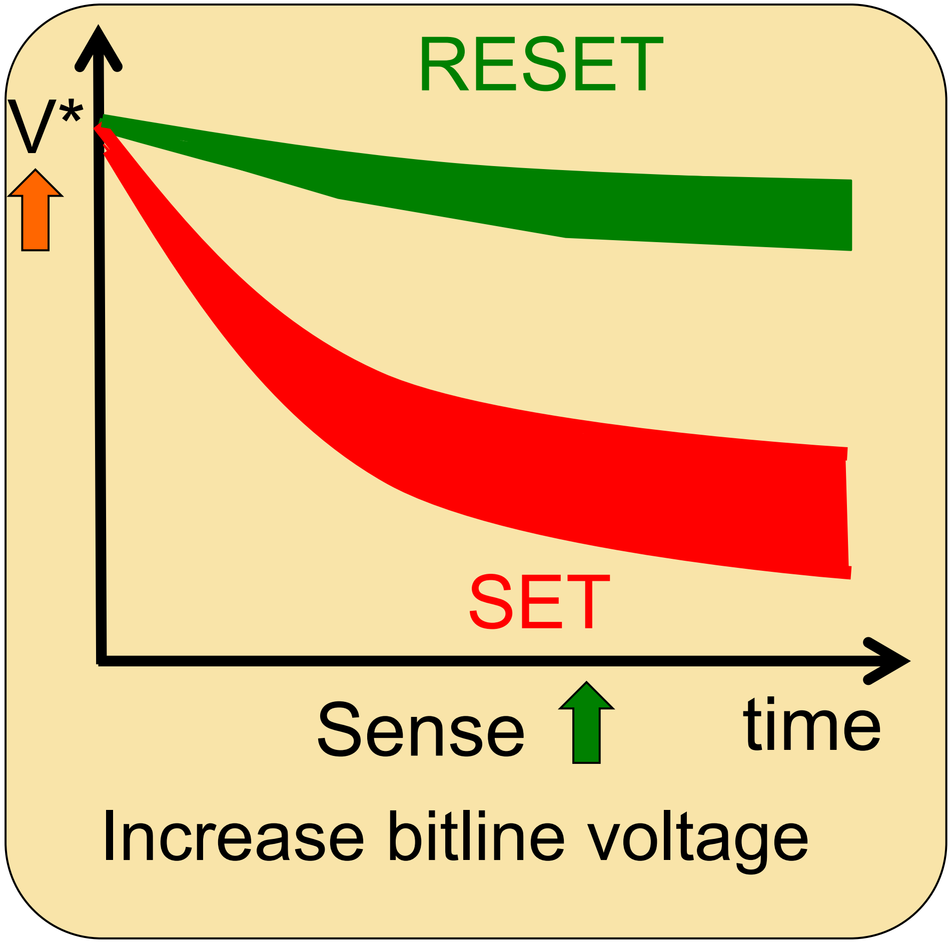
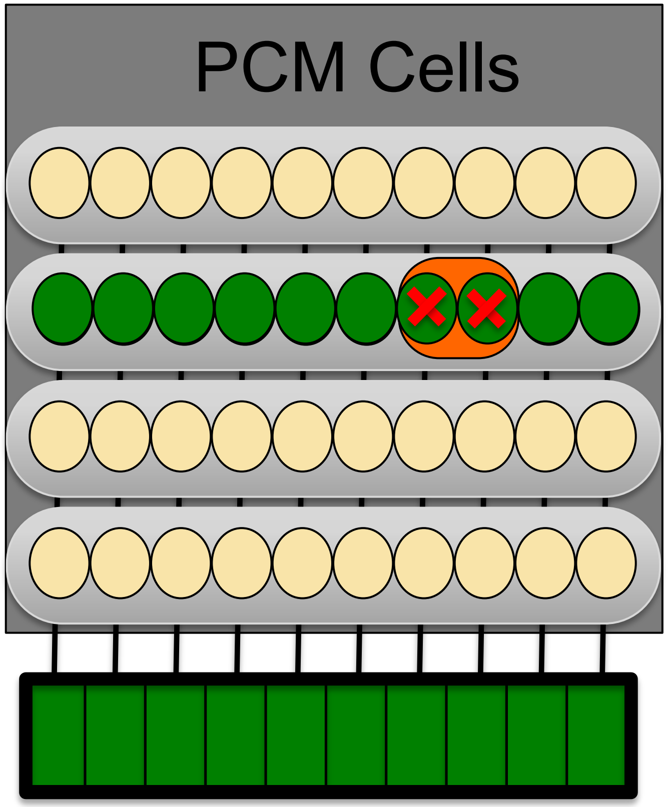
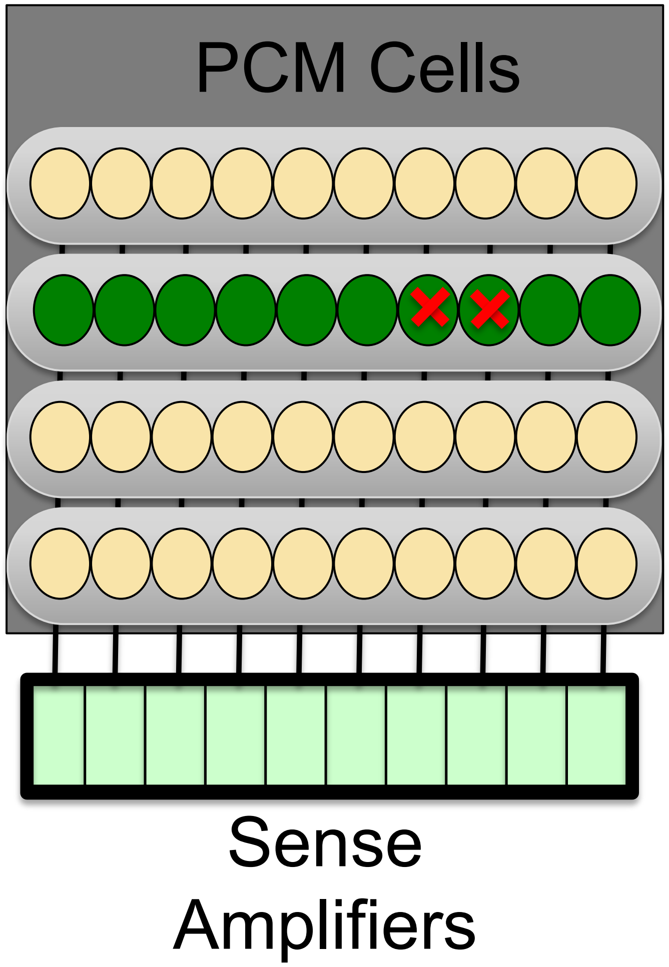




Reading with higher voltage → Read Disturb → causes errors in PCM cells

ECC FOR READ DISTURB ERRORS

- Incorrect value may be read



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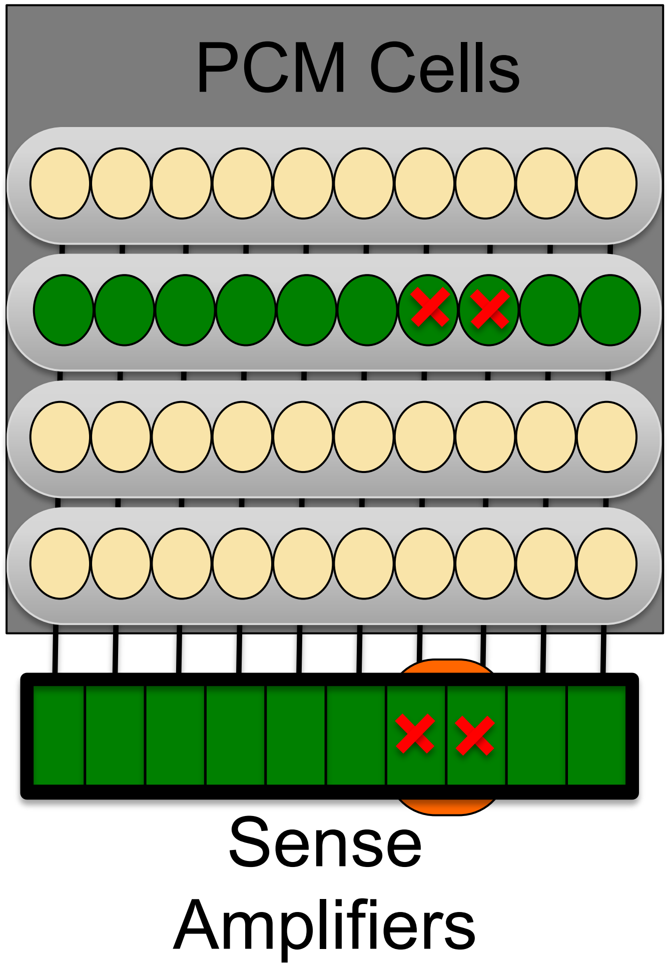

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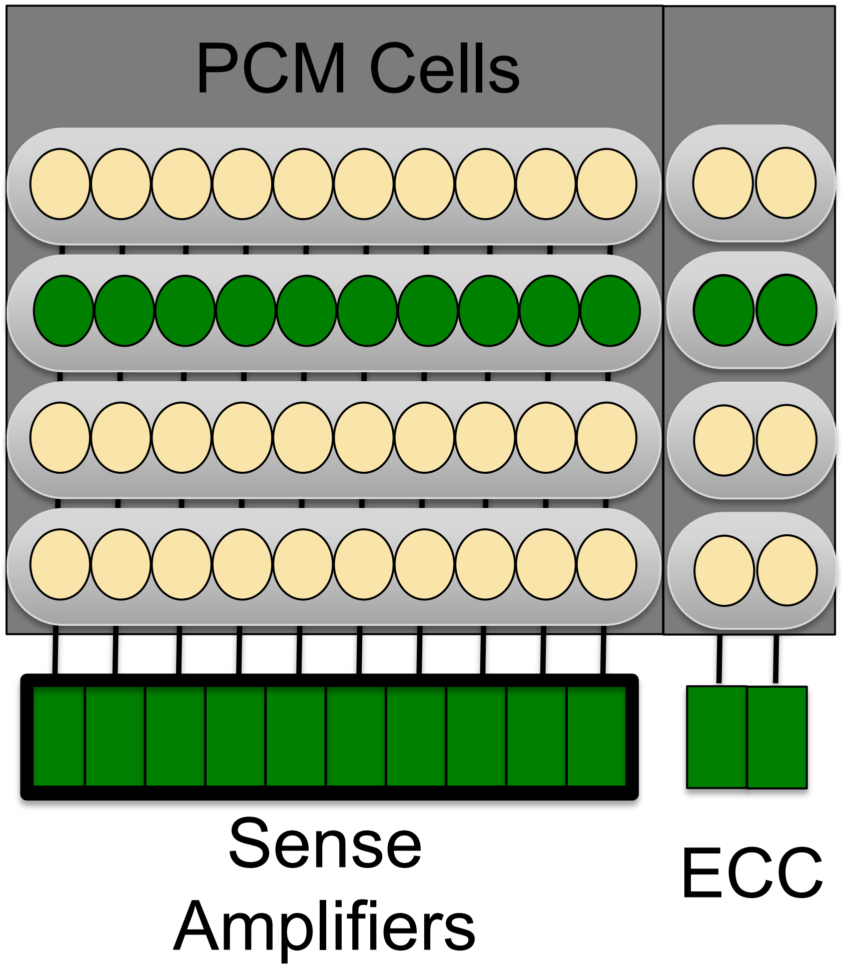

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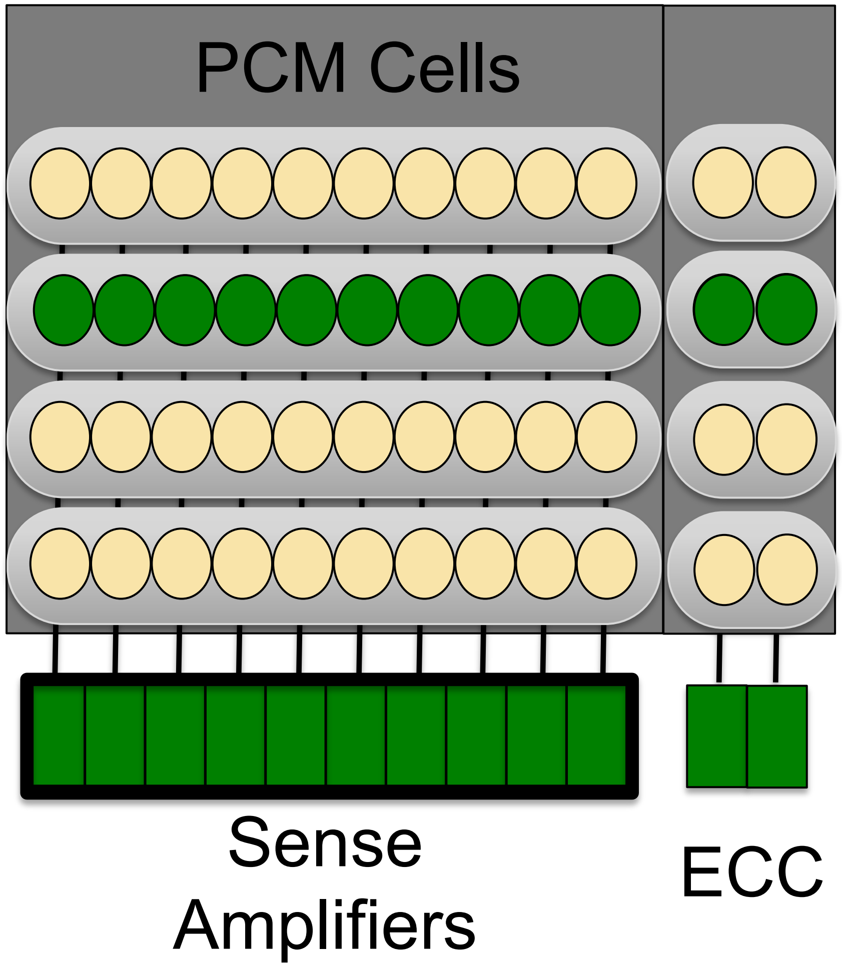
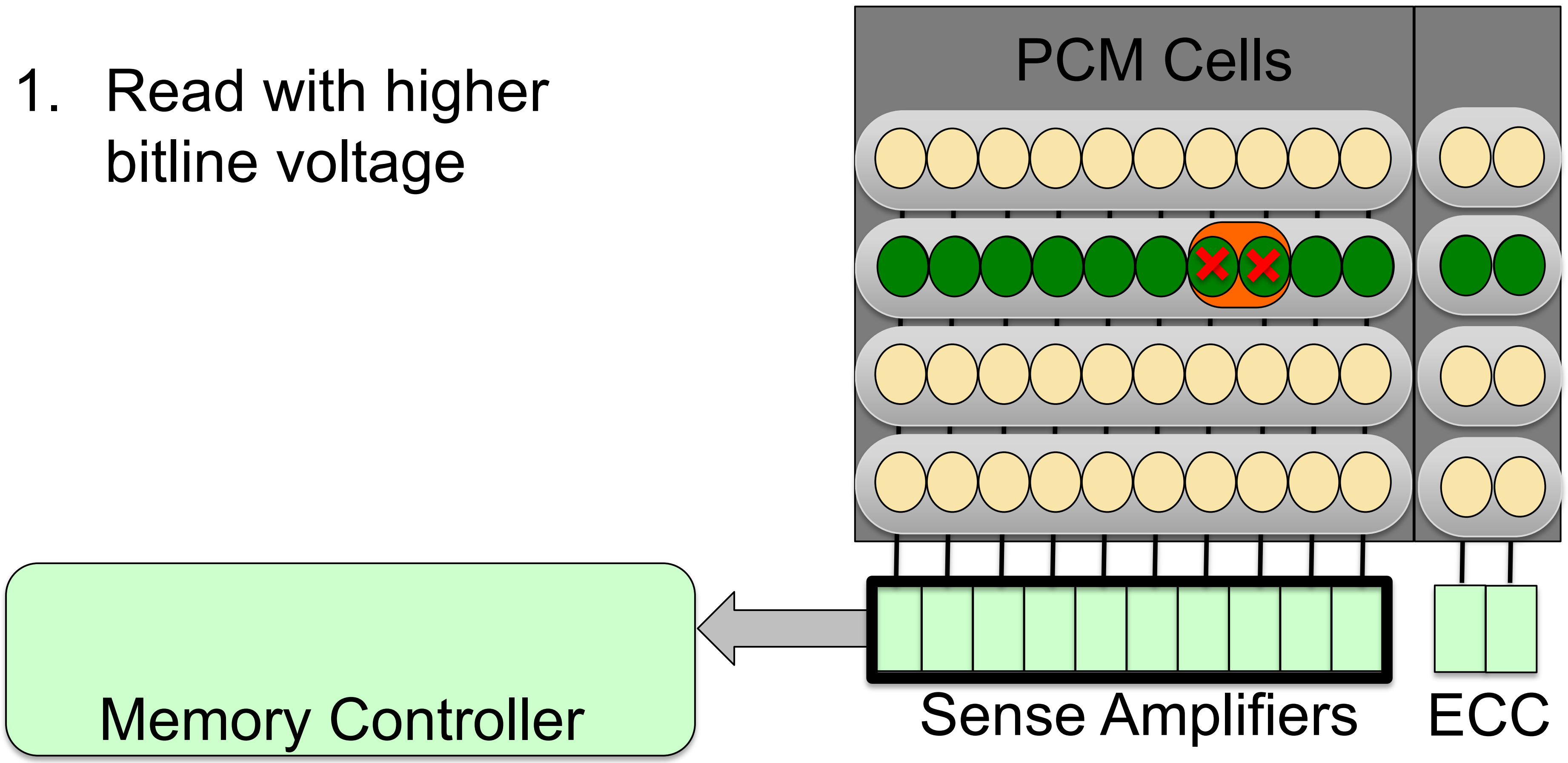


Correcting read disturb with ECC allows low latency read

TURBO READ

1. Read with higher bitline voltage



TURBO READ

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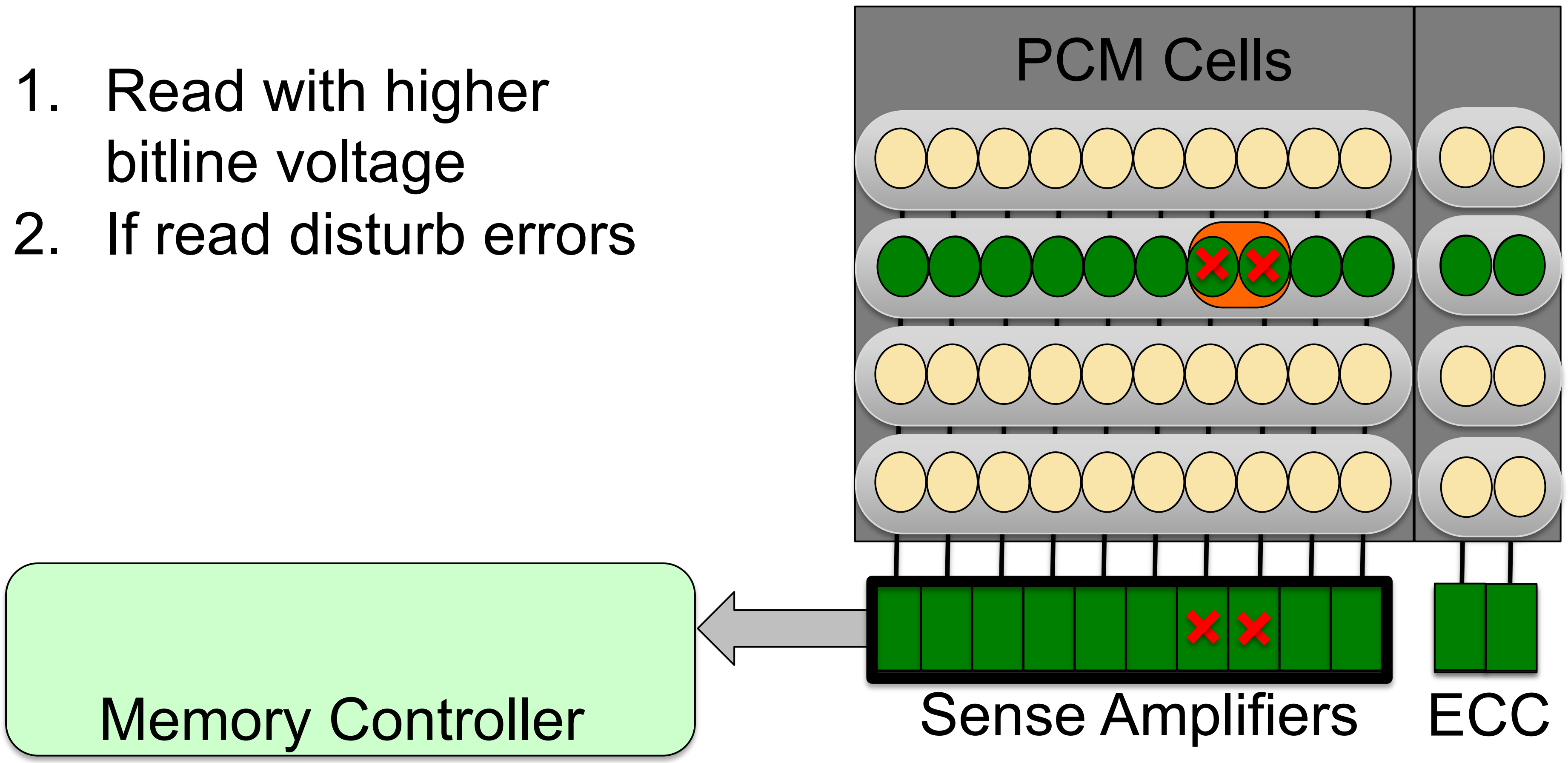
2. If read disturb errors



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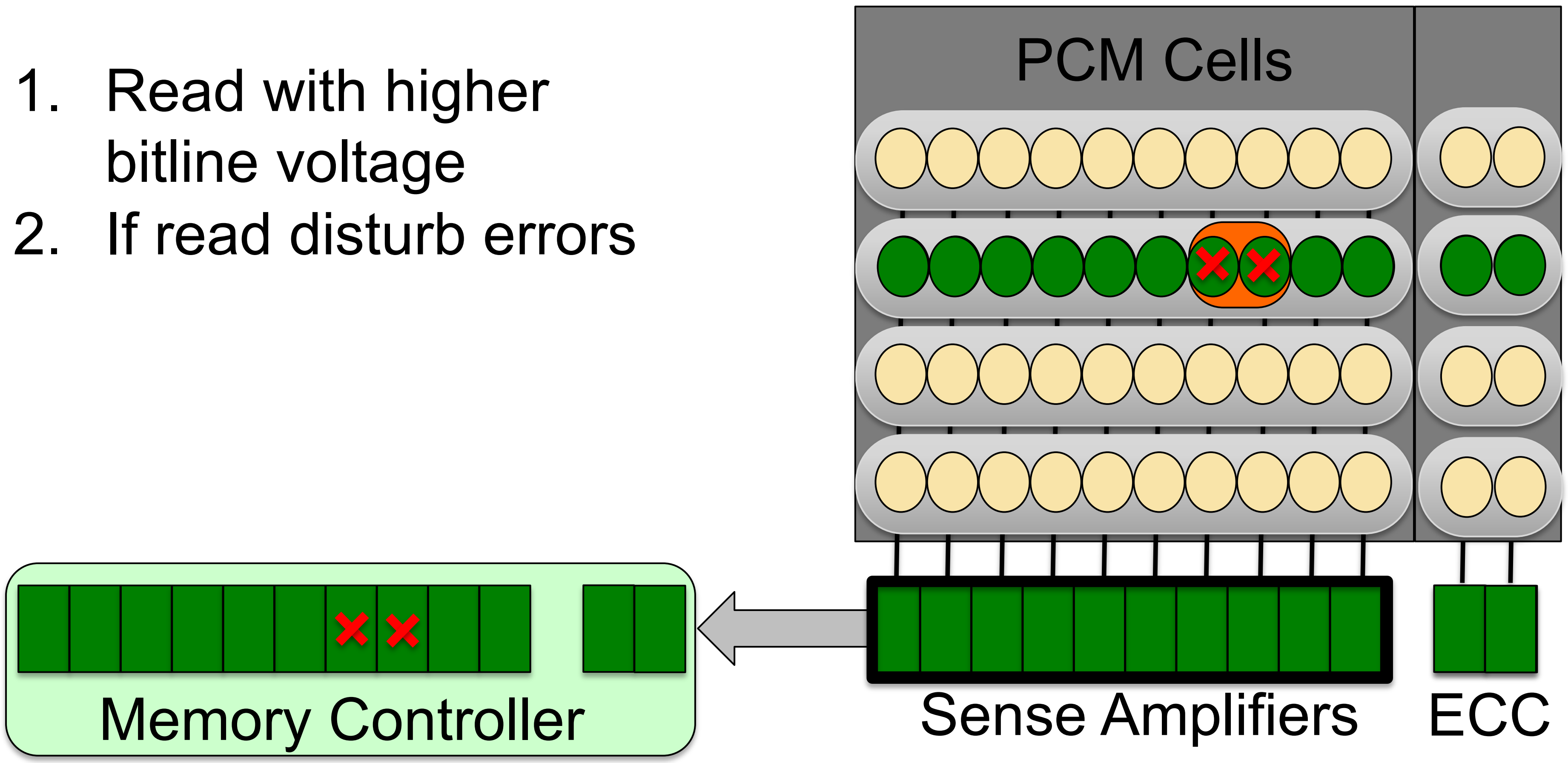

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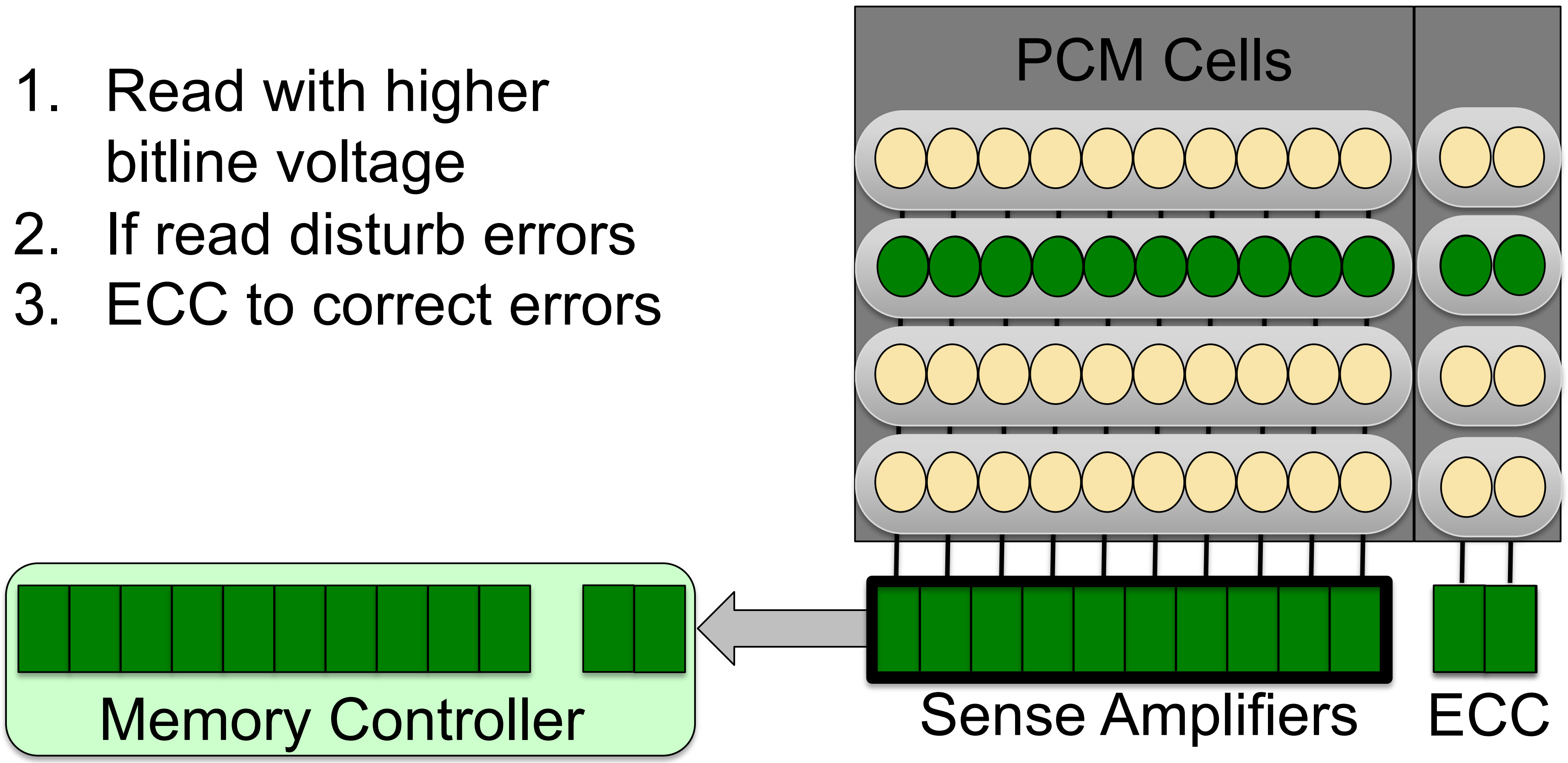

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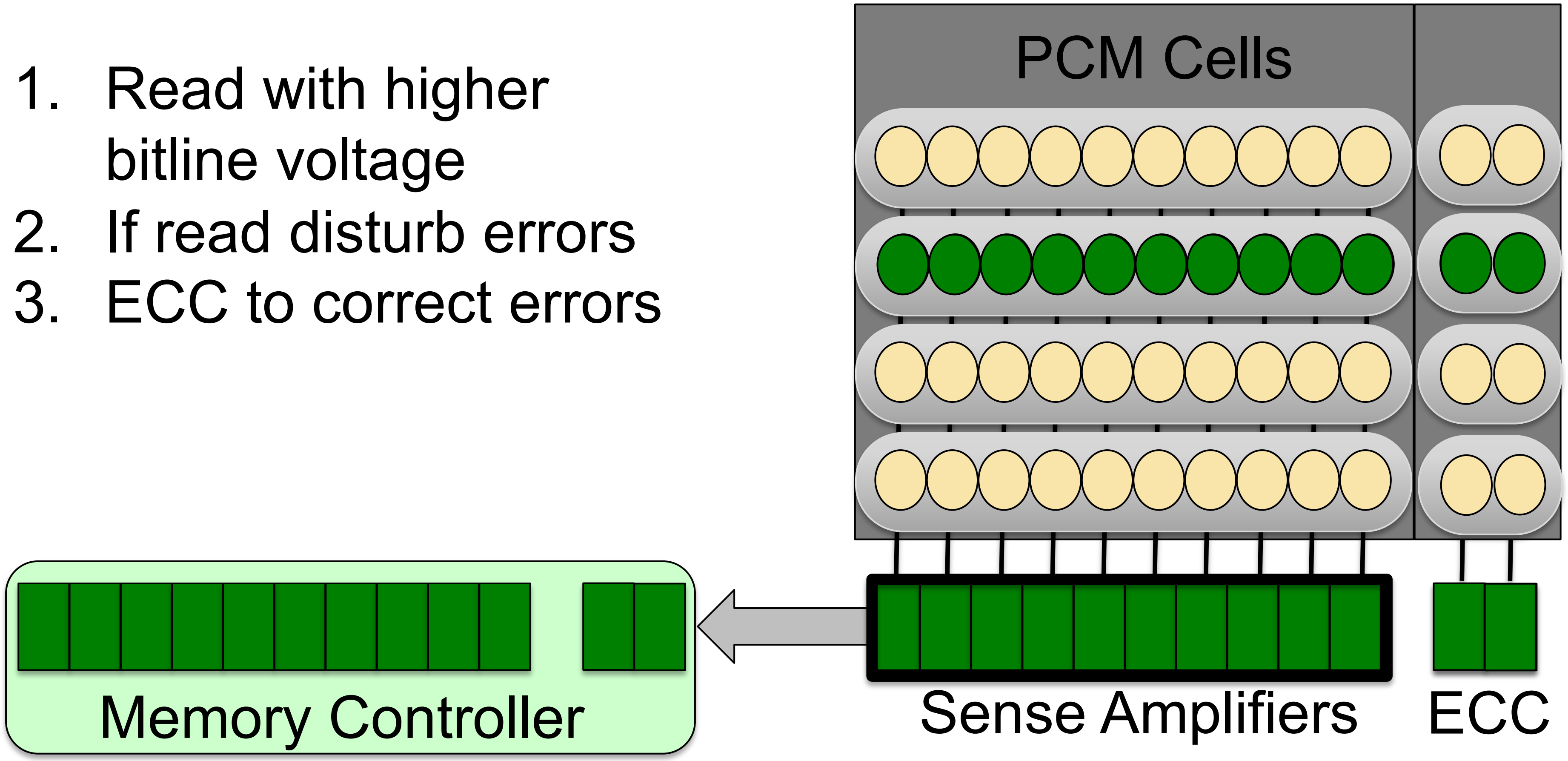

Turbo Read ➔ Read with higher bitline voltage and use ECC to correct read disturb errors

TURBO READ: DESIGN

- Systems are typically designed for failure rate < 10^{-16}
- Fix with a small amount of budget ➔ DECTED

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- Probabilistic Scrub (PRS) to mitigate latent faults

ECC can mitigate read disturb errors in Turbo Read

OUTLINE

WHY COMBINE EARLY AND TURBO READ

Early read➔Error➔Retry

– Bimodal Read Latency

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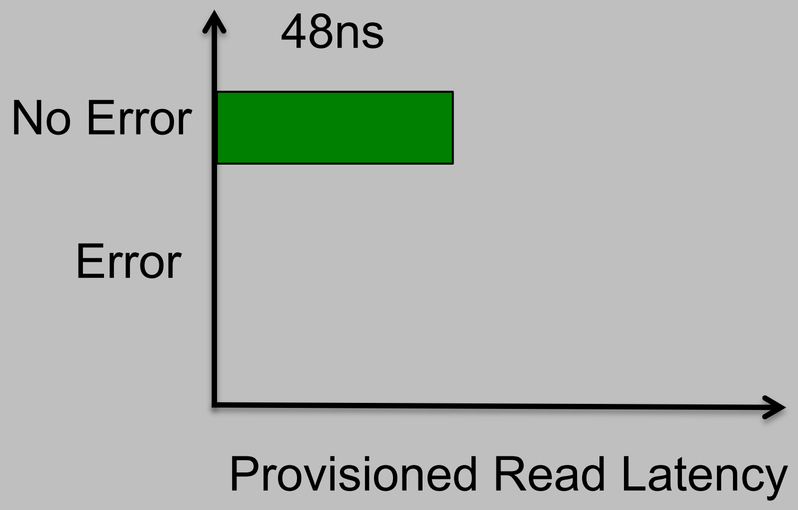

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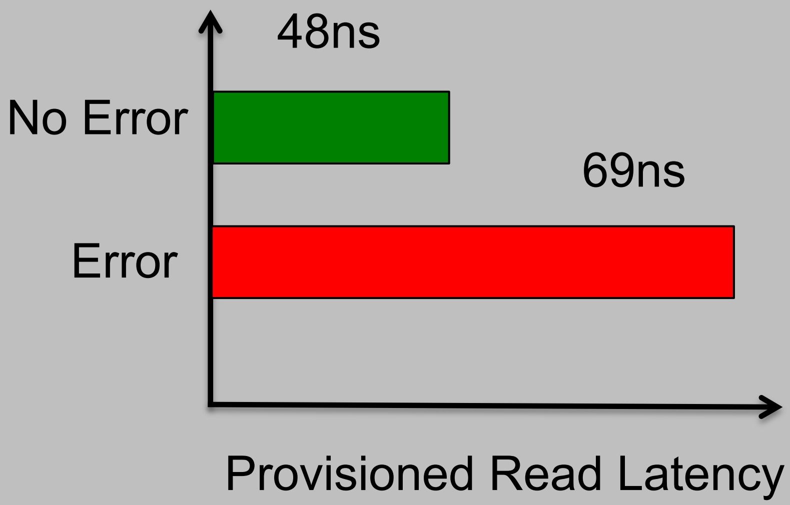

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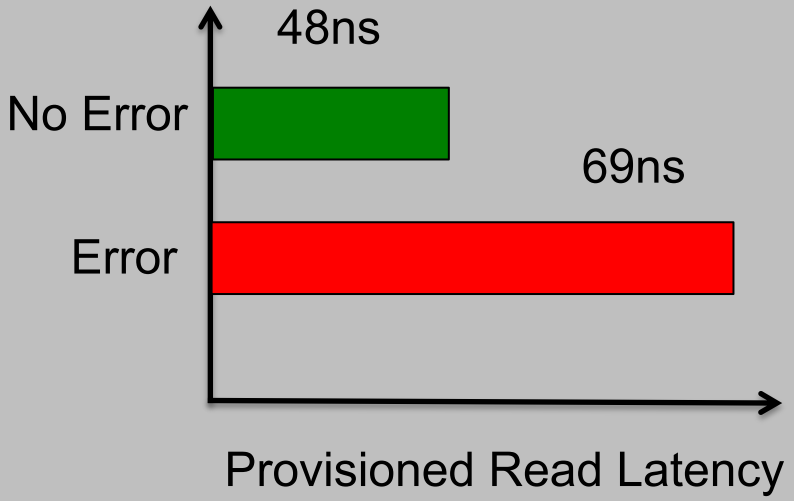

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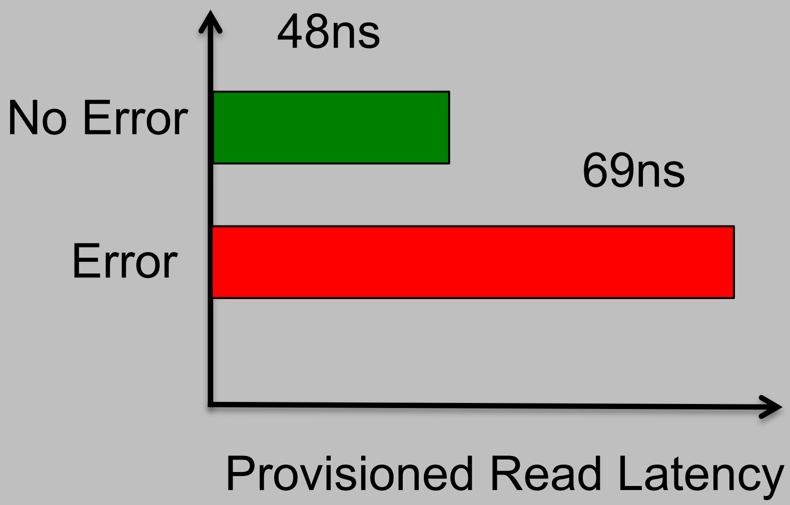

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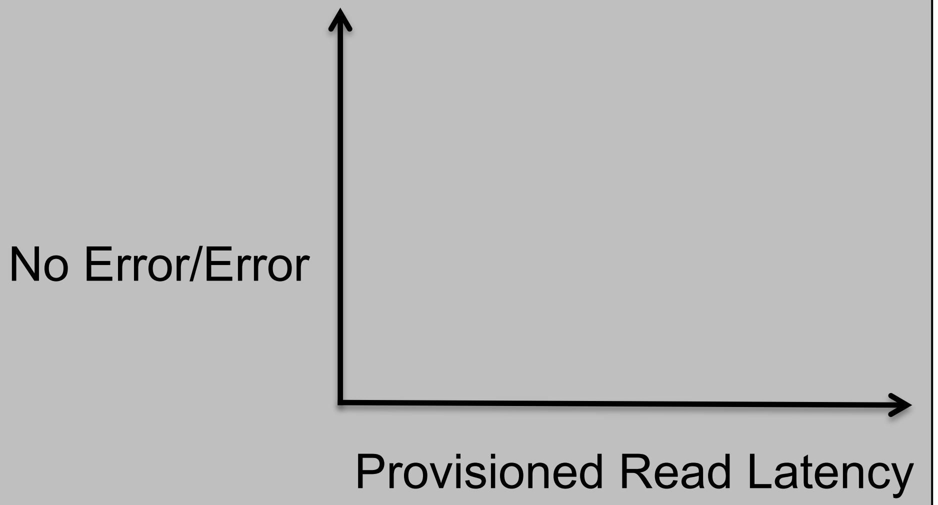

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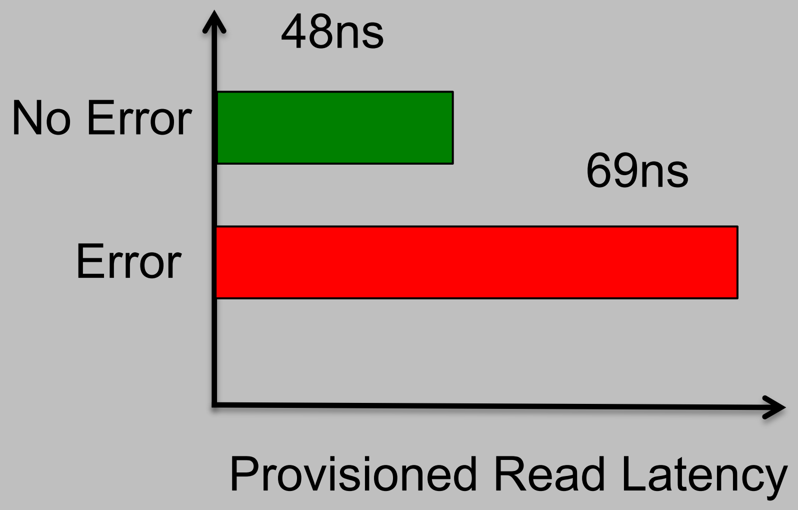

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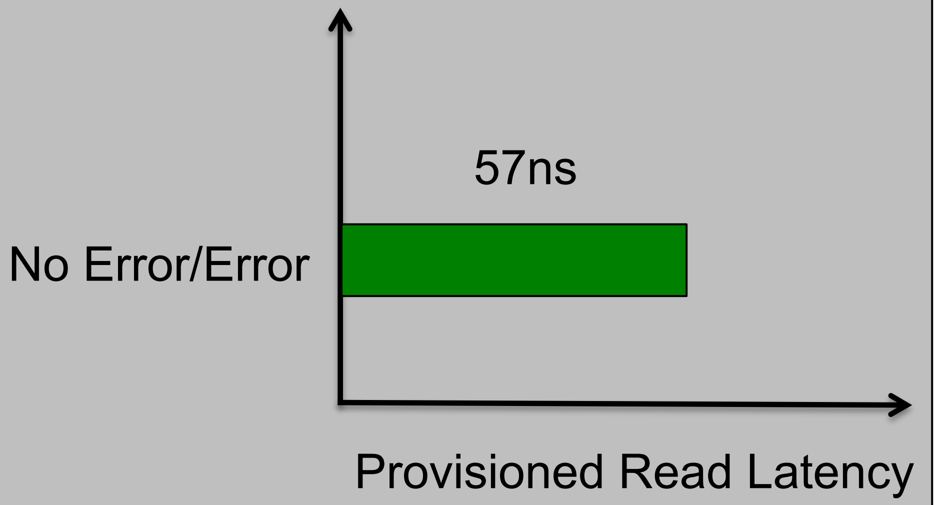

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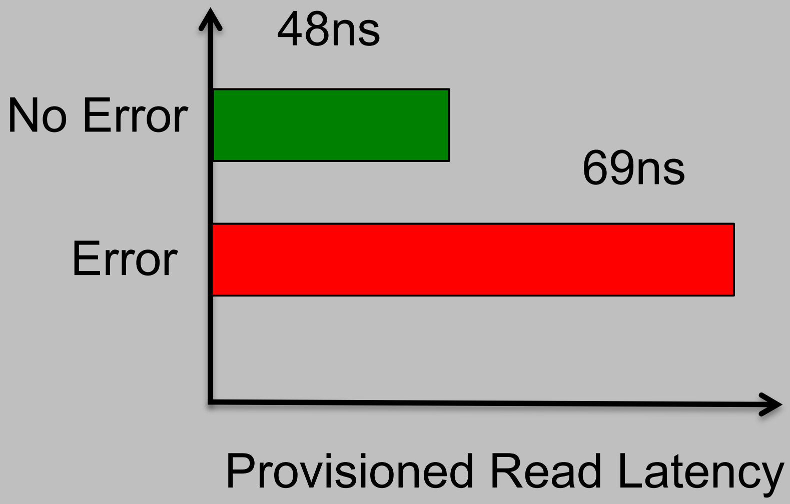

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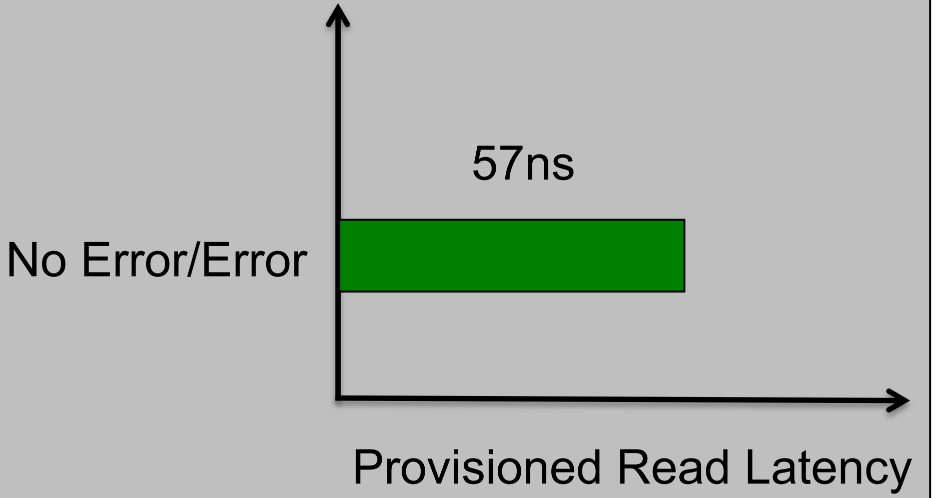
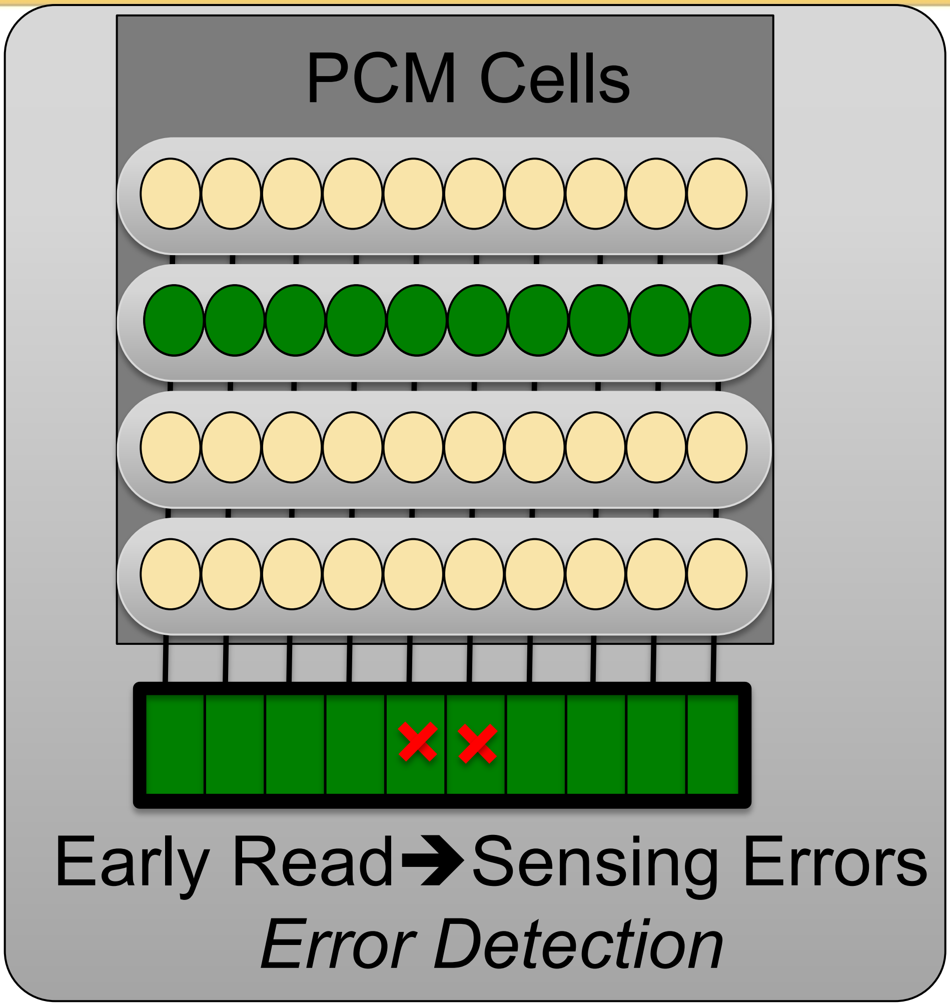


Combine Early and Turbo Reads ➔ Get benefits of both without bimodal latency

CHALLENGES IN EARLY+TURBO READ



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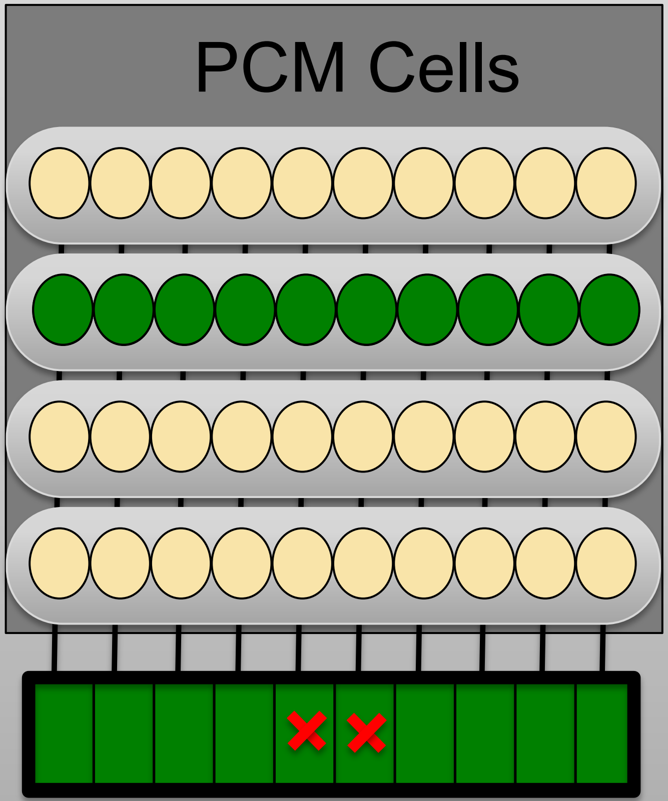
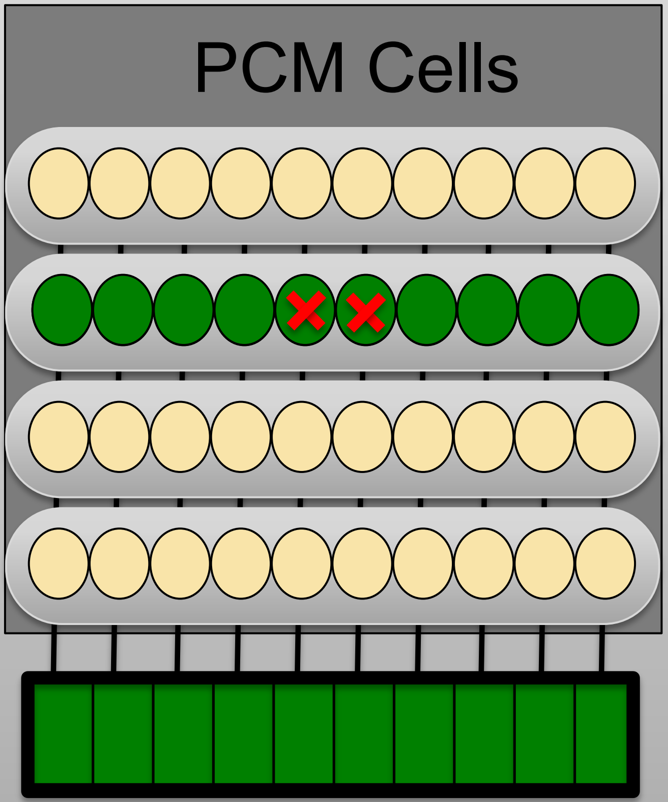


Early Read→Sensing Errors

Error Detection



Turbo Read→PCM Cell Errors

Error Correction

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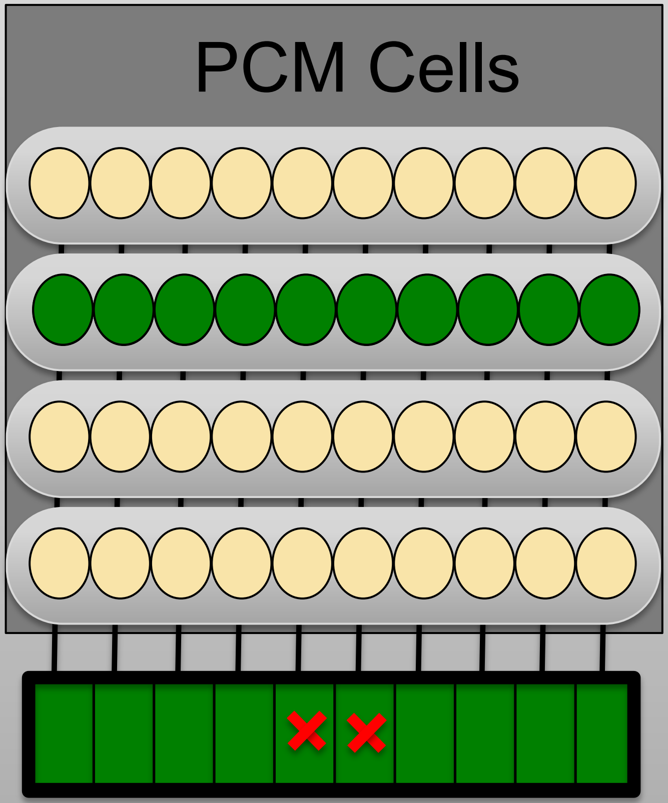

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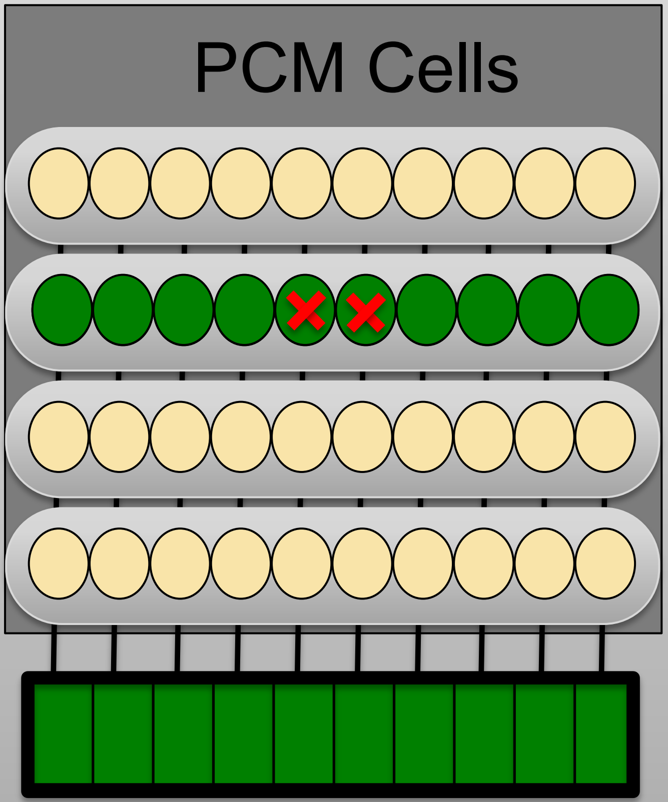


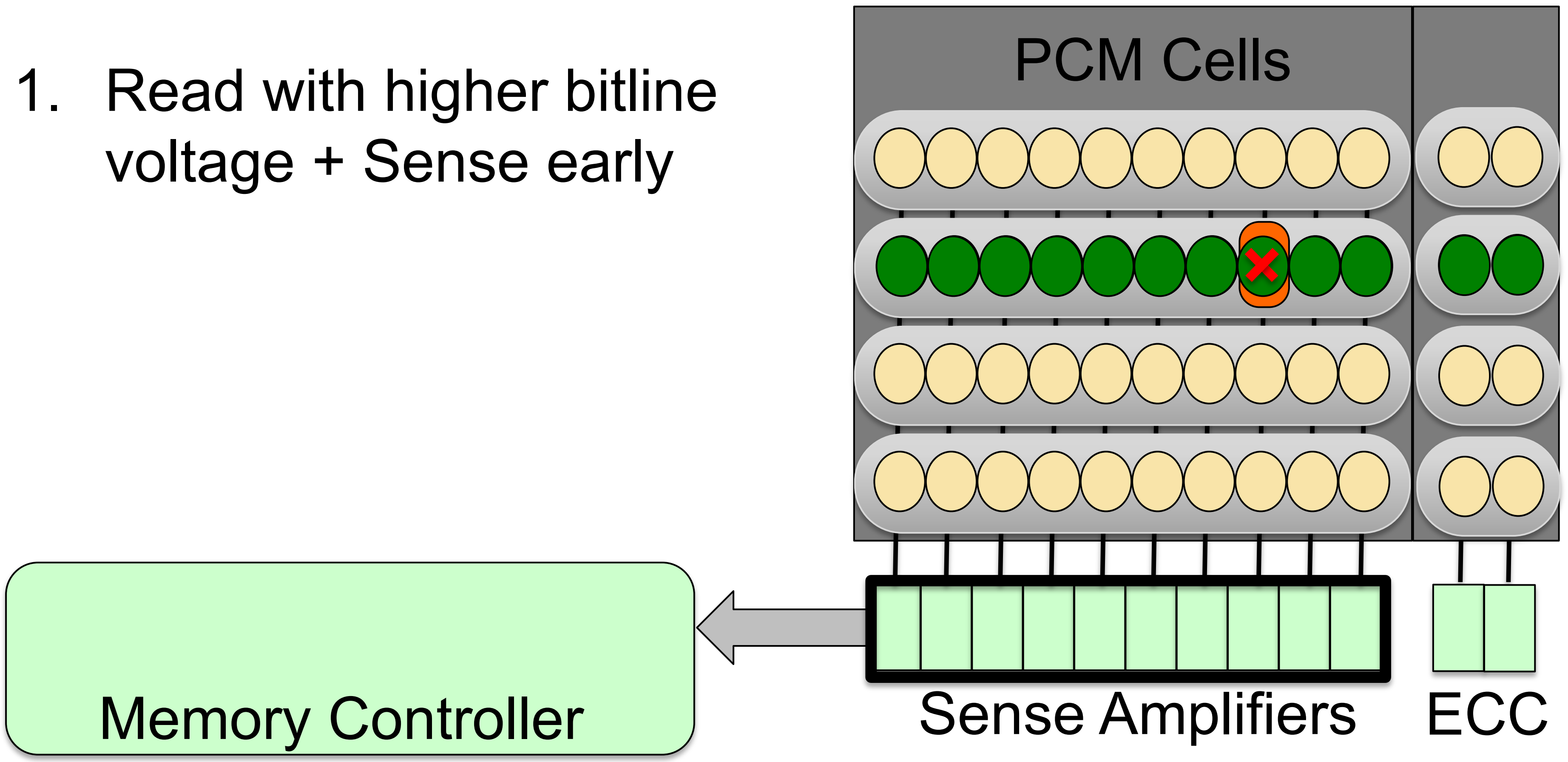
Turbo Read➔PCM Cell Errors

Error Correction

Early+Turbo Read will have PCM cell errors and require Error Correcting Codes

EARLY+TURBO READ

1. Read with higher bitline voltage + Sense early



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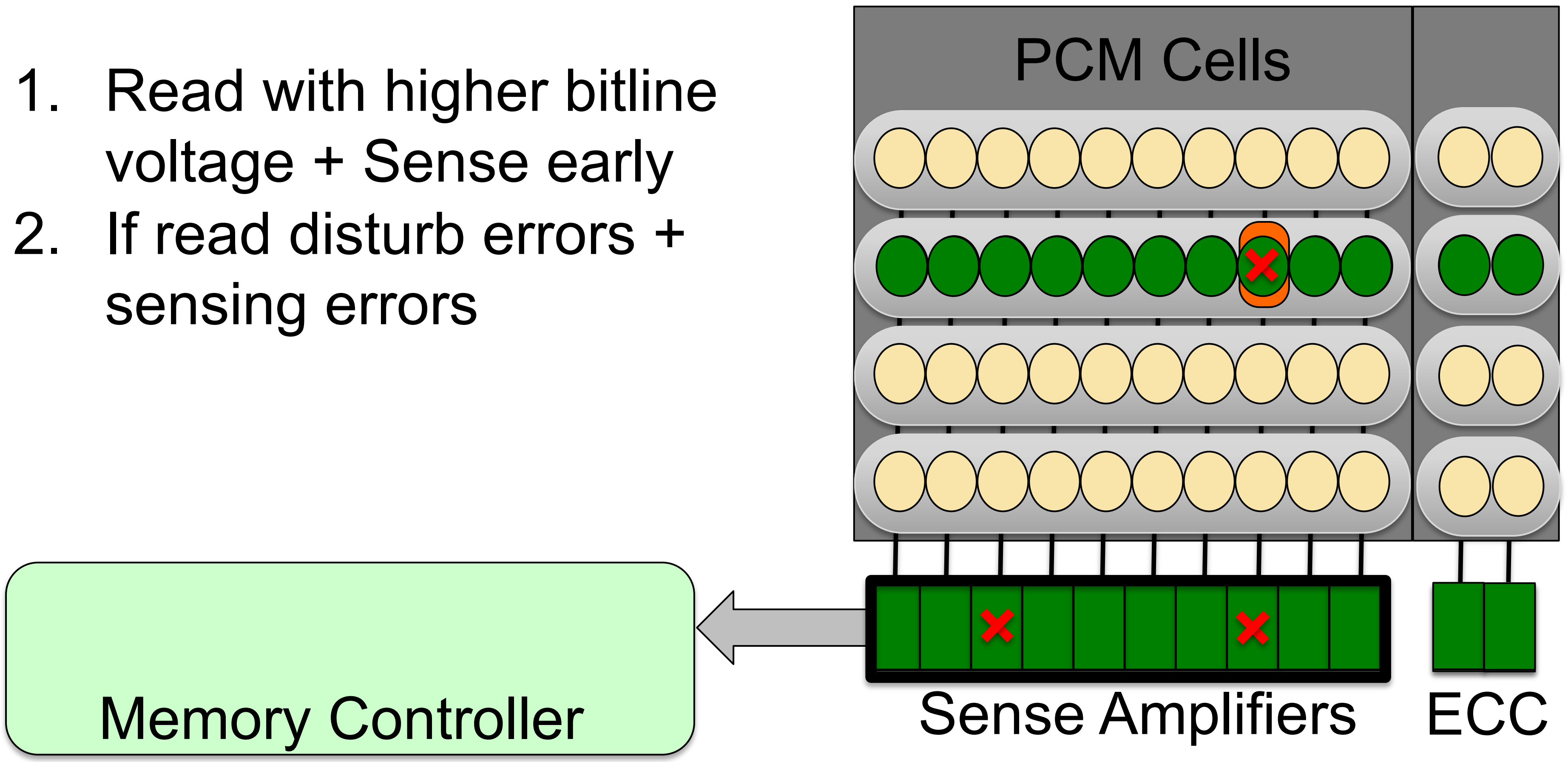

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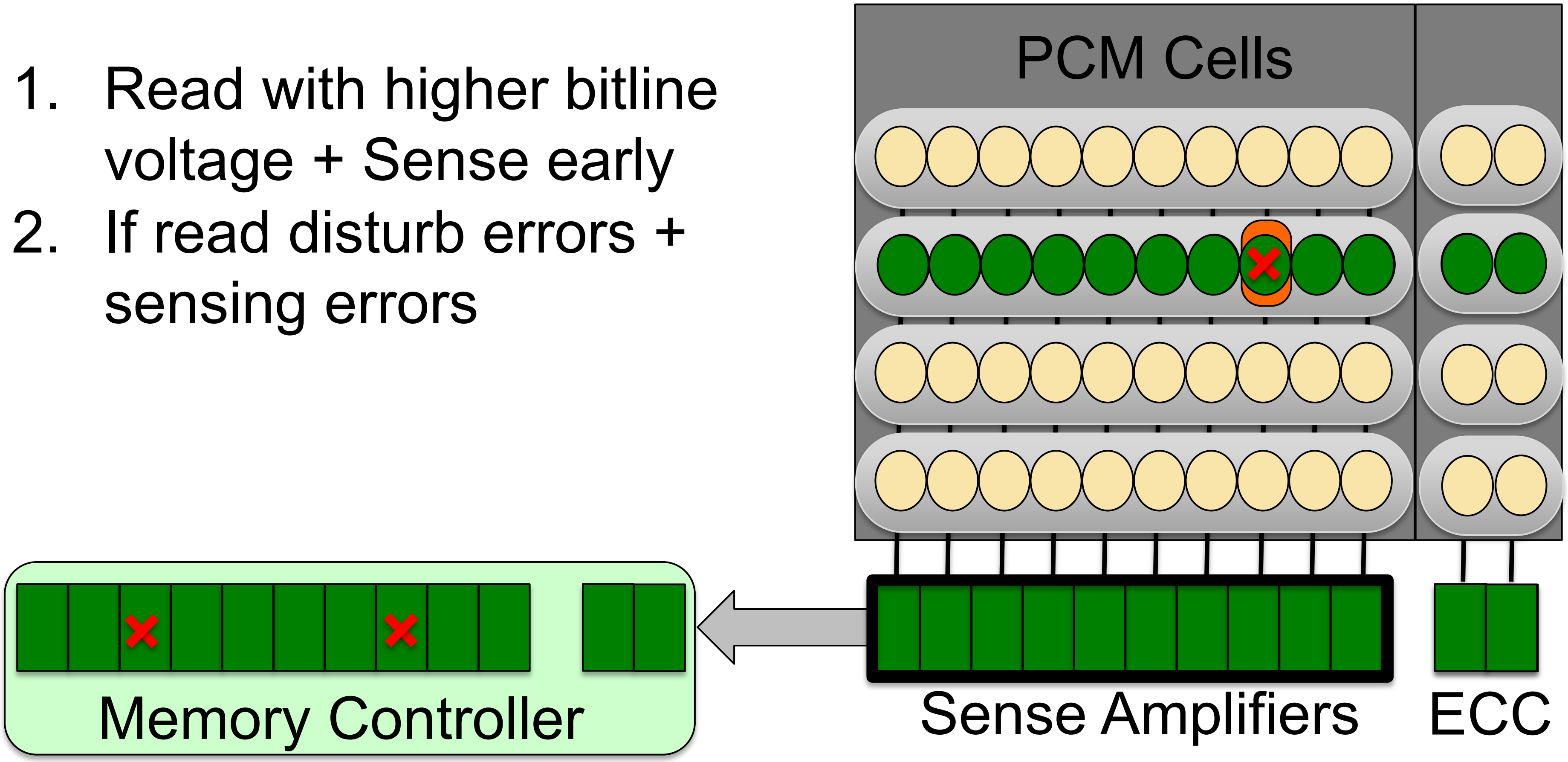

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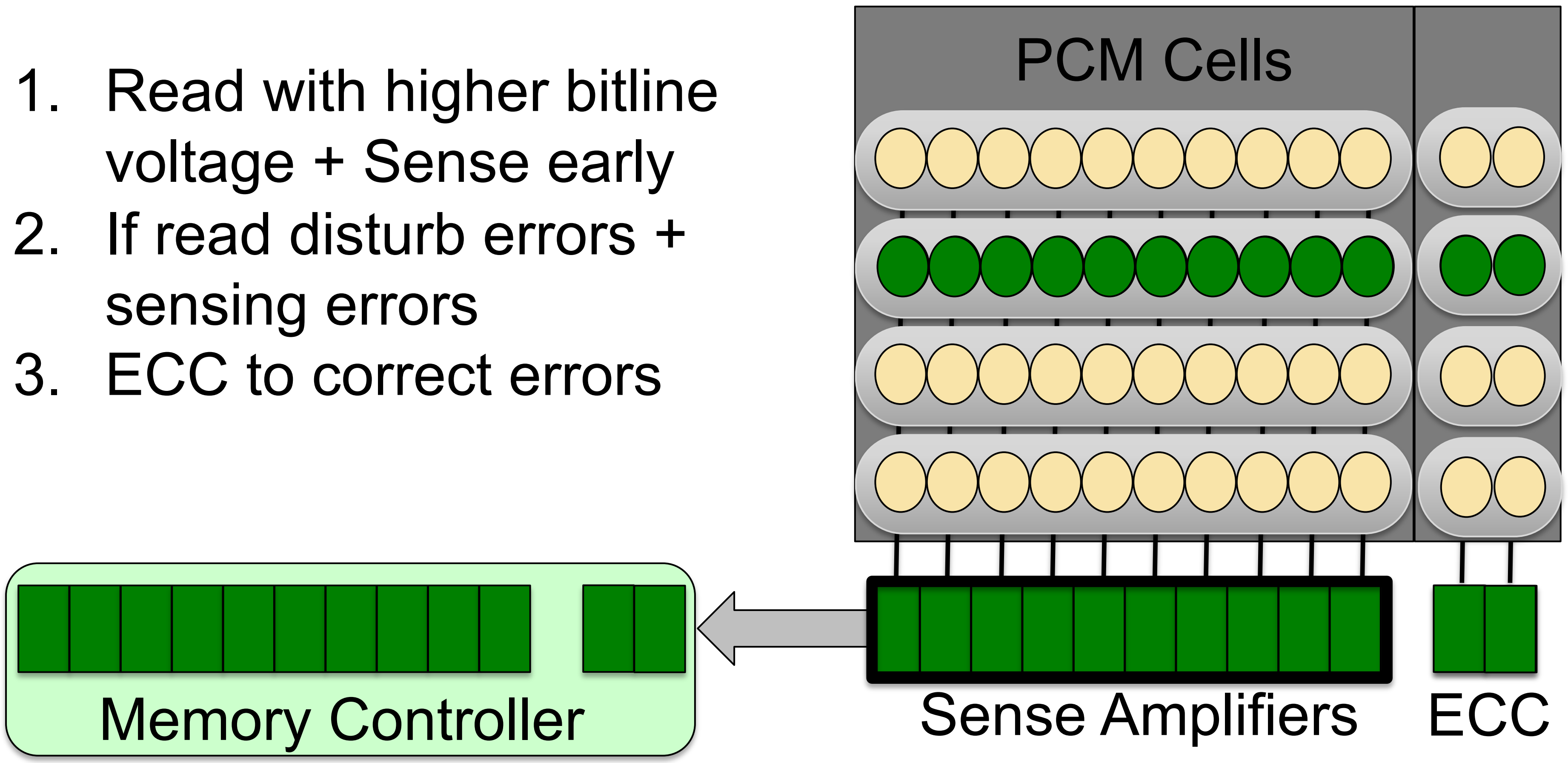

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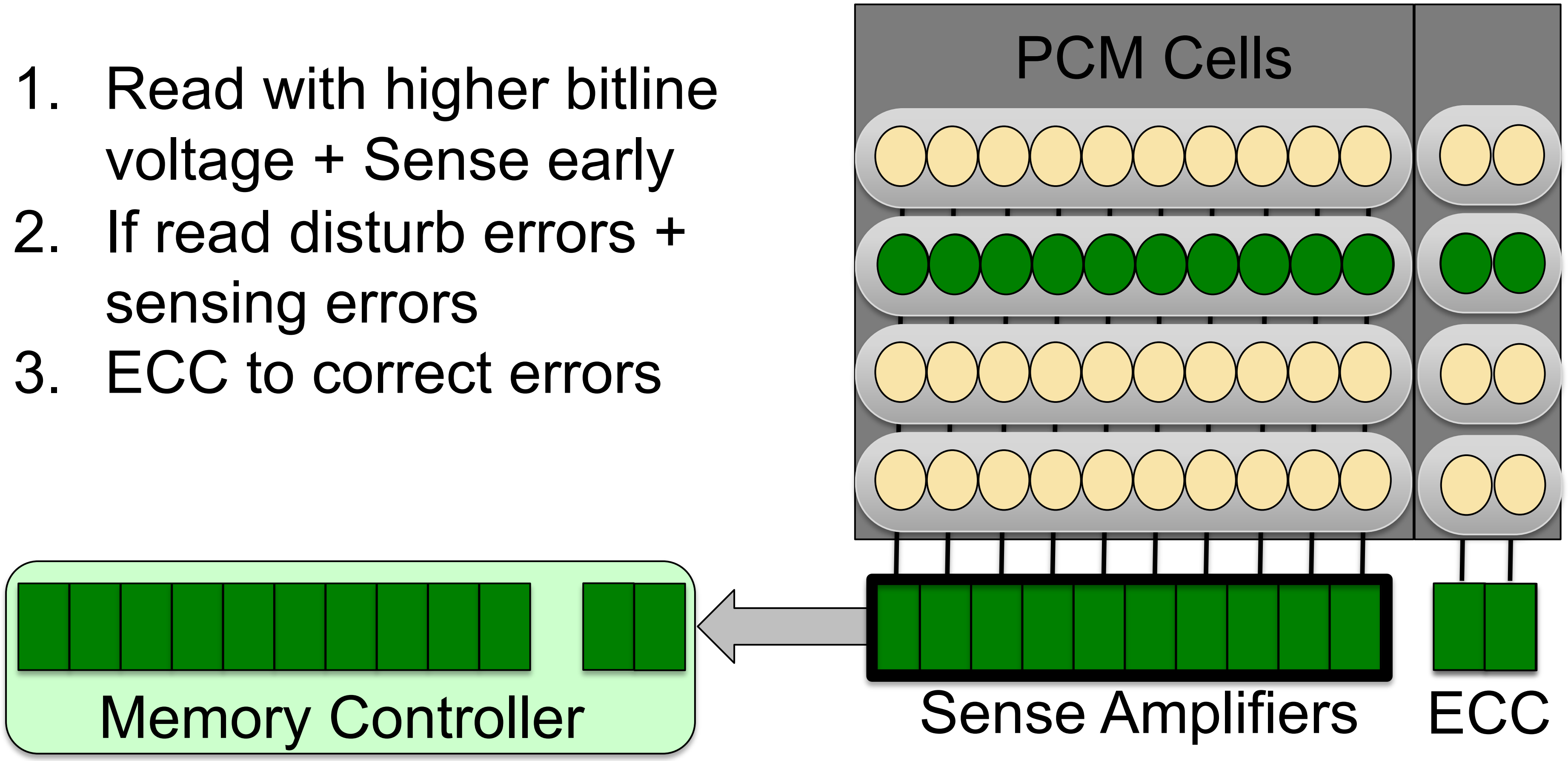

Early+Turbo Read ➔ Read with higher bitline voltage and sense early ➔ Use ECC to correct errors

EARLY+TURBO READ: DESIGN

	Early Read	Turbo Read	Early+Turbo Read
BER	10^{-5}	10^{-9}	$2x10^{-9}$
Sensing Latency	48ns or 69ns (Bimodal)	57ns (Fixed)	45ns (Fixed)
Storage Overhead	10 bits/line	20 bits/line	20 bits/line

- $2x10^{-9}$ BER ➔ DECTED ➔ System Failure Rate < 10^{-19}

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Early+Turbo Read reduces read latency by 30%

OUTLINE

- Background
- Early Read
- Turbo Read
- Early+Turbo Read
- Results
- Summary

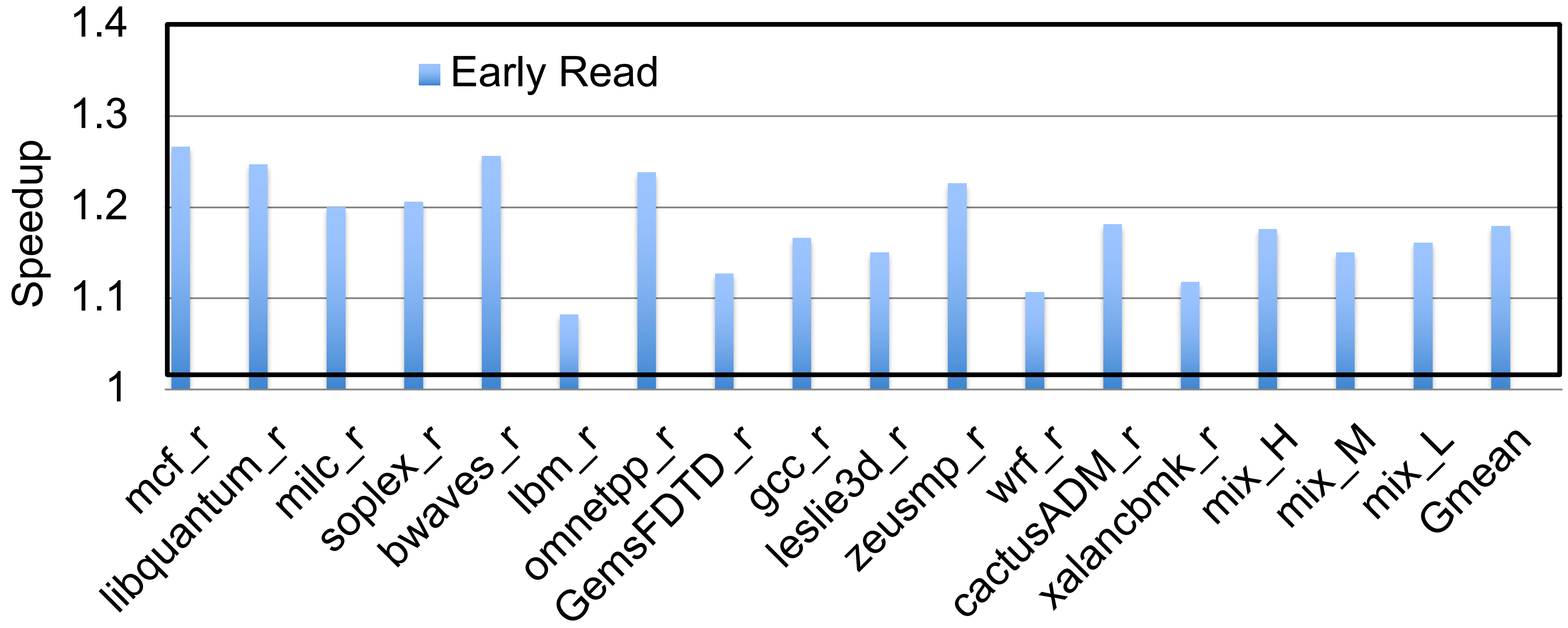
SYSTEM CONFIGURATION

Parameter	Configuration
Cores	8 cores @ 3Ghz
L1-L2-L3 Cache	32KB-256KB-1MB (Private)
L4 Cache	128MB (Shared) @ 15ns latency
PCM System	
Channels	4 Channels @ 8GB/Channel
Read Latency	80ns → 69ns sensing time*
Write Latency	250ns*

Spec Benchmarks with read MPKI from DRAM Cache > 1

* ISSCC 2012 [PCM-Samsung]

PERFORMANCE



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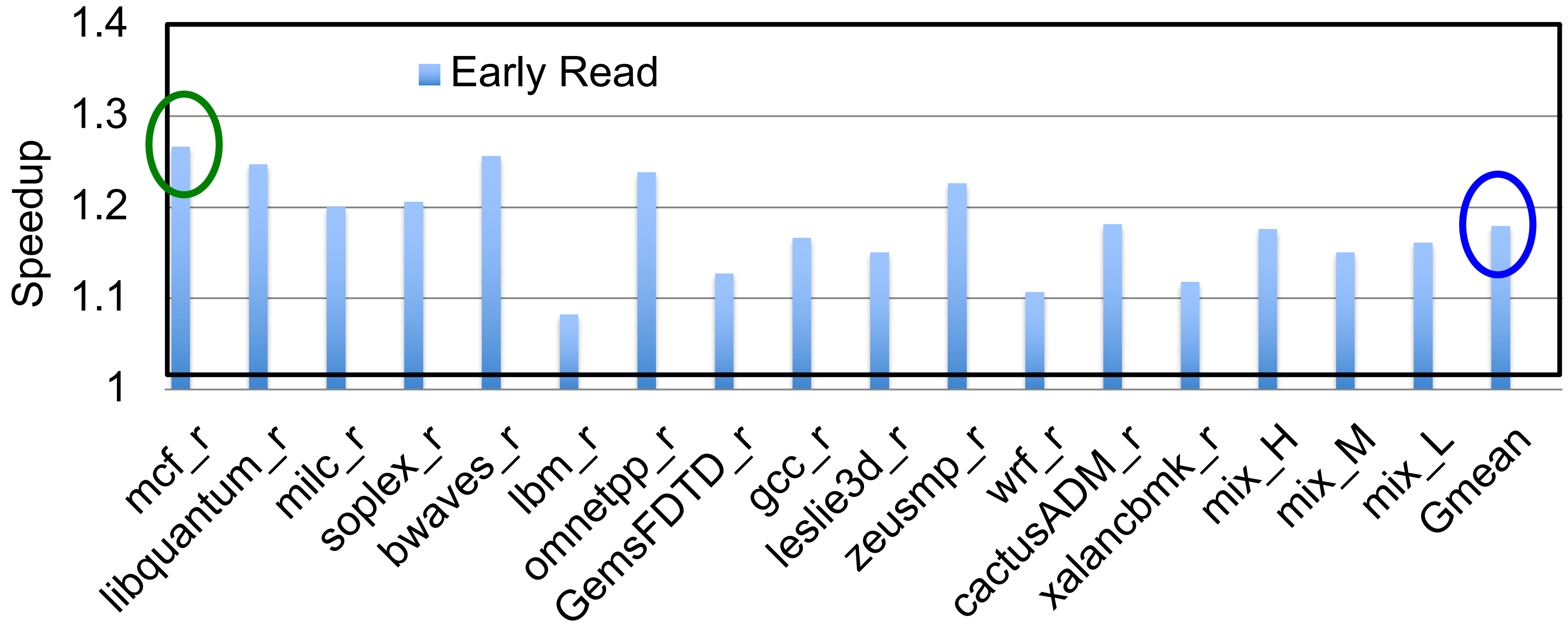

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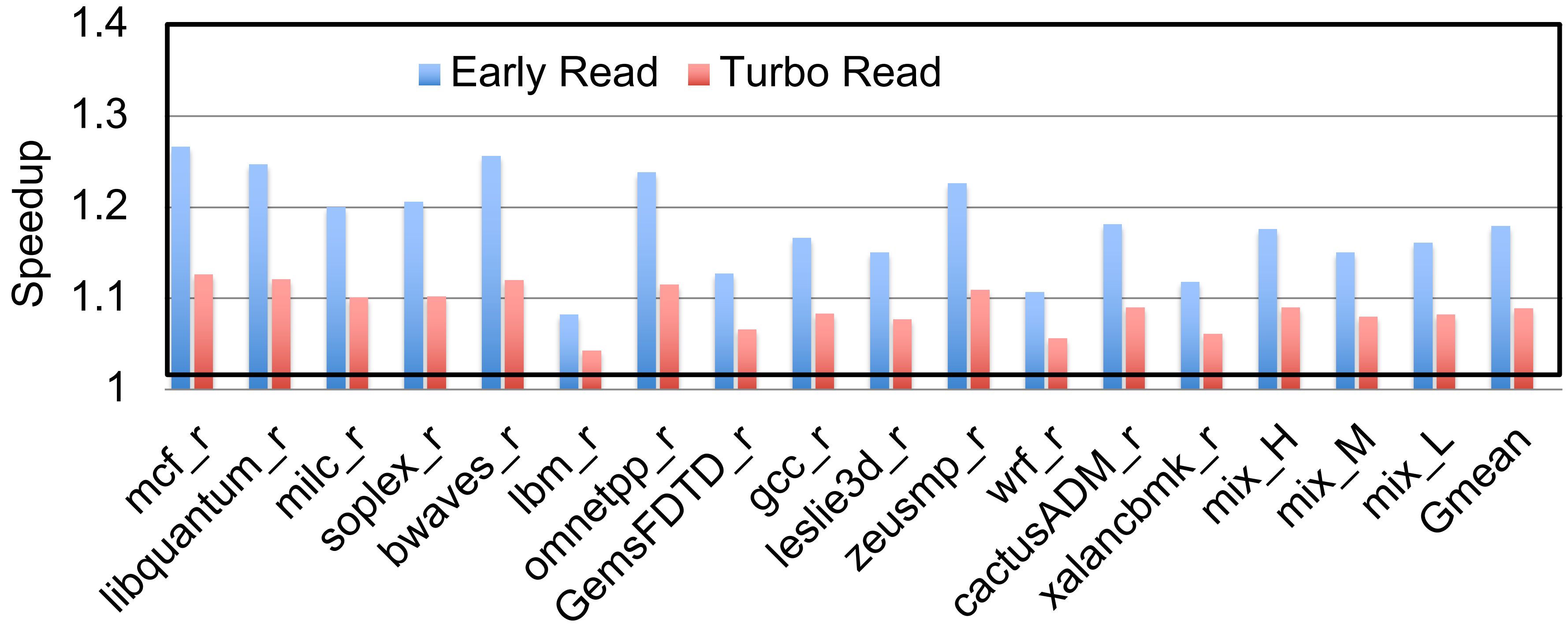

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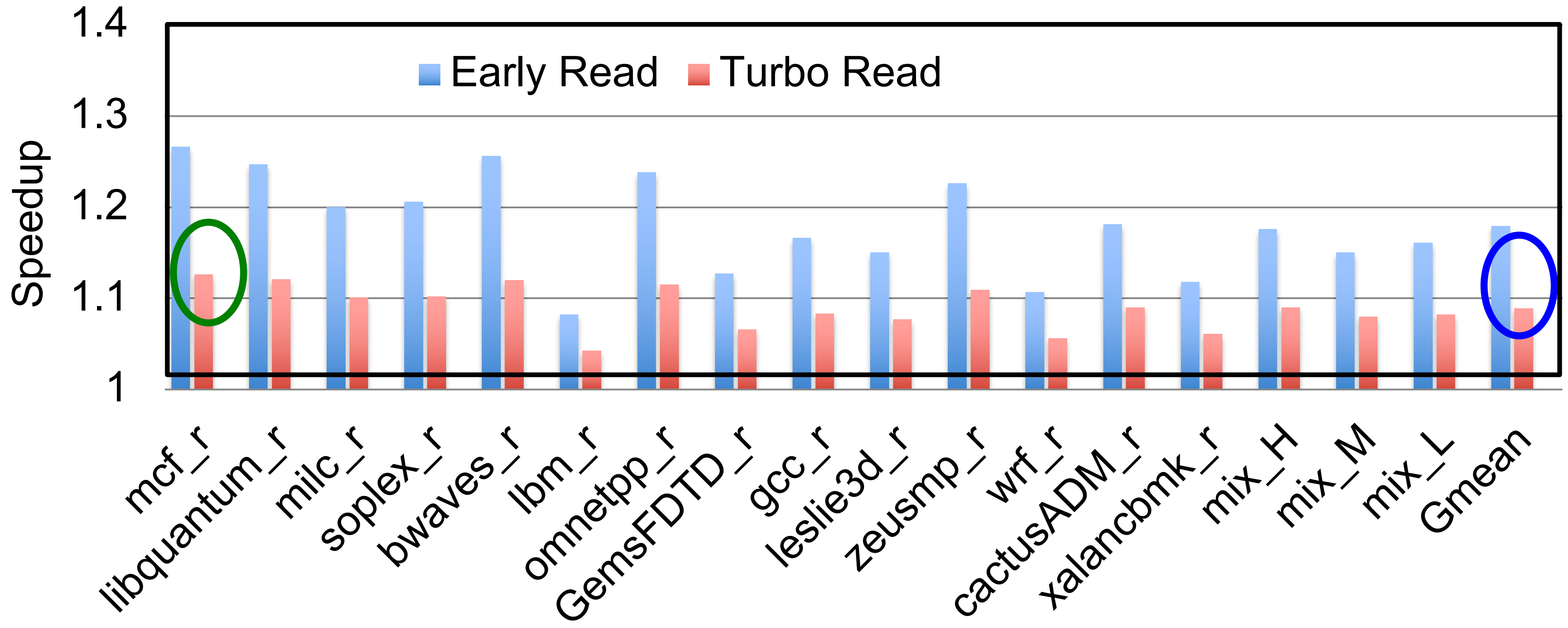

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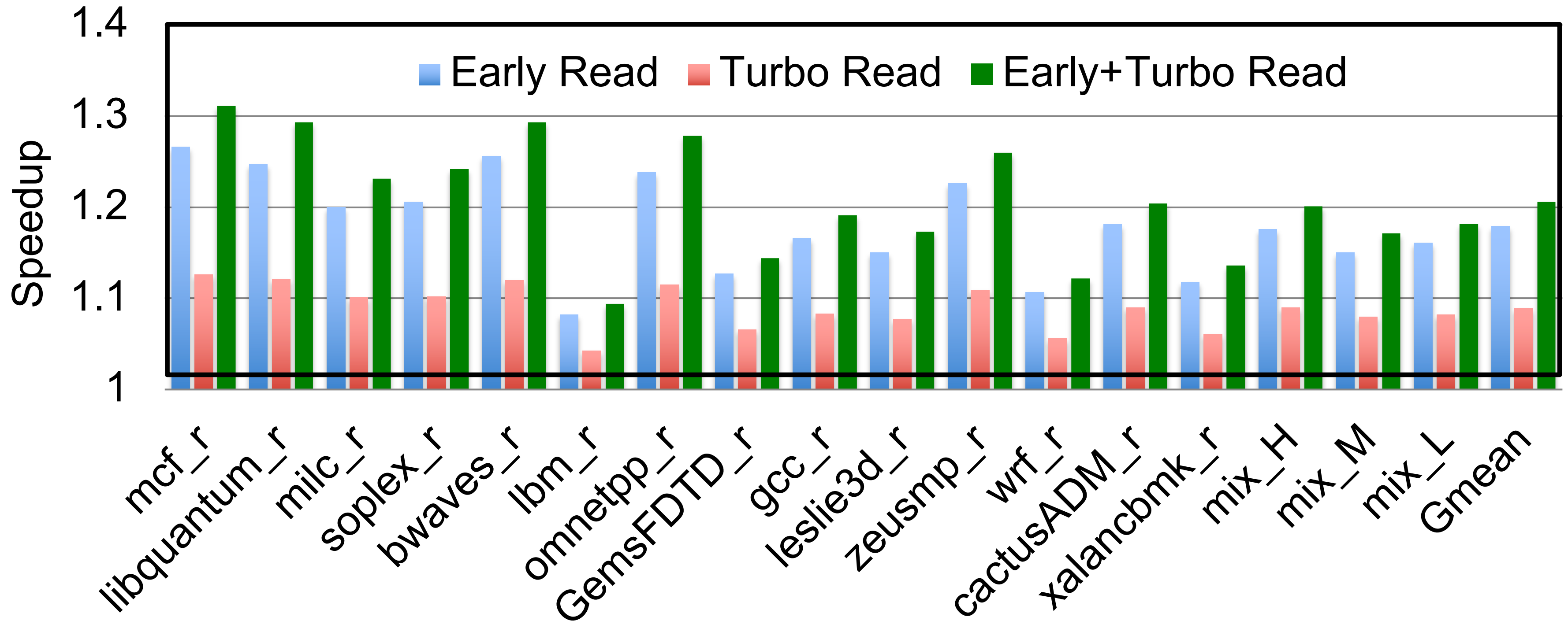

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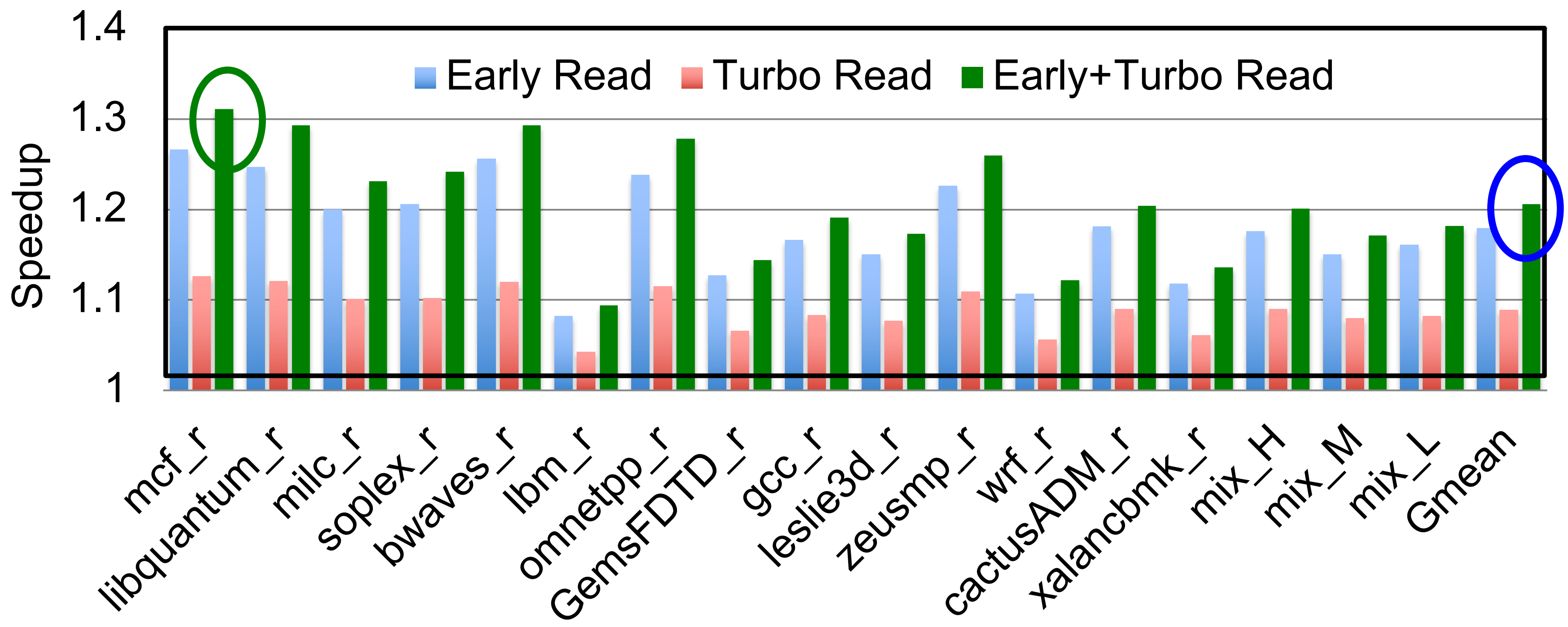

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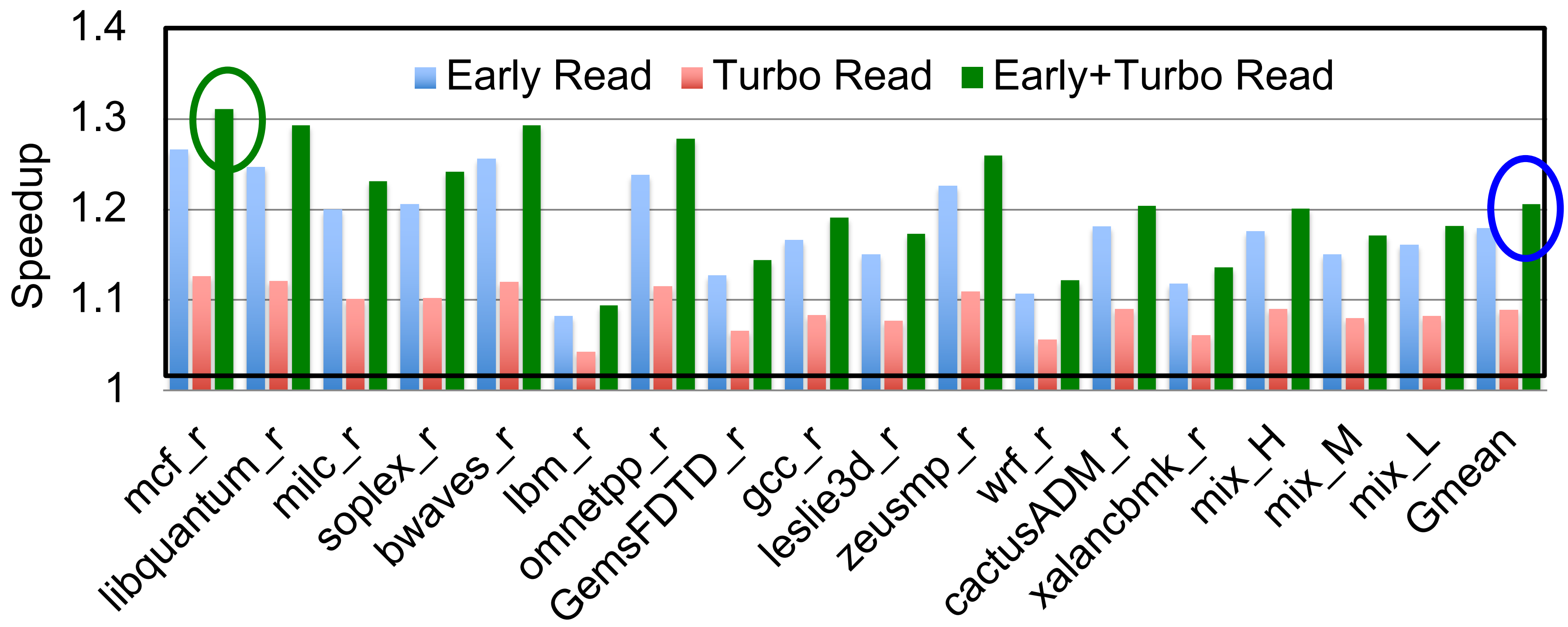
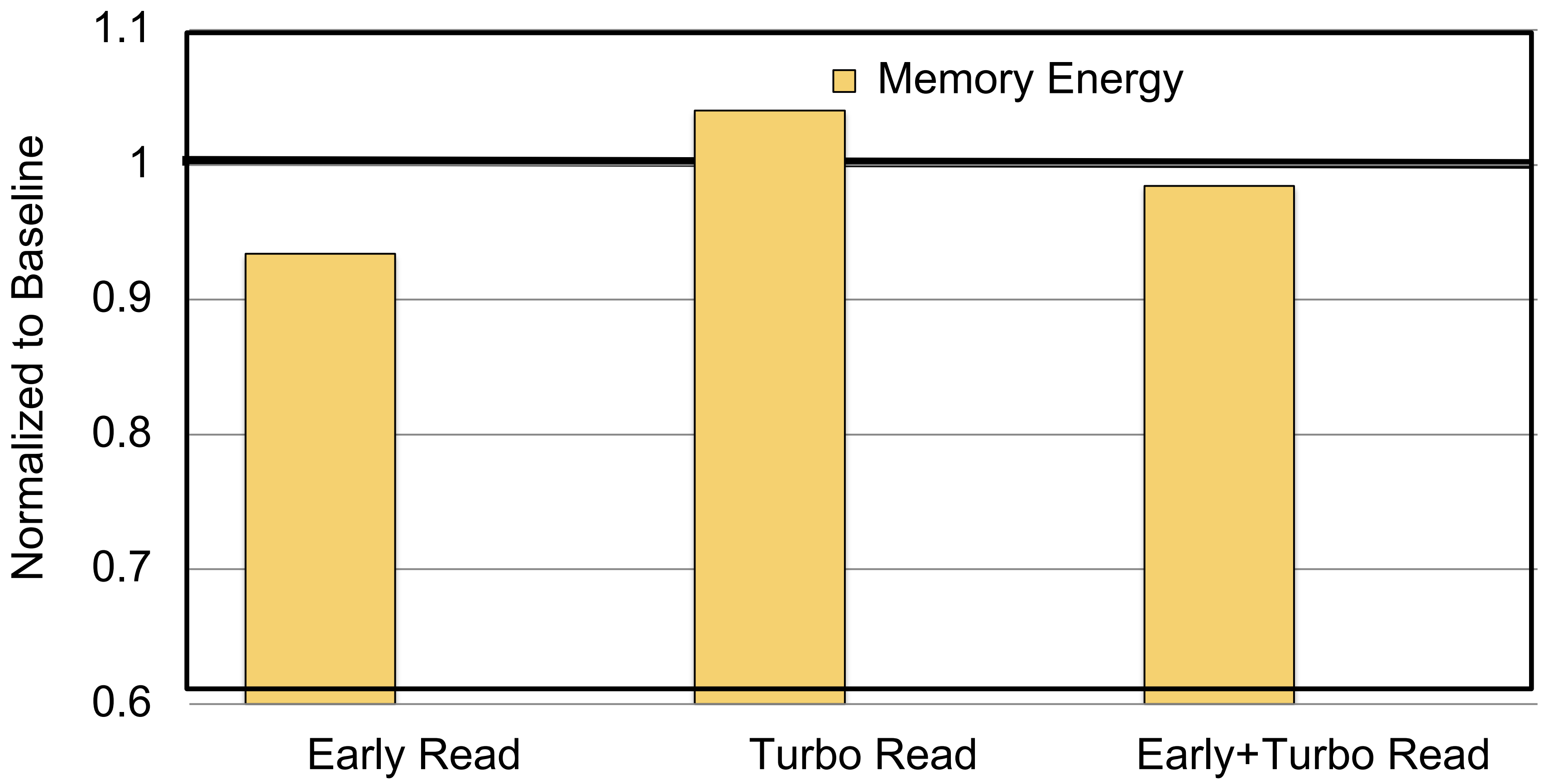


Our proposals improve performance by upto 21%

ENERGY AND EDP



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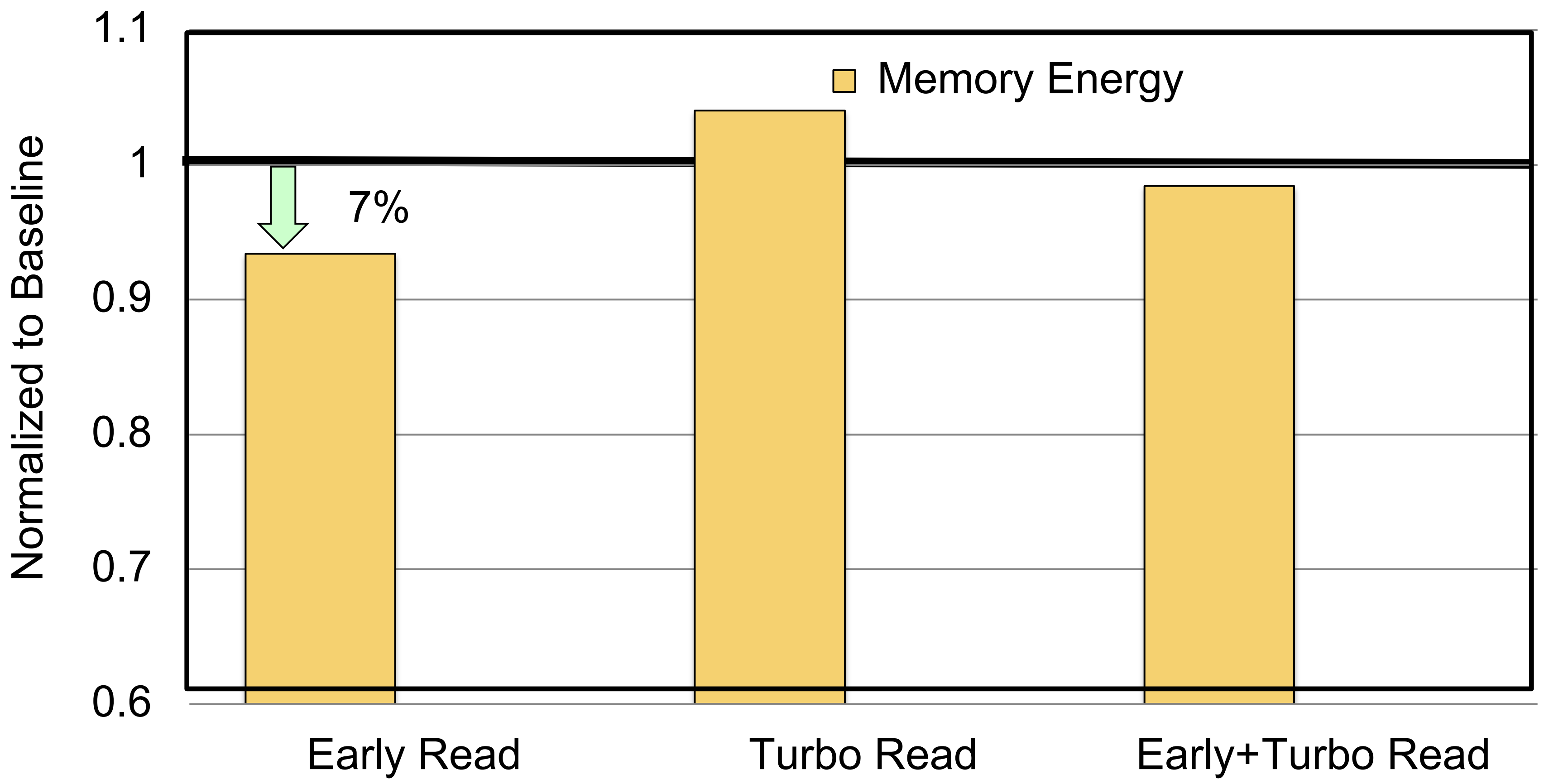

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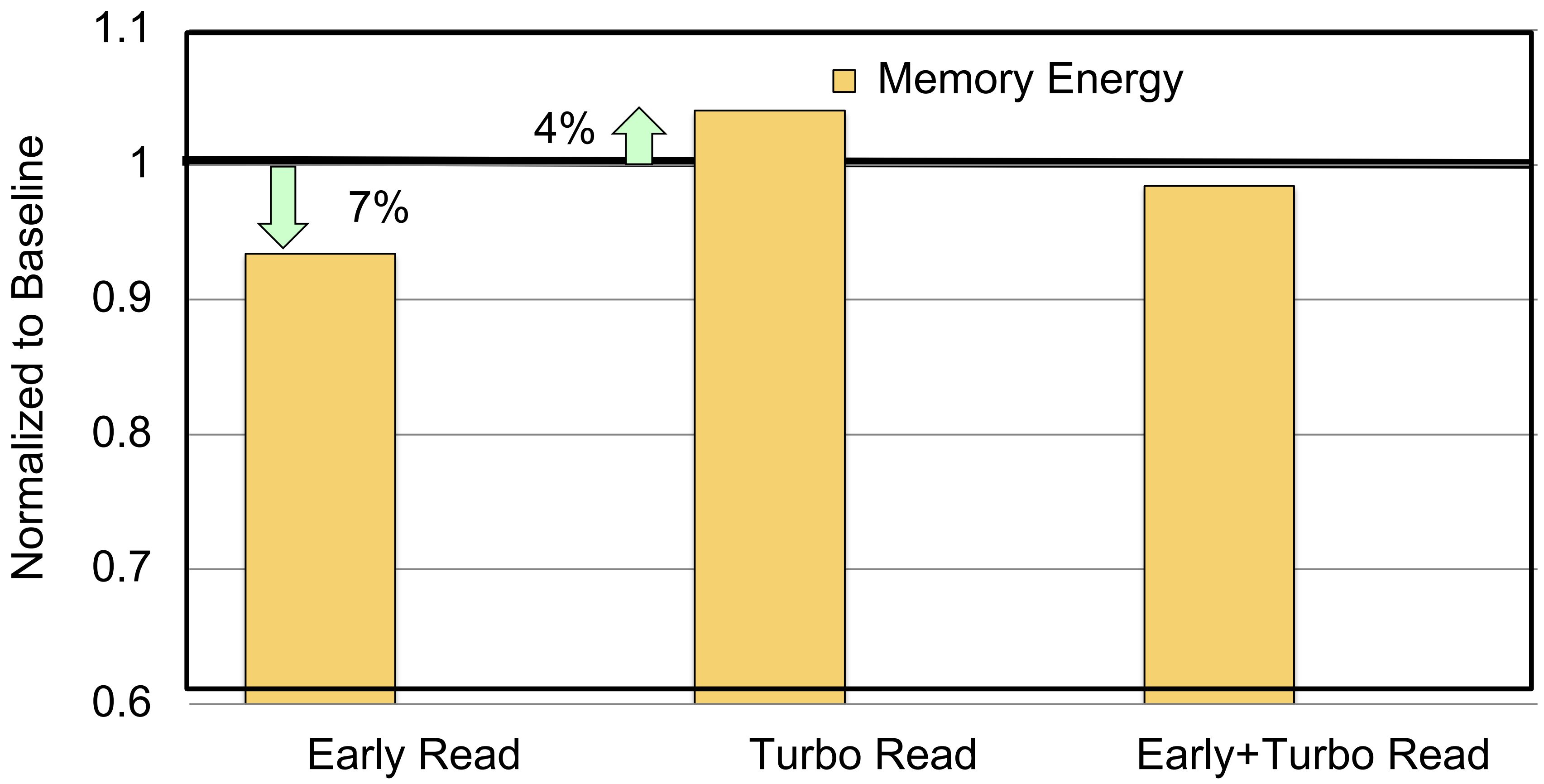

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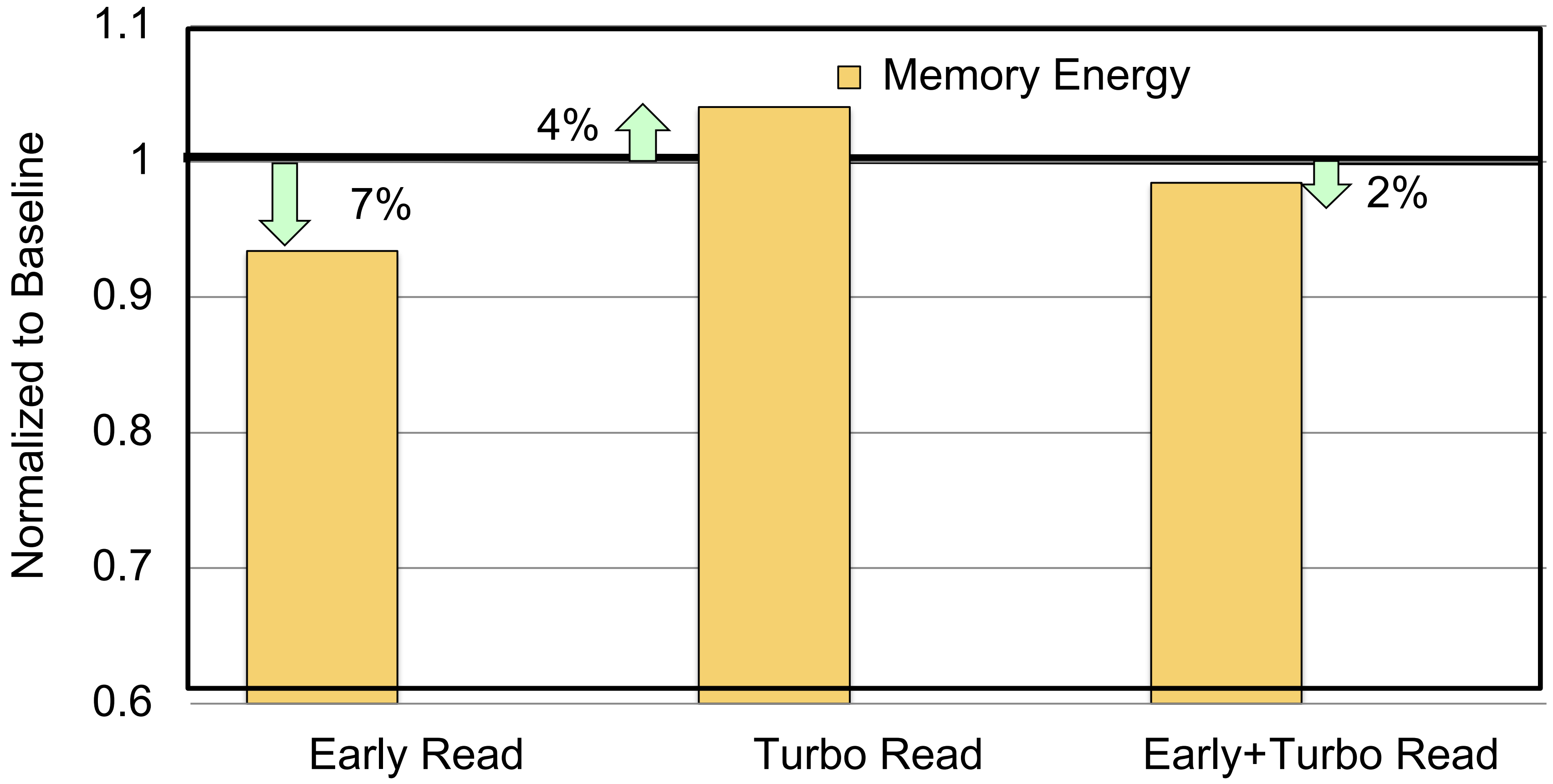

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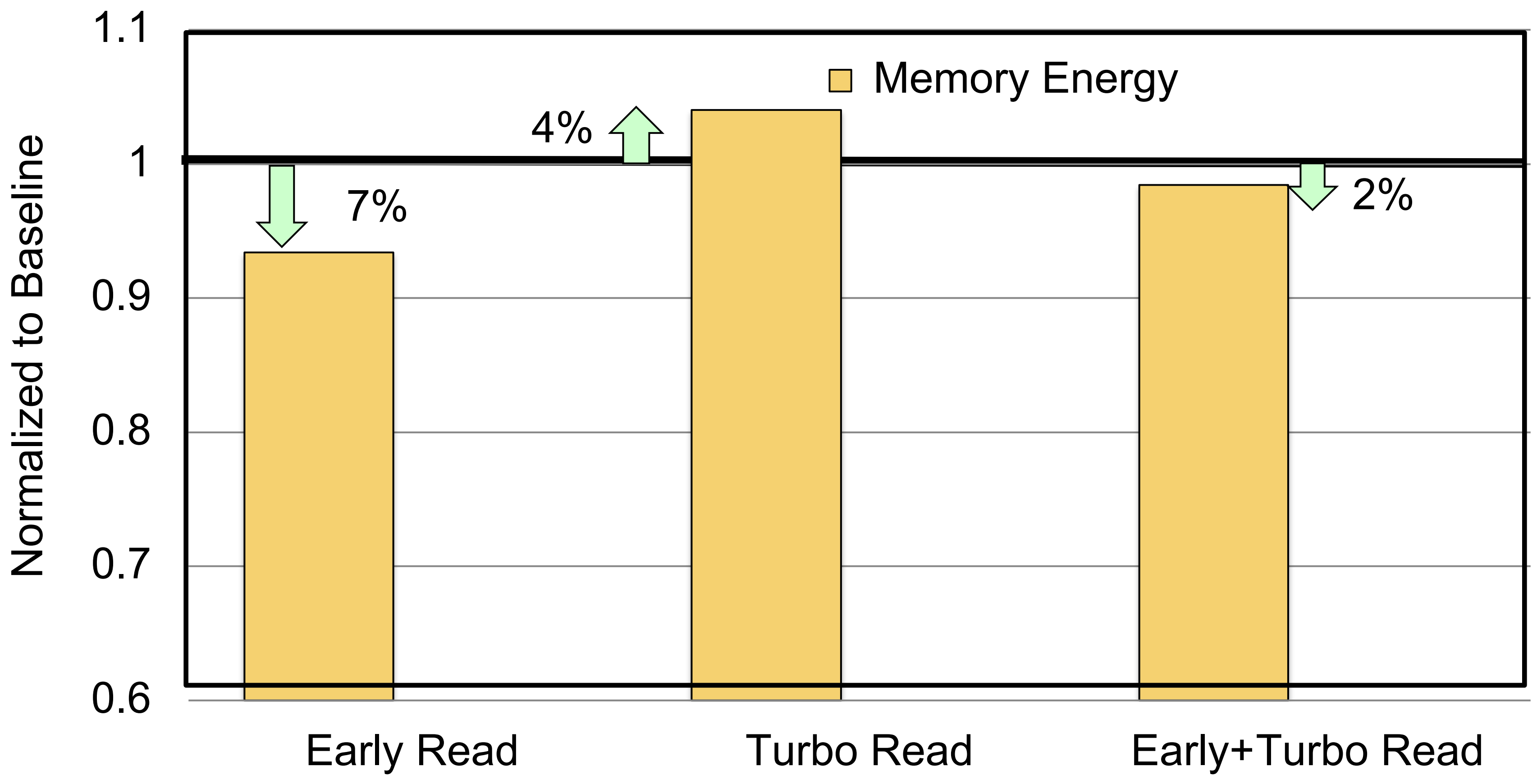

Our proposals reduce energy by 7%

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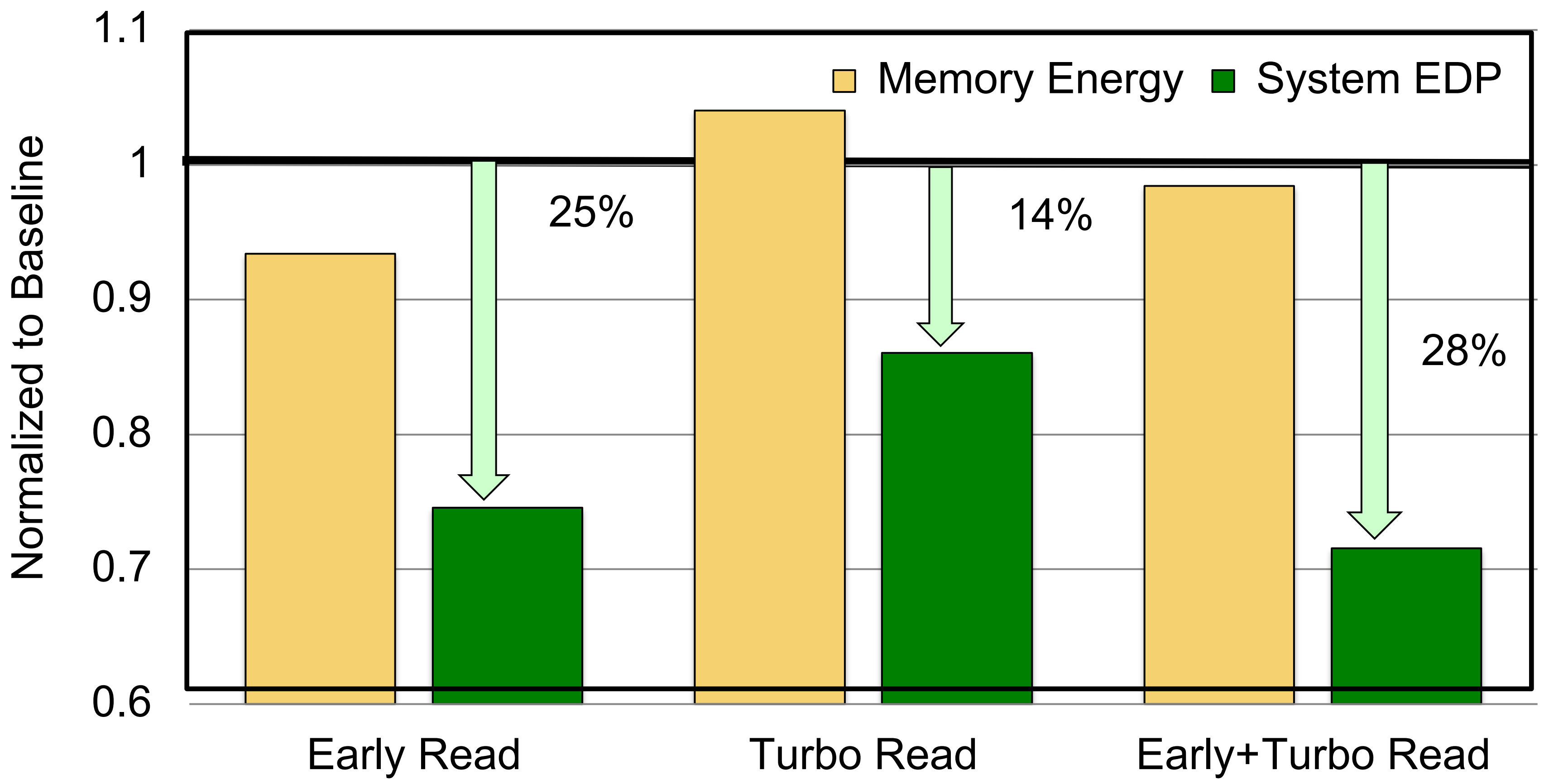

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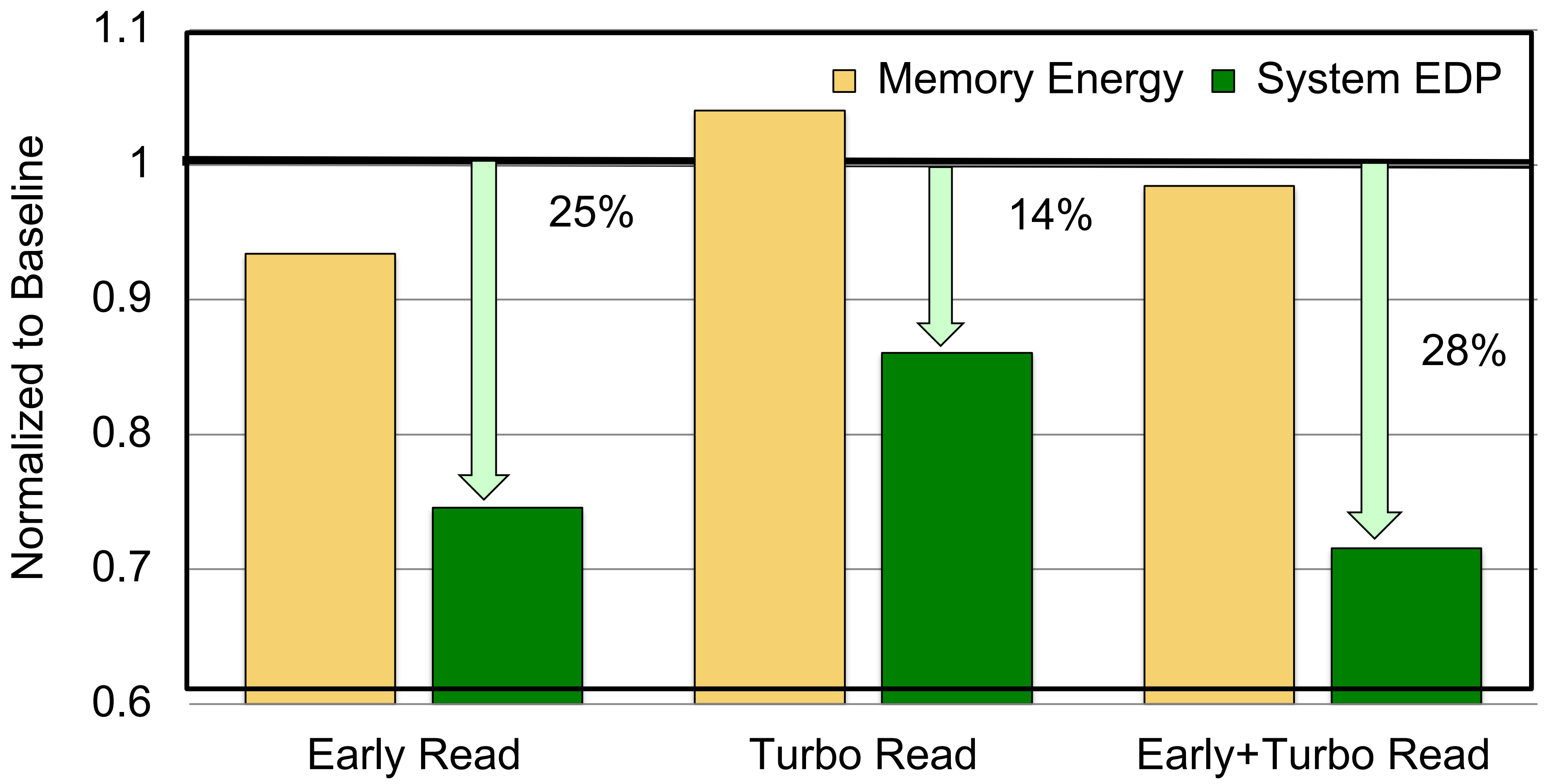

Our proposals reduce energy by 7%

Our proposals reduce EDP by 28%

OUTLINE

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- Two low cost solutions
- Early Read: Better-than-worst-case sensing using Berger Codes to detect errors and retry
- Turbo Read: Read with higher current and fix read disturb errors with ECC

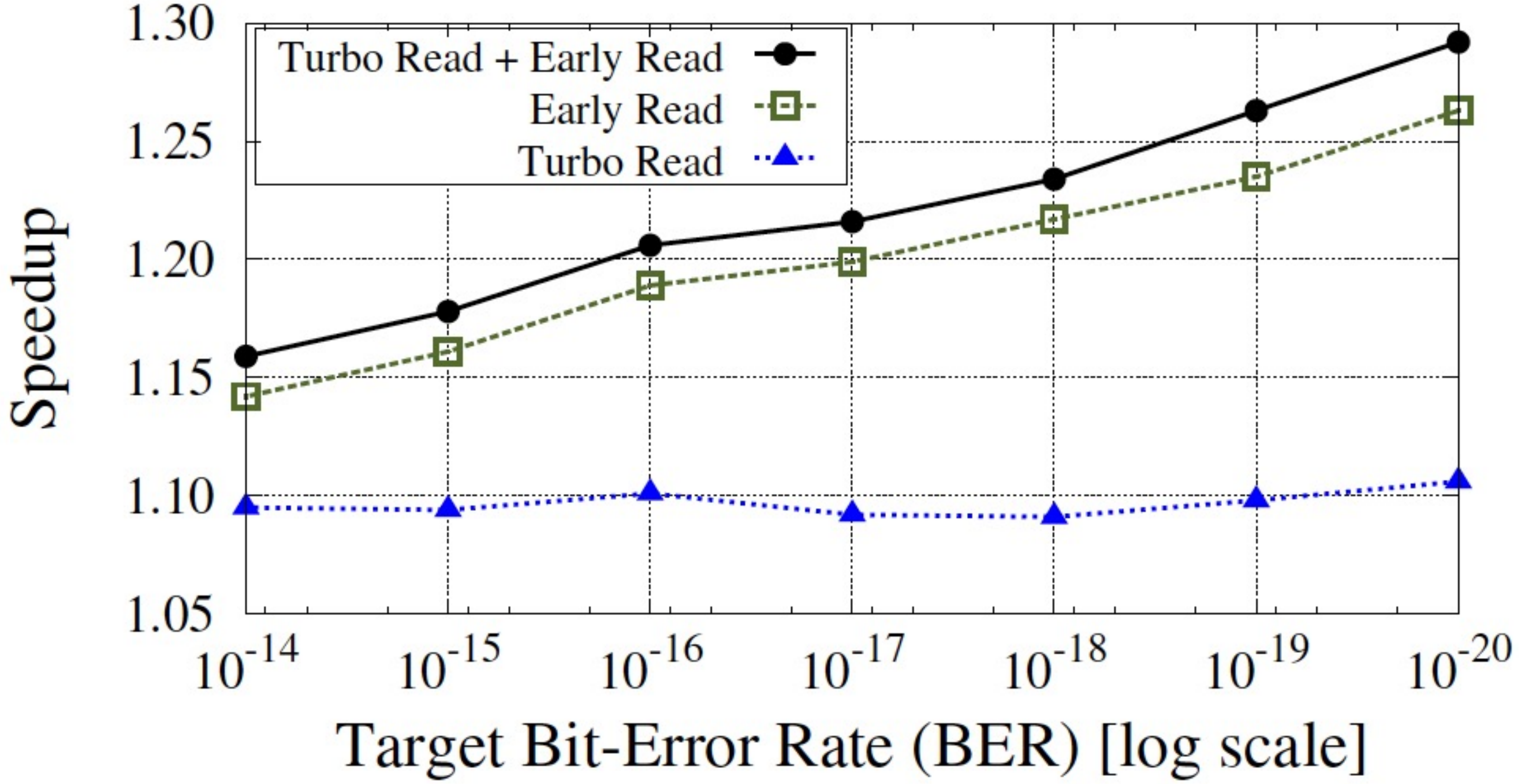
- Proposed solutions reduce read latency by 30% ➔ Performance improves by 21%, EDP by 28%

Thank You

BEWARE OF THE WORST-CASE SCENARIO
You could do so much more by thinking of "Better-Than-the-Worst-Case"!

BACKUP

SENSITIVITY TO TARGET ERROR RATES



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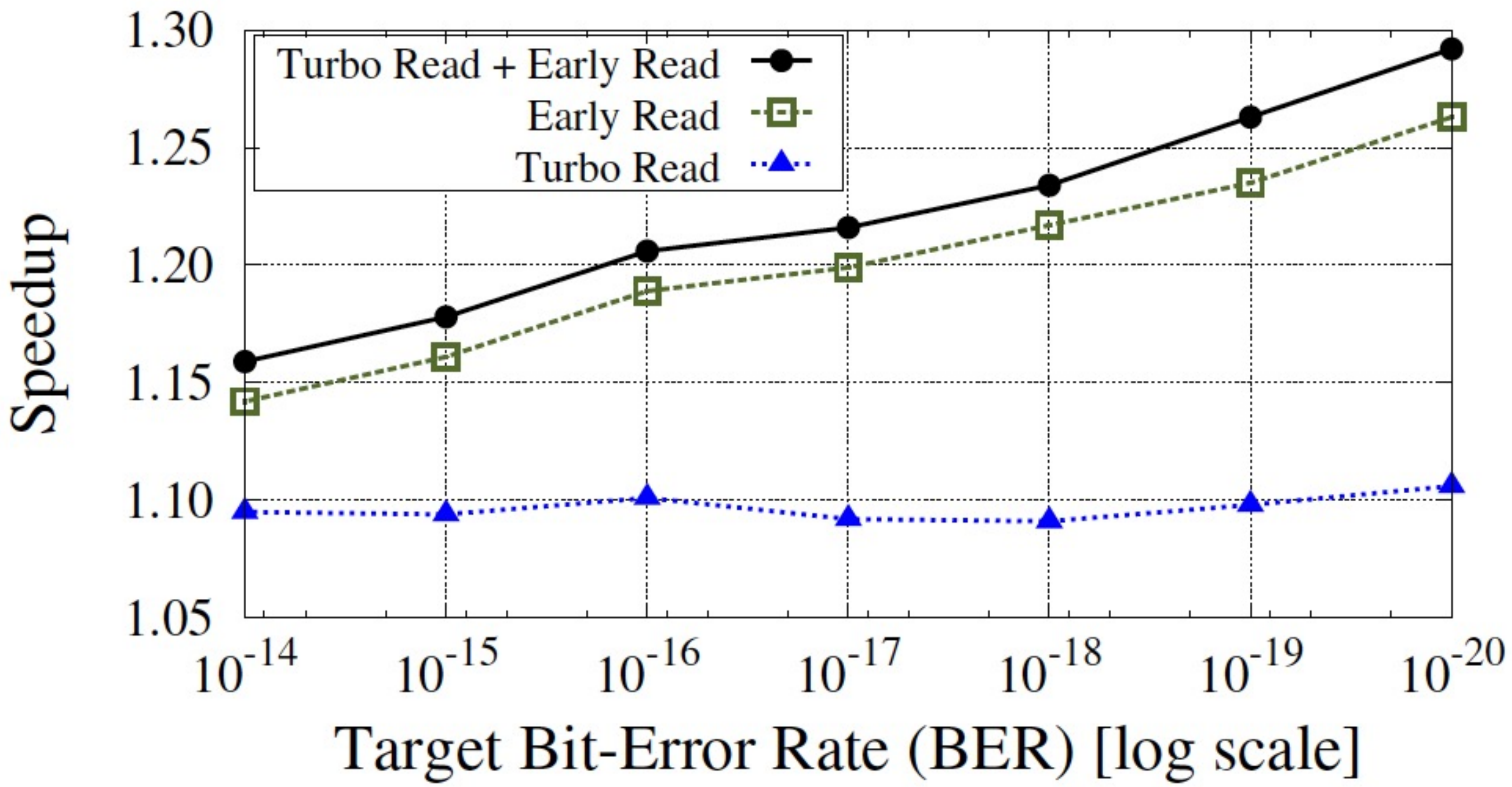
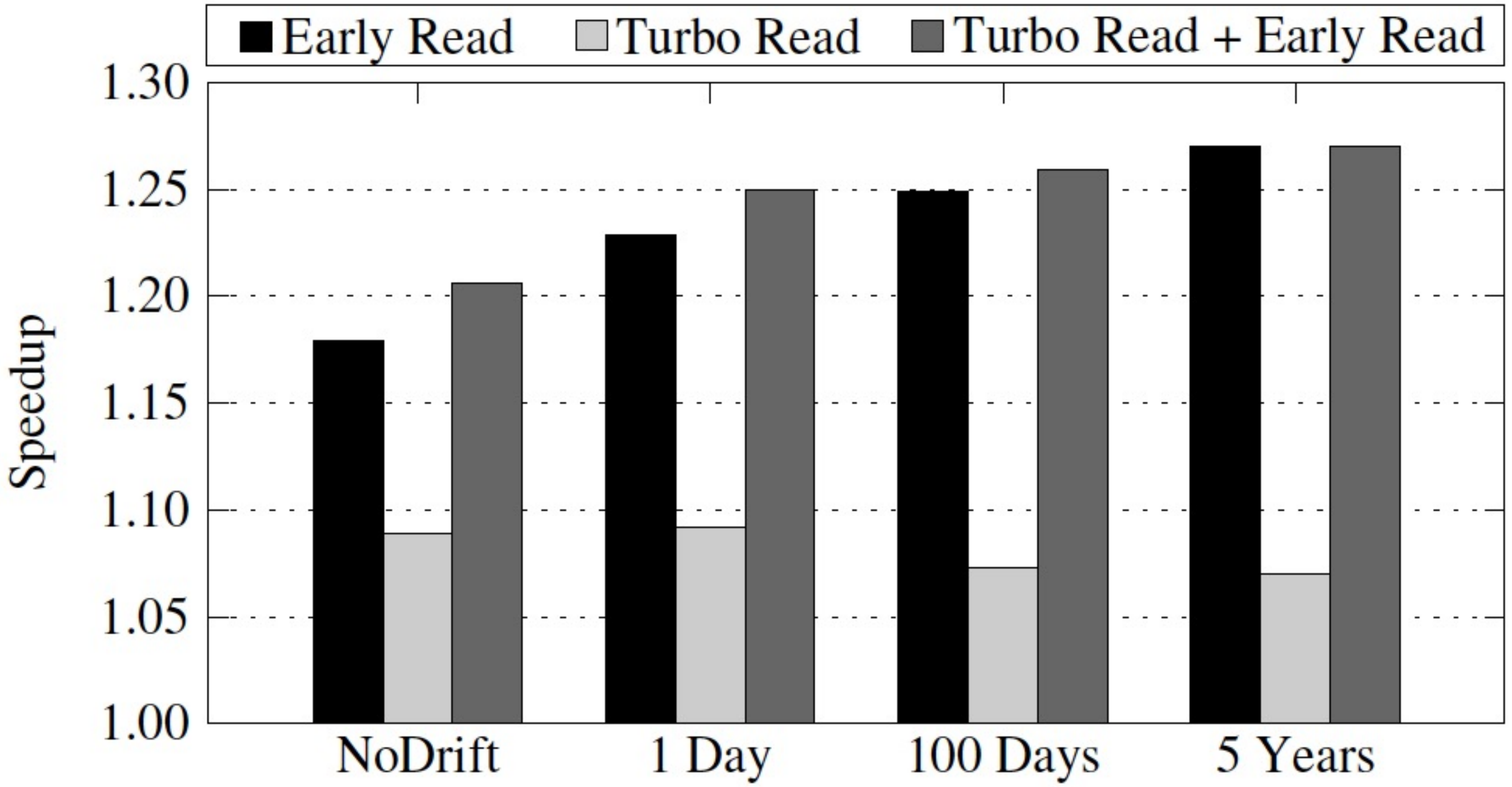


Our proposals become even more effective at higher target design error rates

SENSITIVITY TO DRIFT



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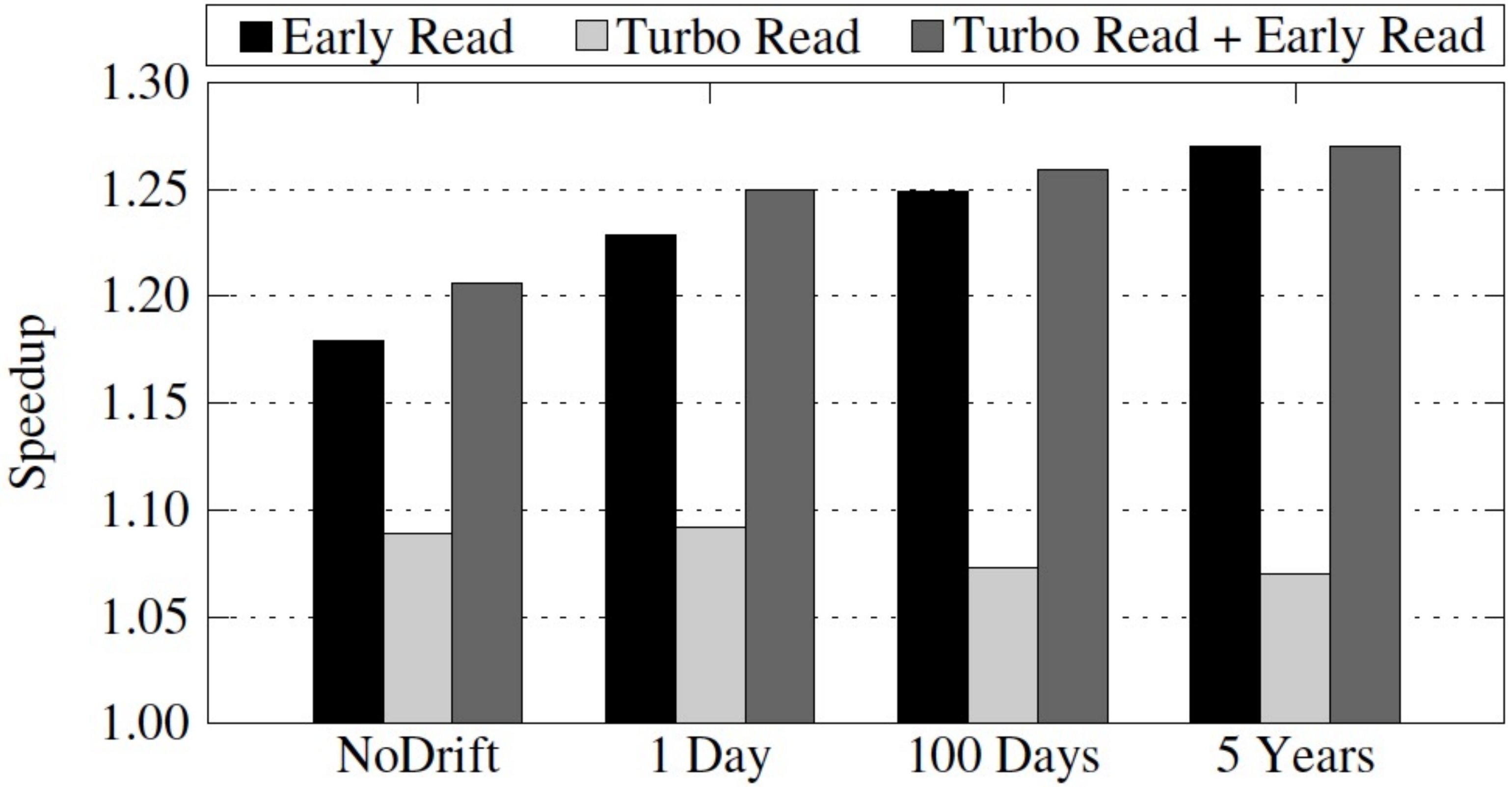
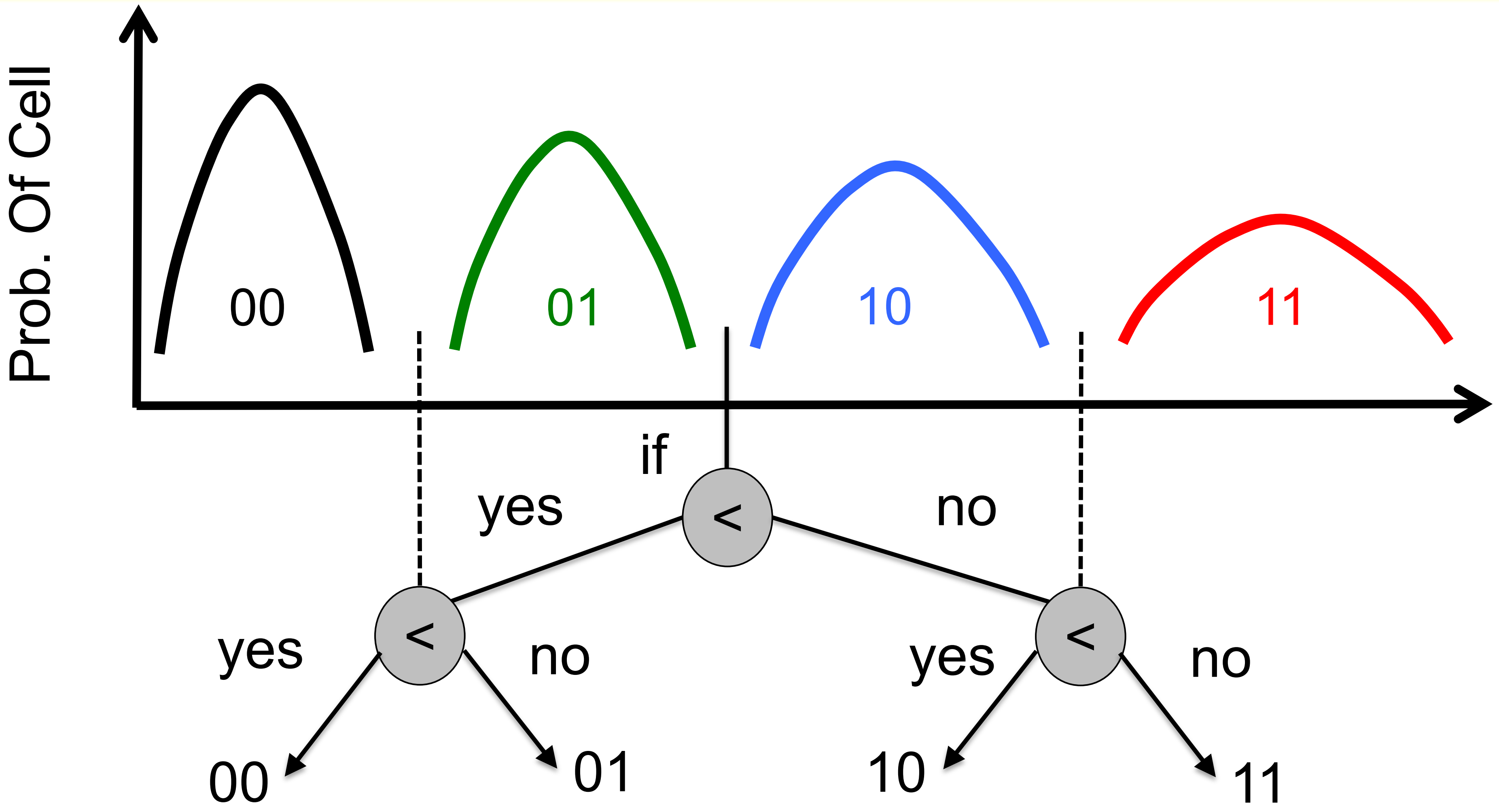


Our proposals become even more effective when drift margins are taken into account

MLC PCM LATENCY



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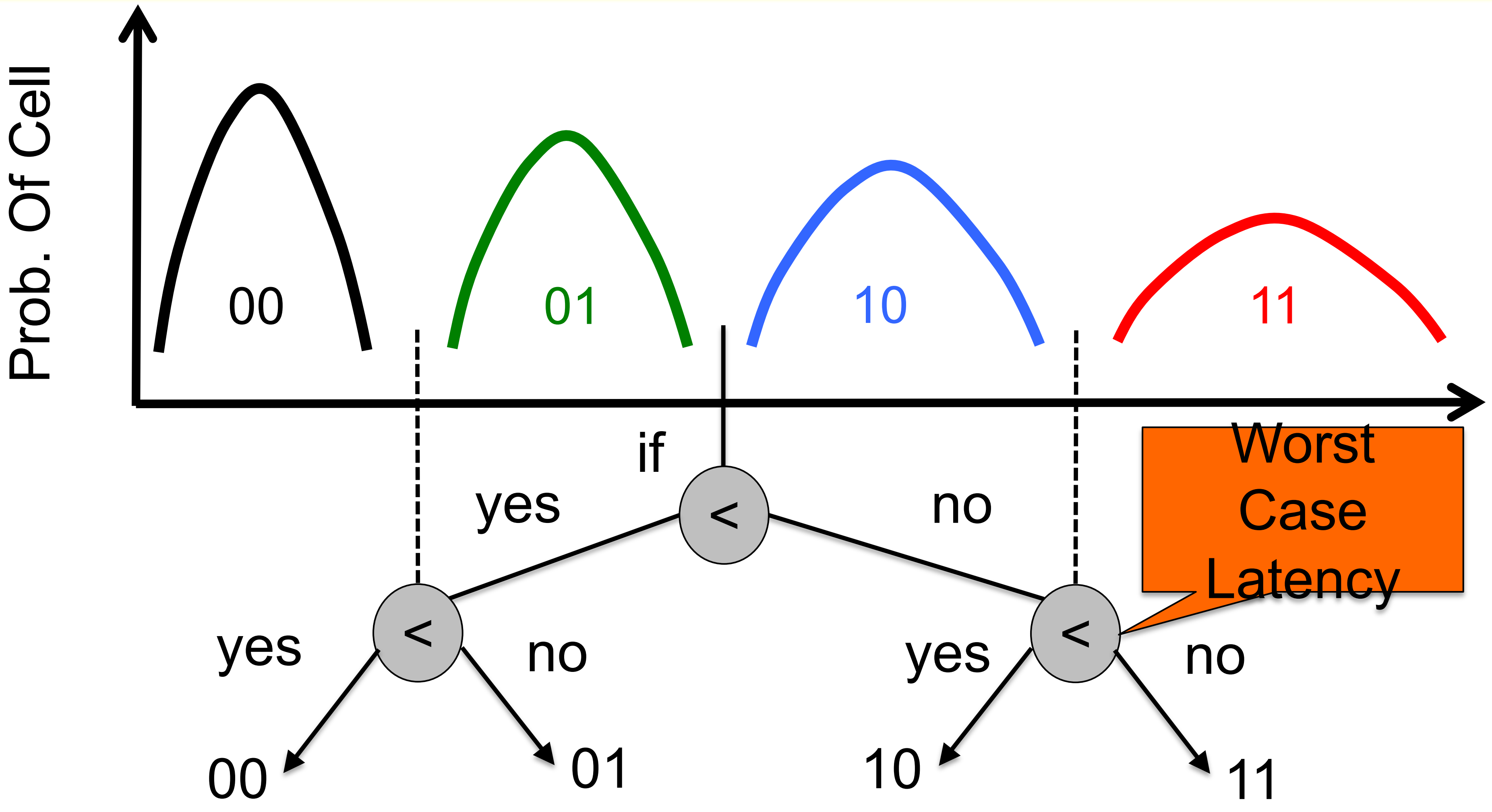

Latency determined by highest resistance states

LATENCY TREND WITH SCALING

- PCM stores values by varying resistance
- Higher resistance causes more read latency

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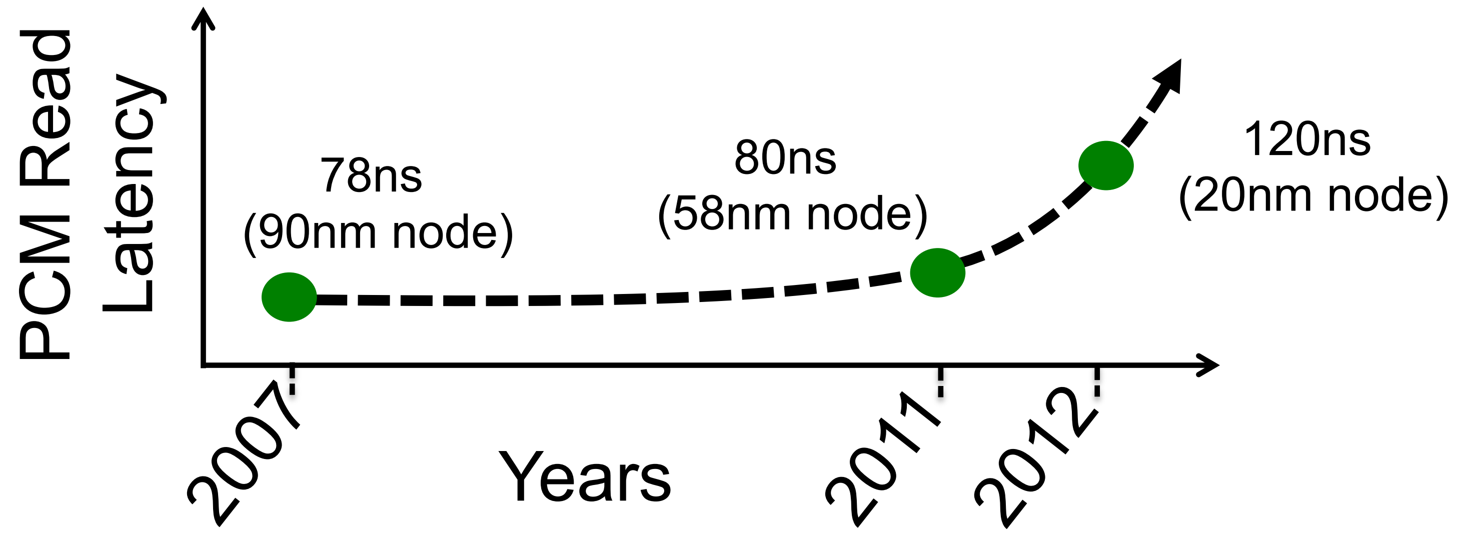

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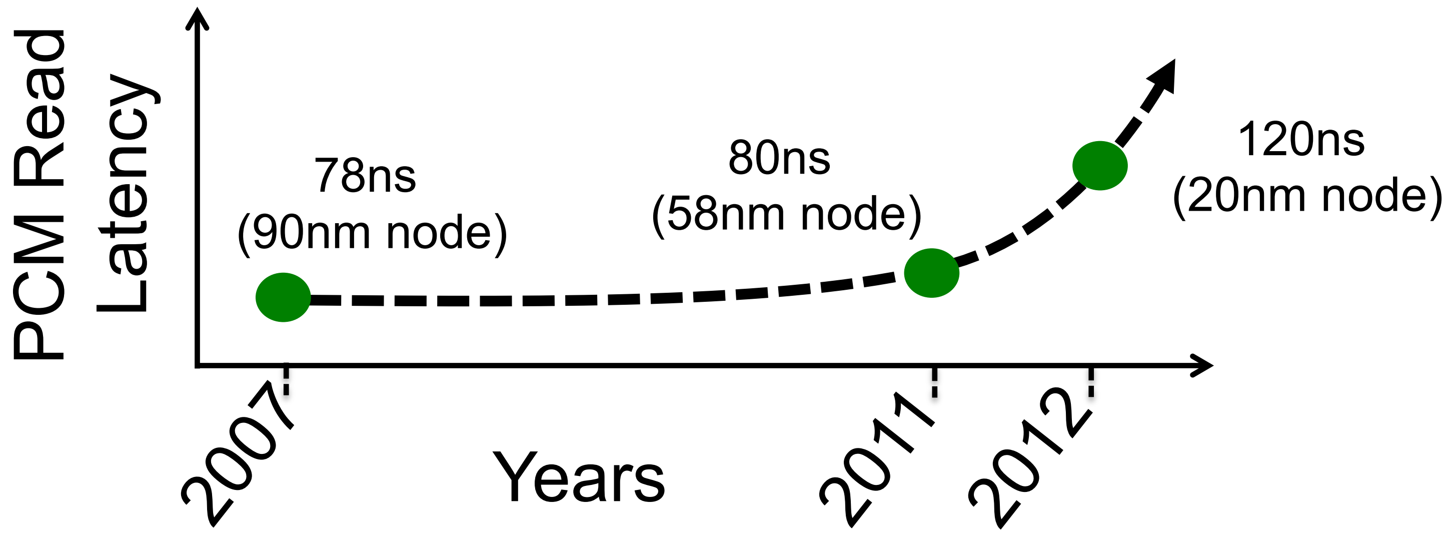

PCM read latency increases with scaling

REDUCING READ LATENCY MATTERS

- Read requests tend to halt execution
- Write requests can be buffered/paused/cancelled

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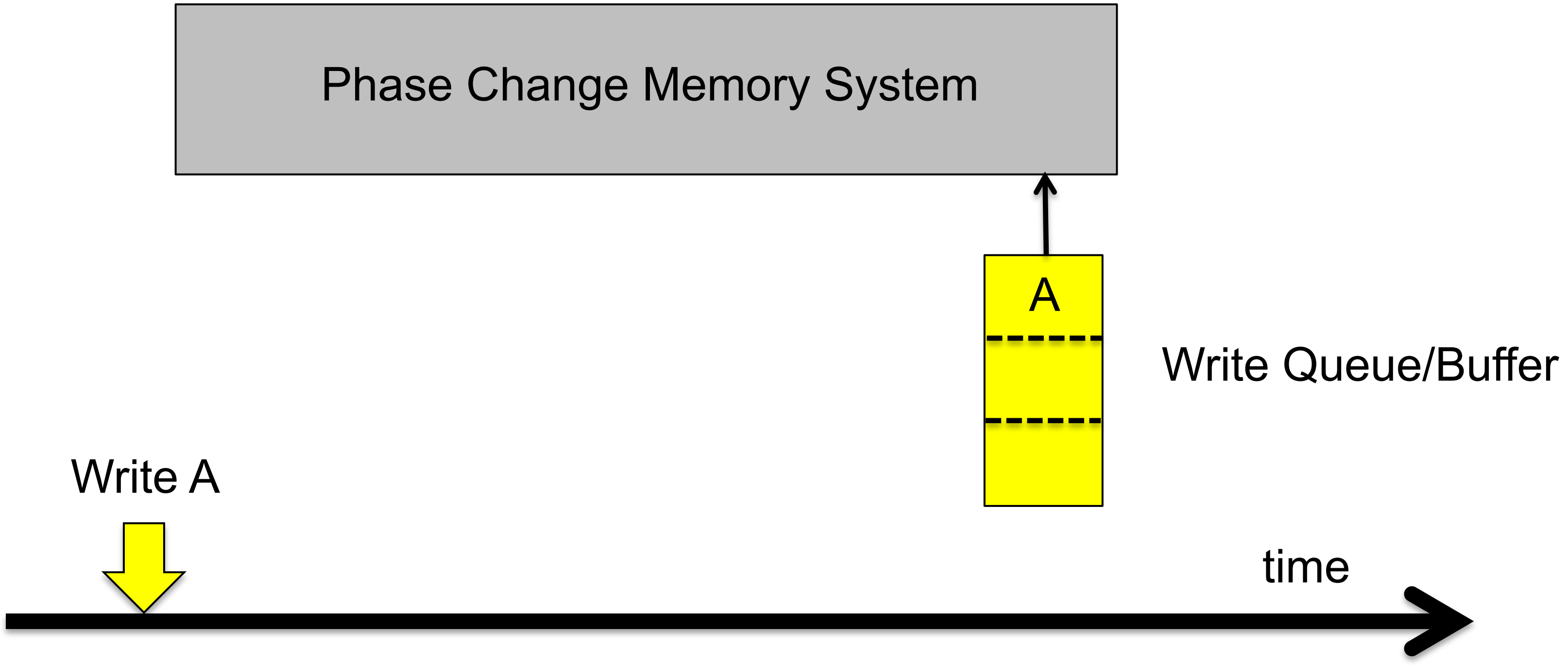

REDUCING READ LATENCY MATTERS

- Read requests tend to halt execution
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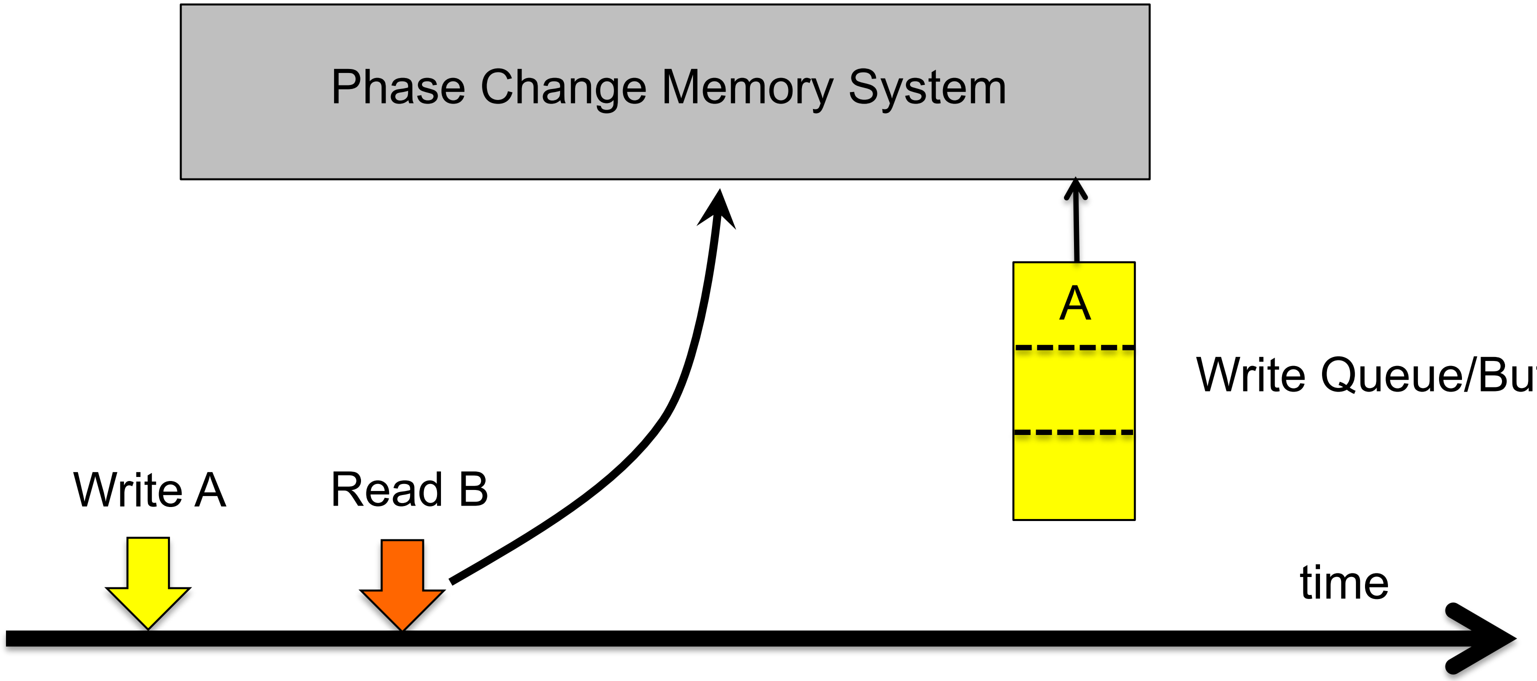

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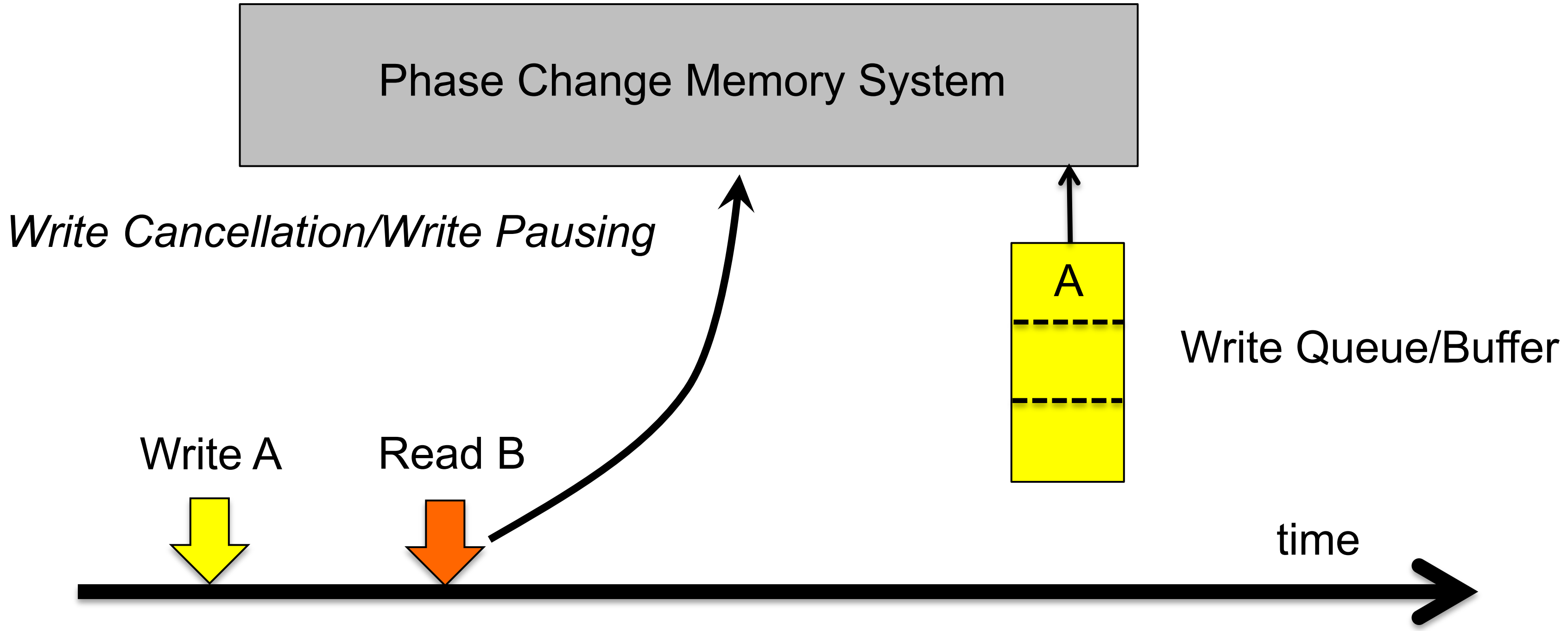
Phase Change Memory System
Write Cancellation/Write Pausing
A
Write Queue/Buffer
Write A
Read B
time

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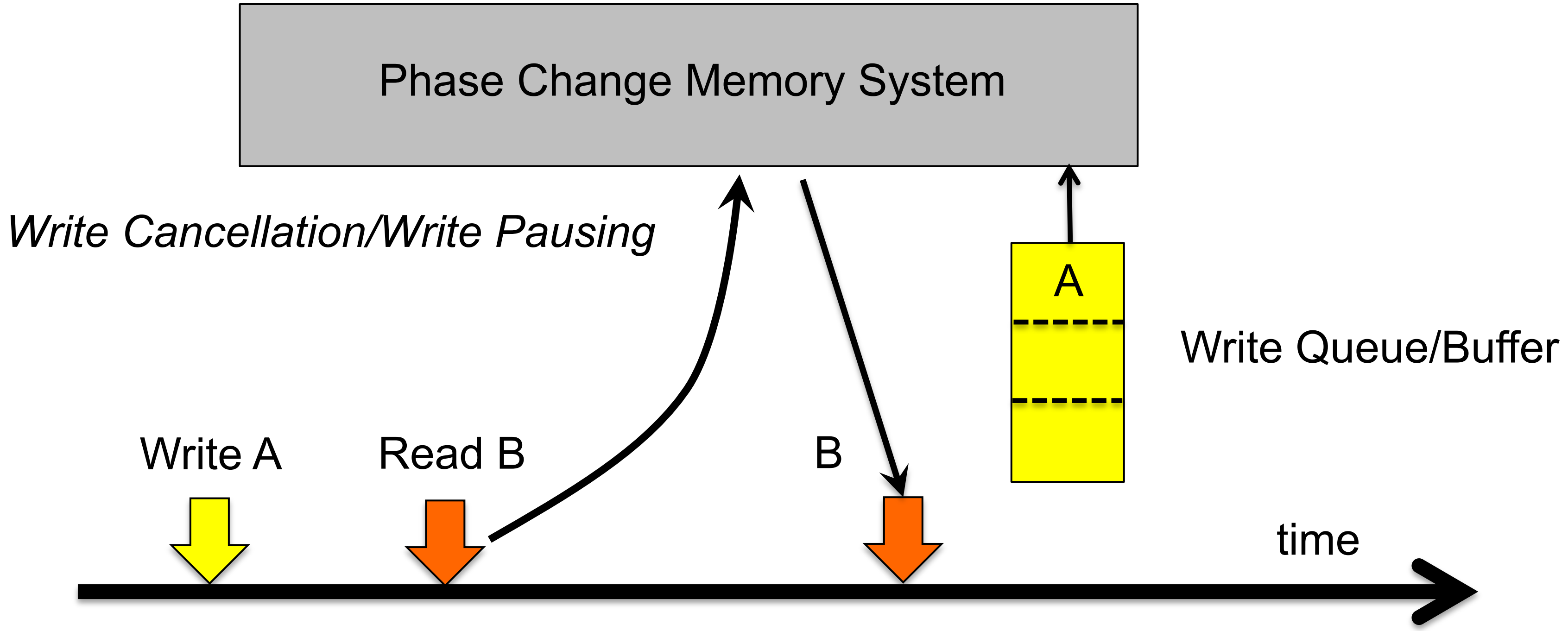

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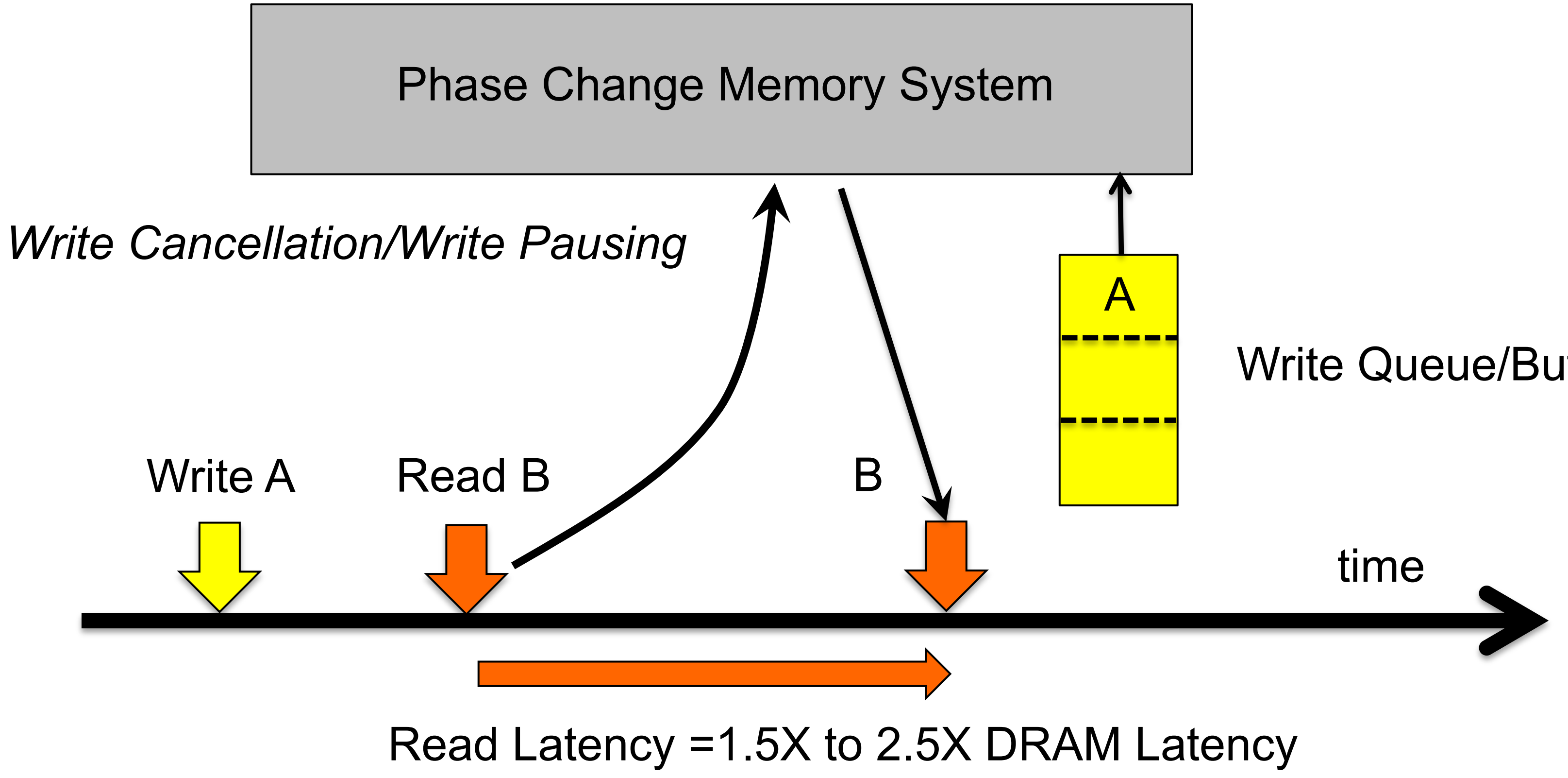
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B
time
Read Latency =1.5X to 2.5X DRAM Latency

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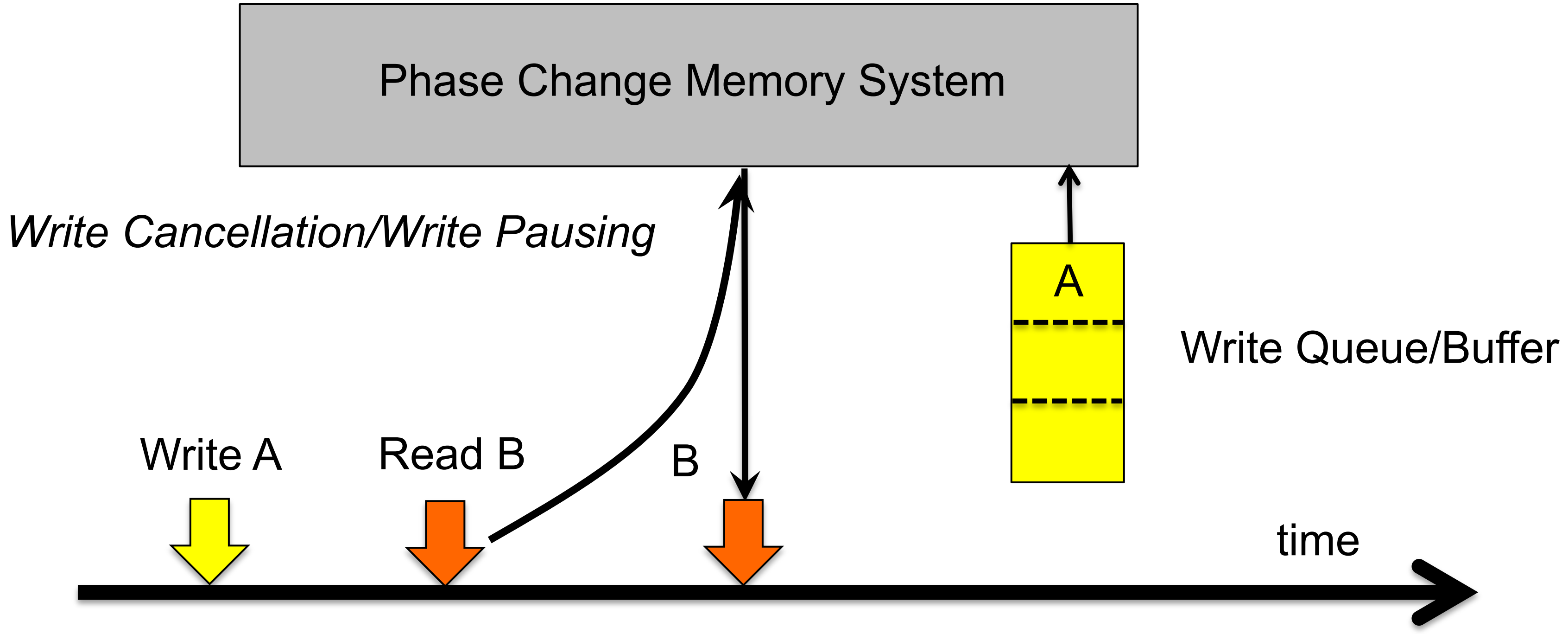

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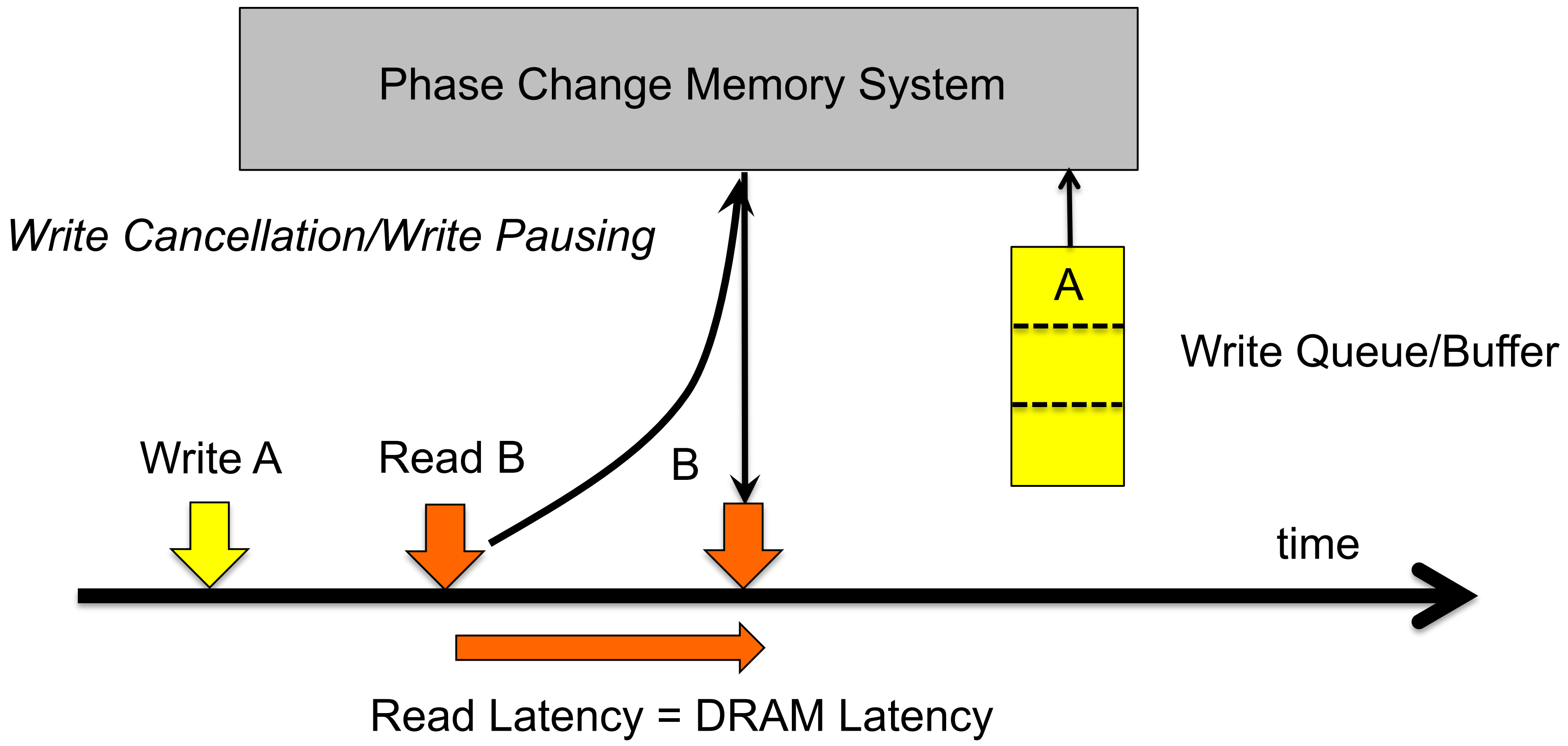
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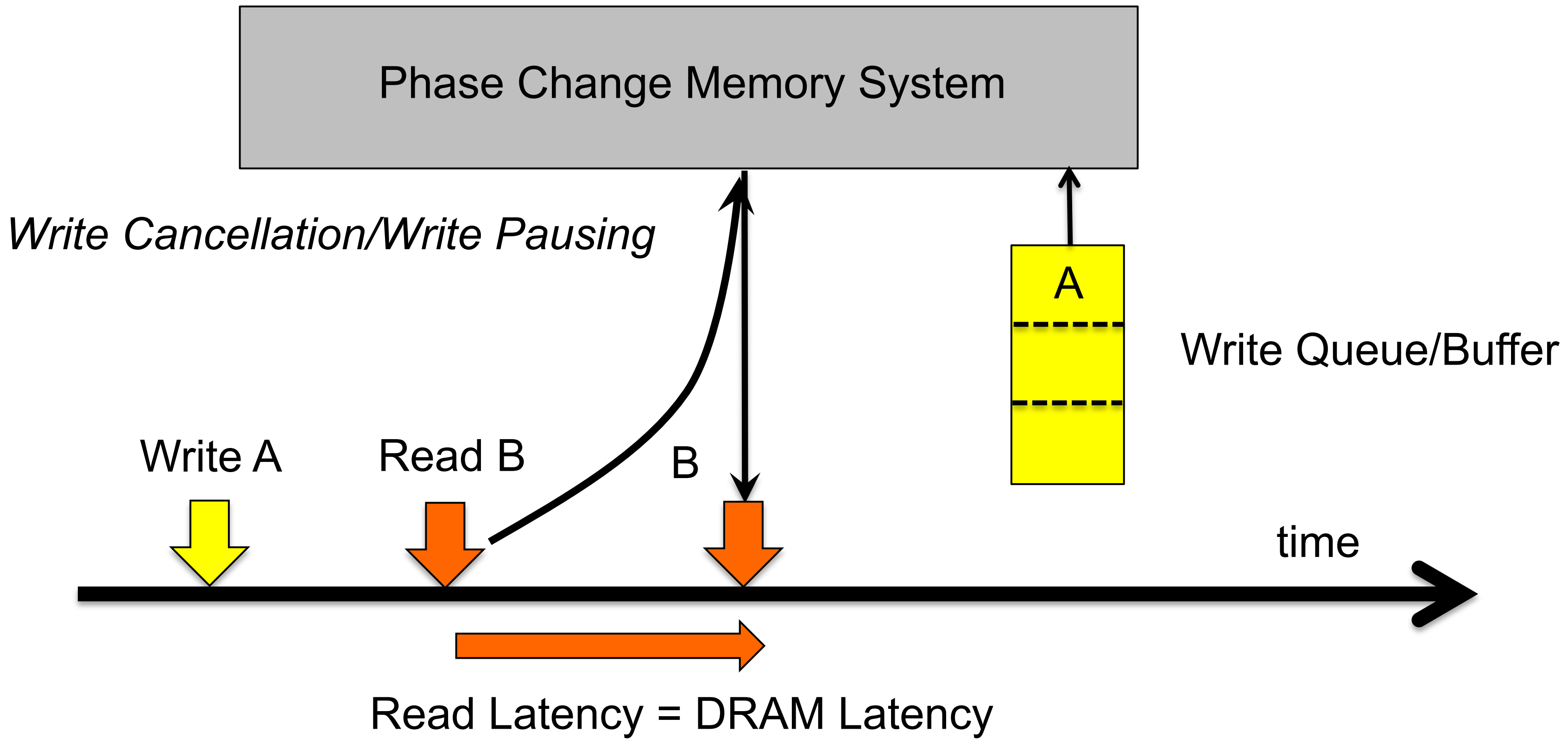
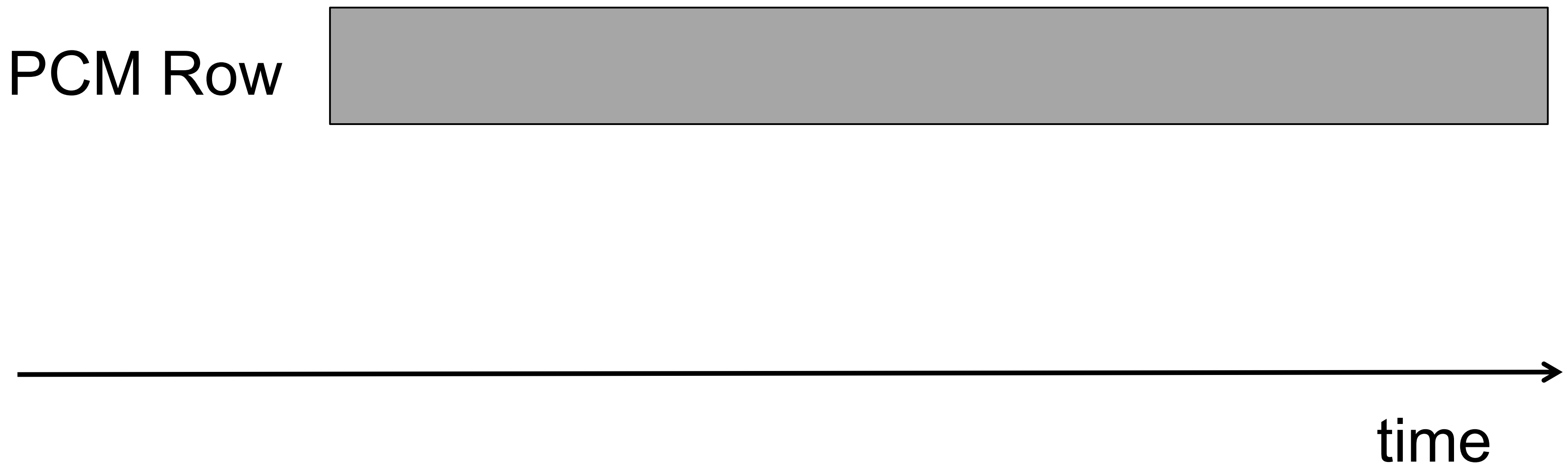


Phase Change Memory System
Write Cancellation/Write Pausing
A
Write Queue/Buffer
Write A
Read B
B
time
Read Latency = DRAM Latency

Low read latency improves performance directly

LATENT FAULTS FROM READ DISTURB

- Adversarial read sequences can cause latent faults



Need a low cost solution to mitigate latent faults

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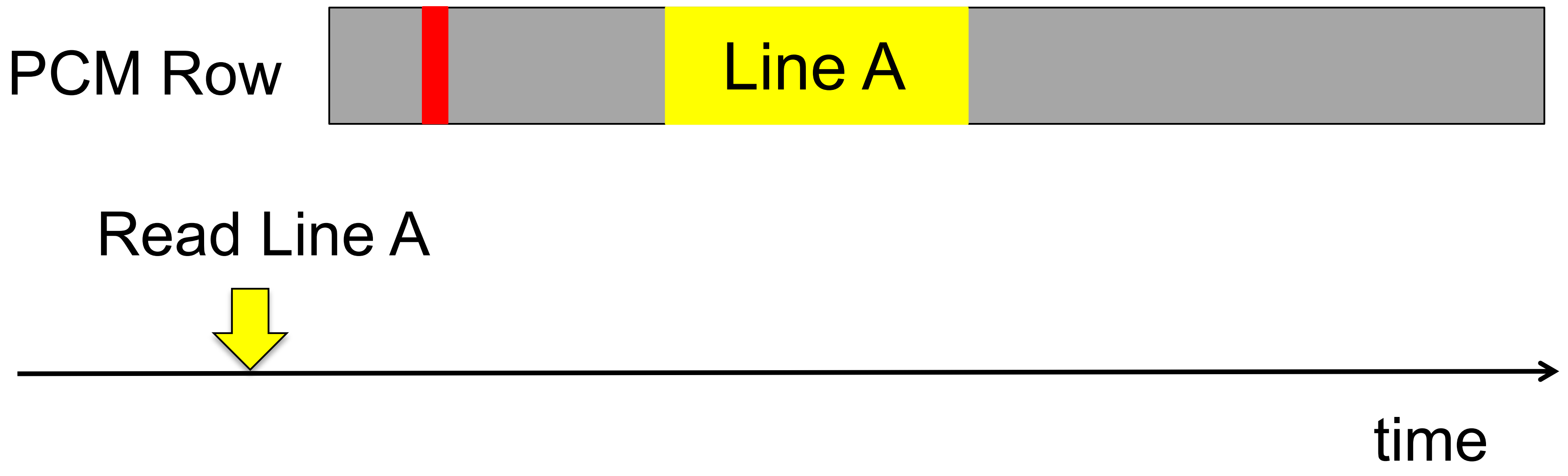

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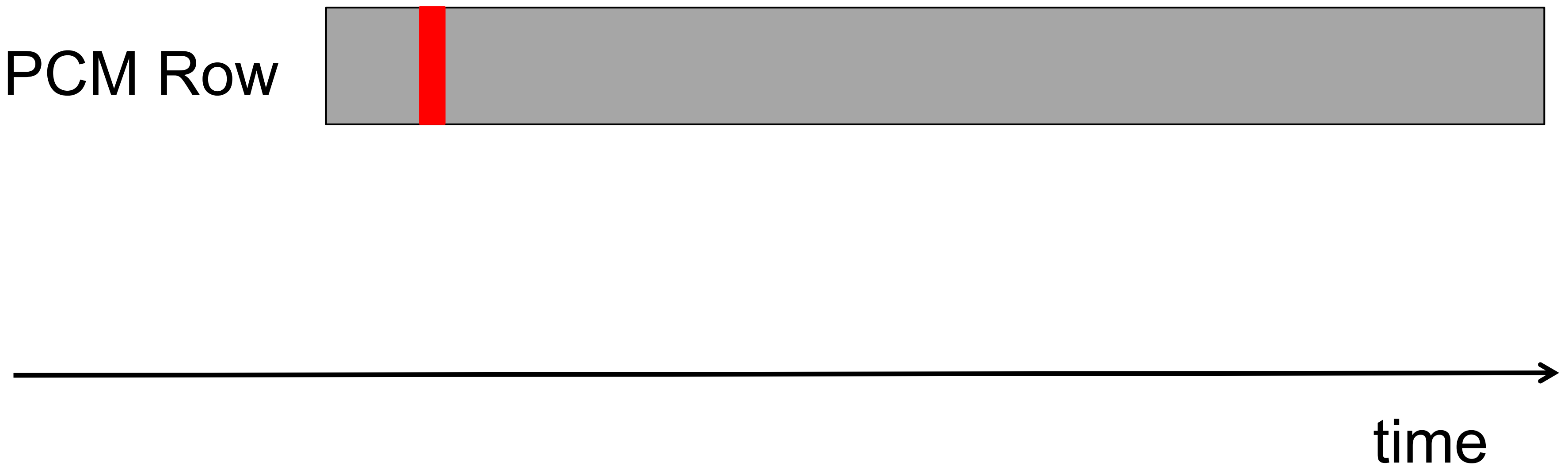

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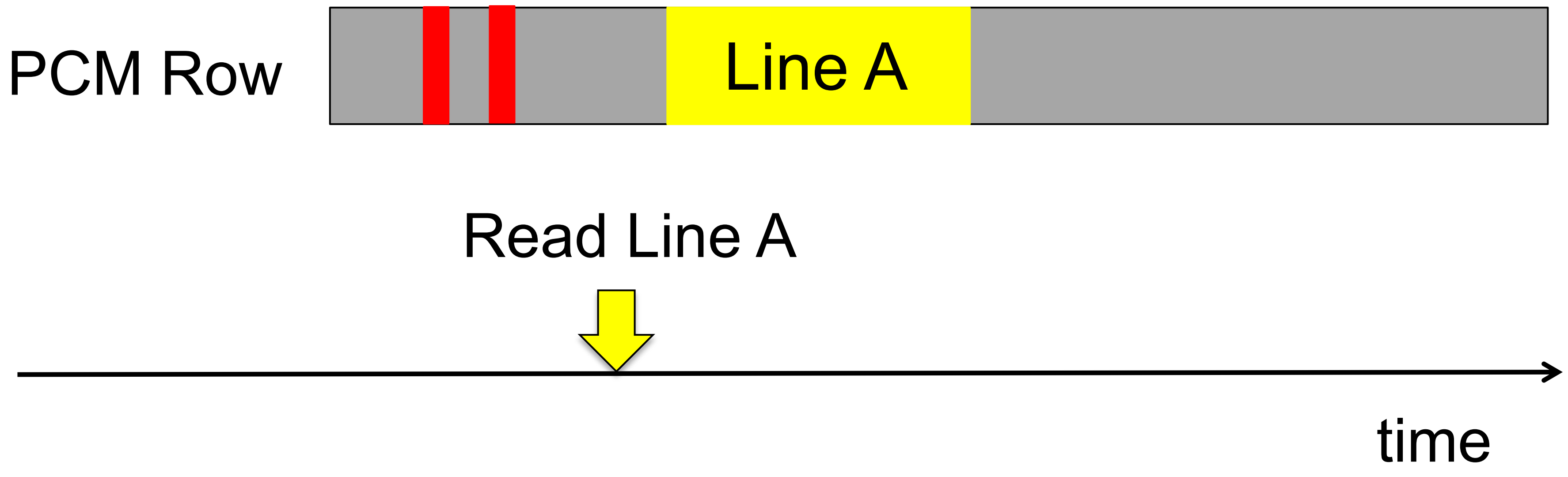

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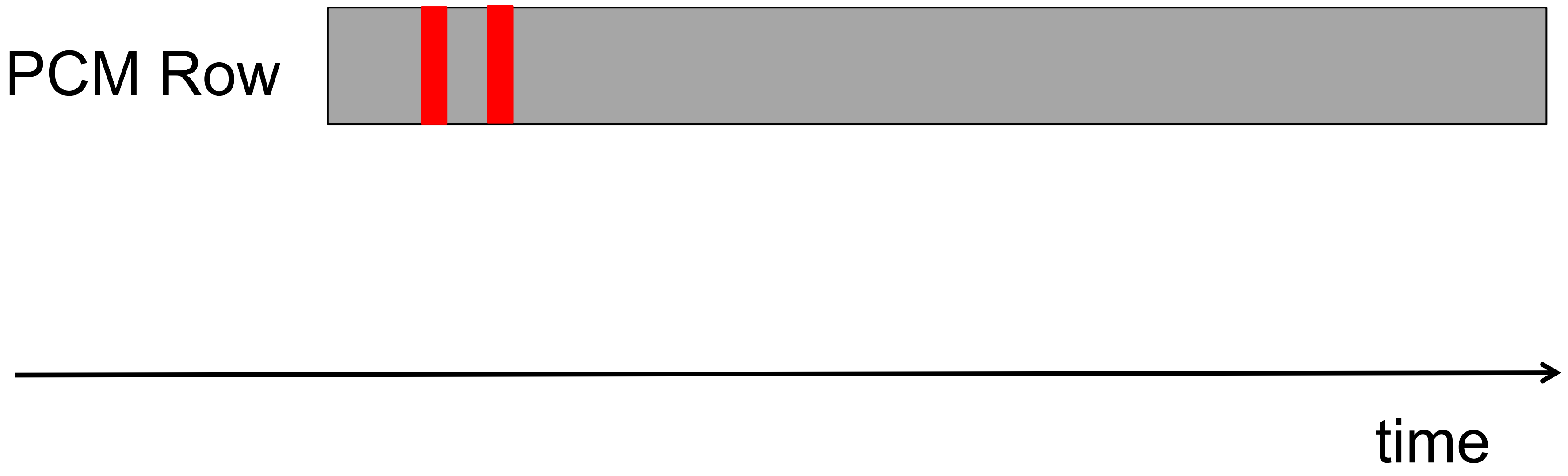

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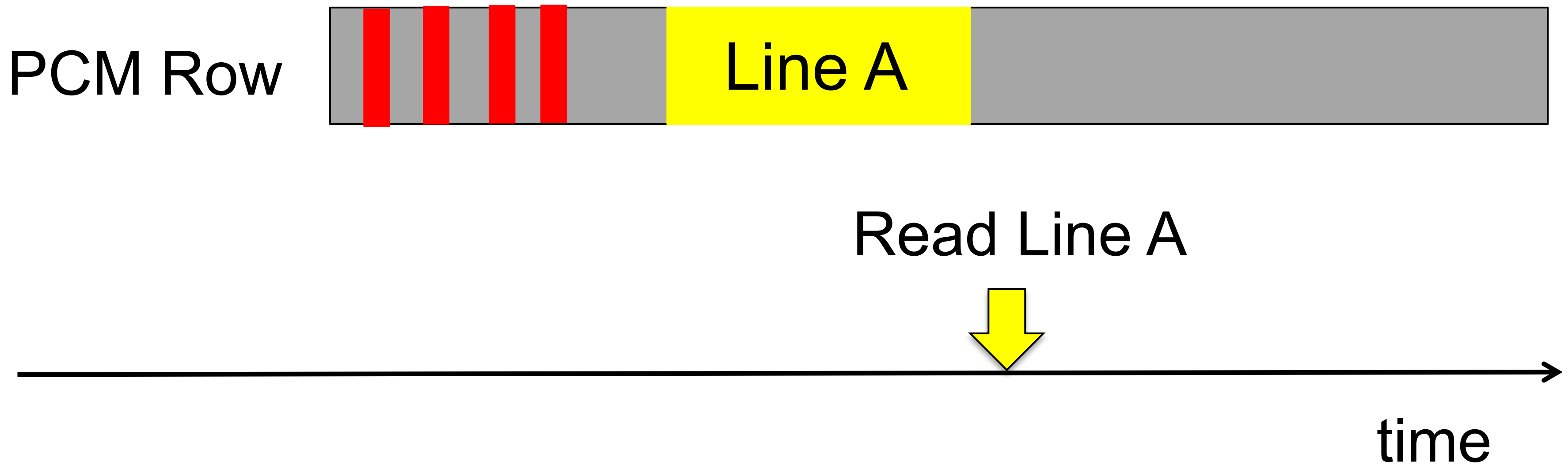

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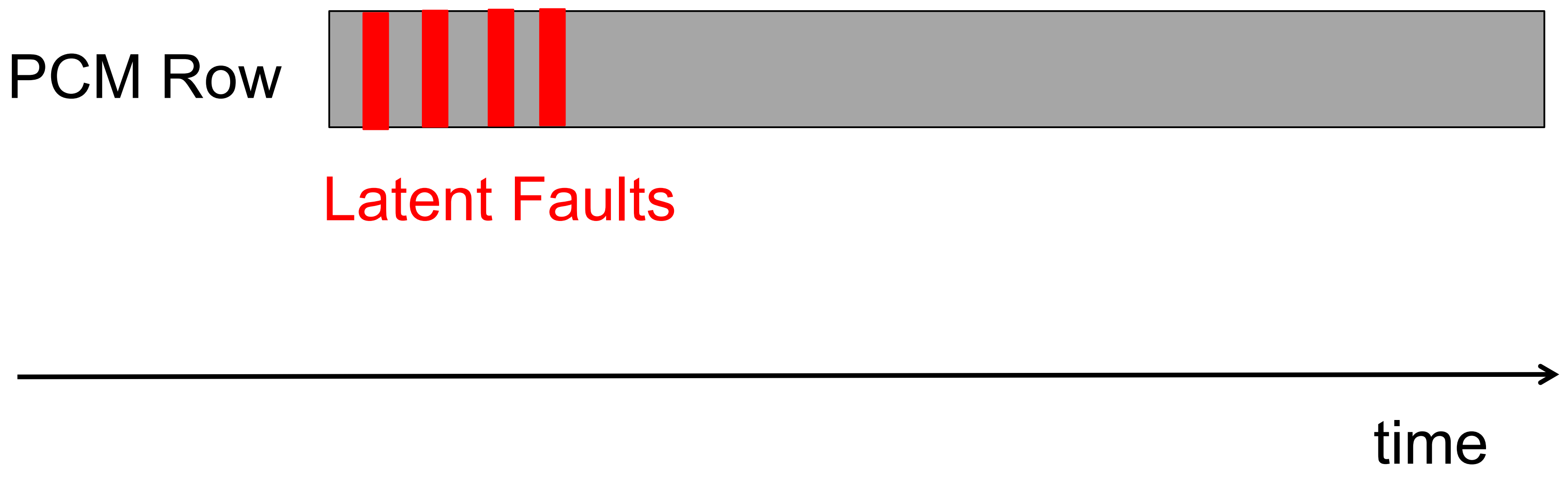

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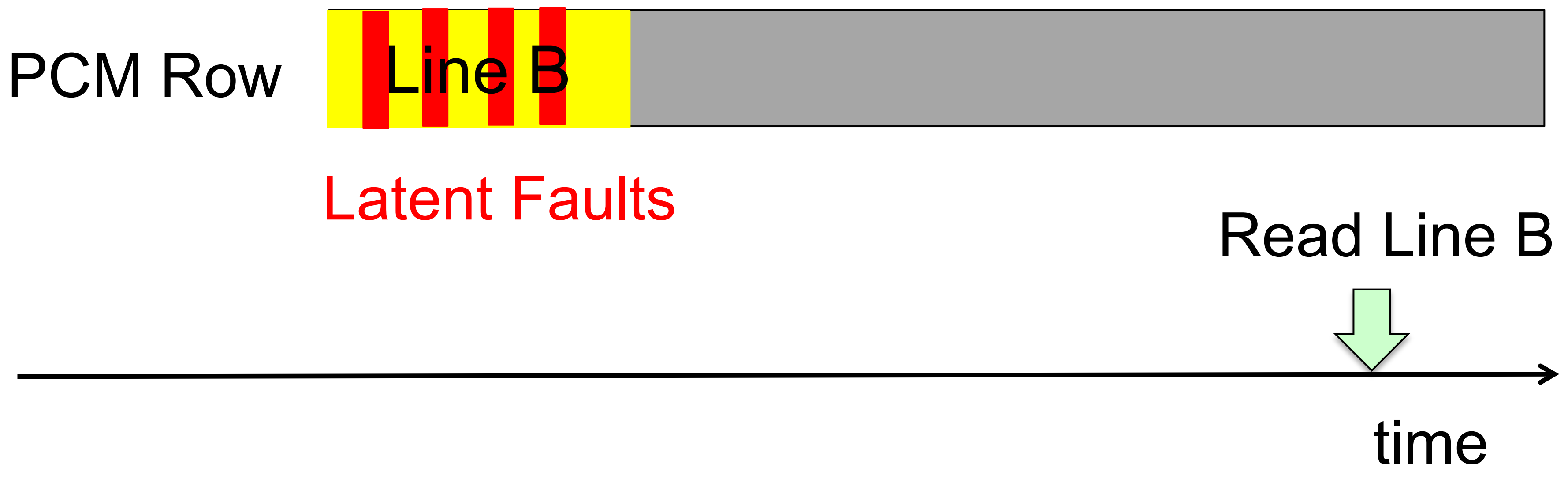

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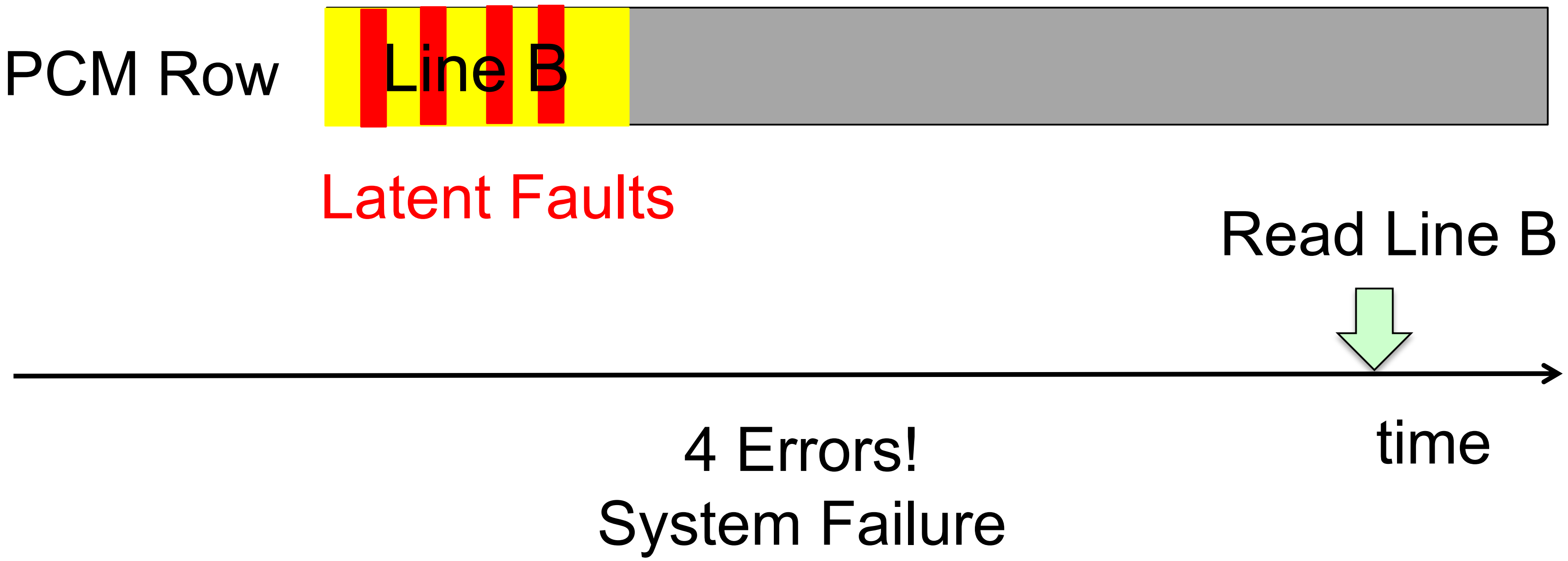
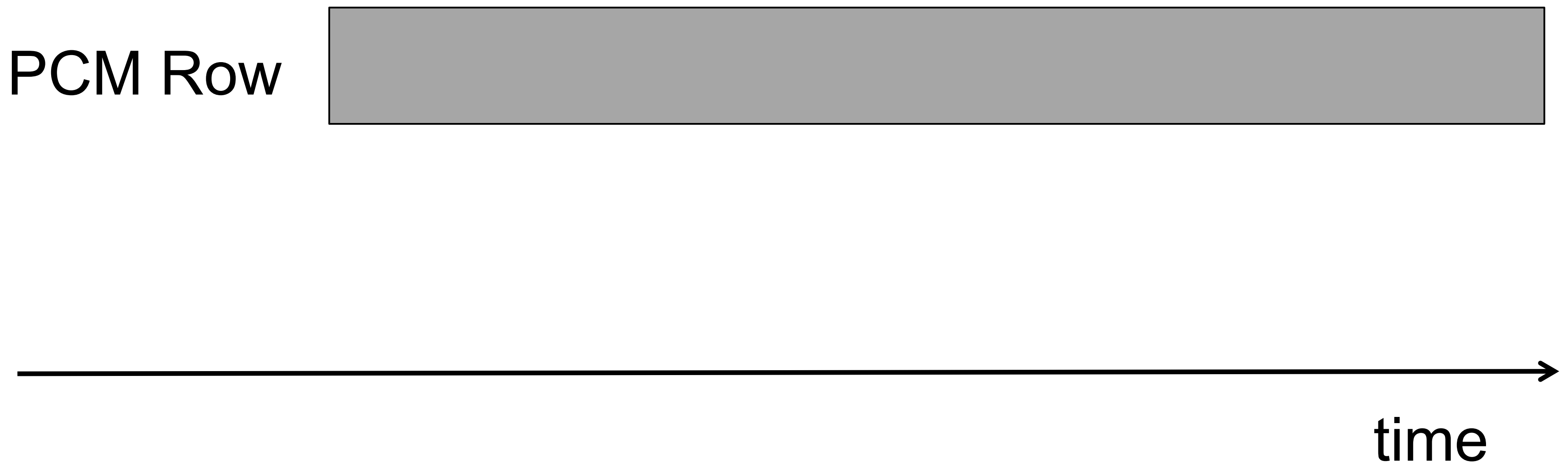


Need a low cost solution to mitigate latent faults

OUR SOLUTION: PROBABILISTIC SCRUB

- Scrub the entire row with low probability (say 1%)



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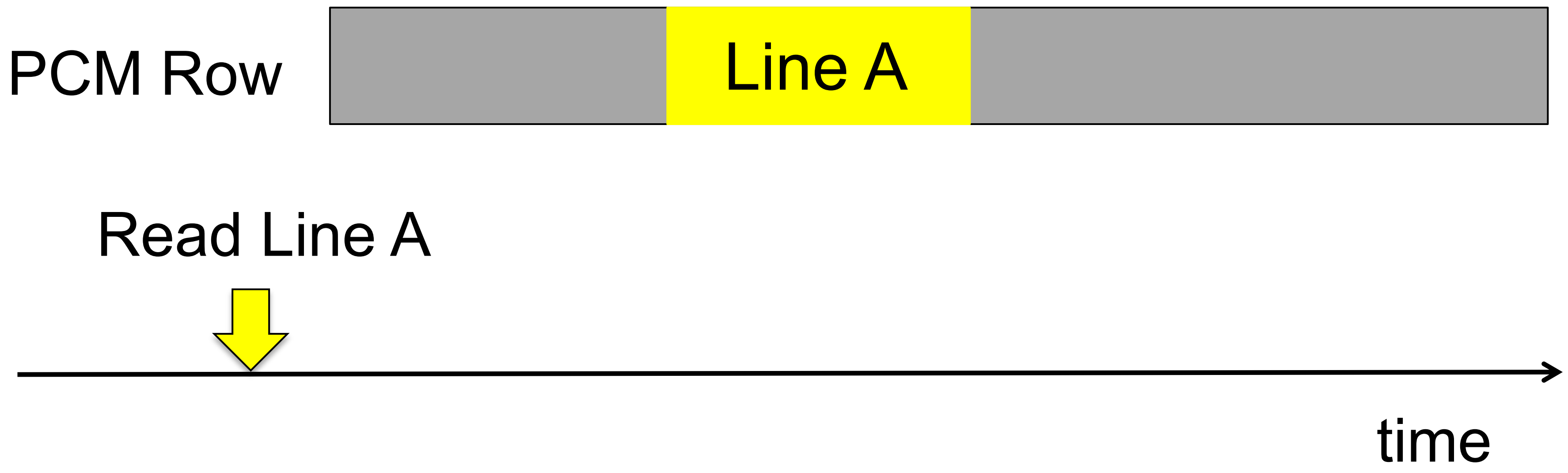

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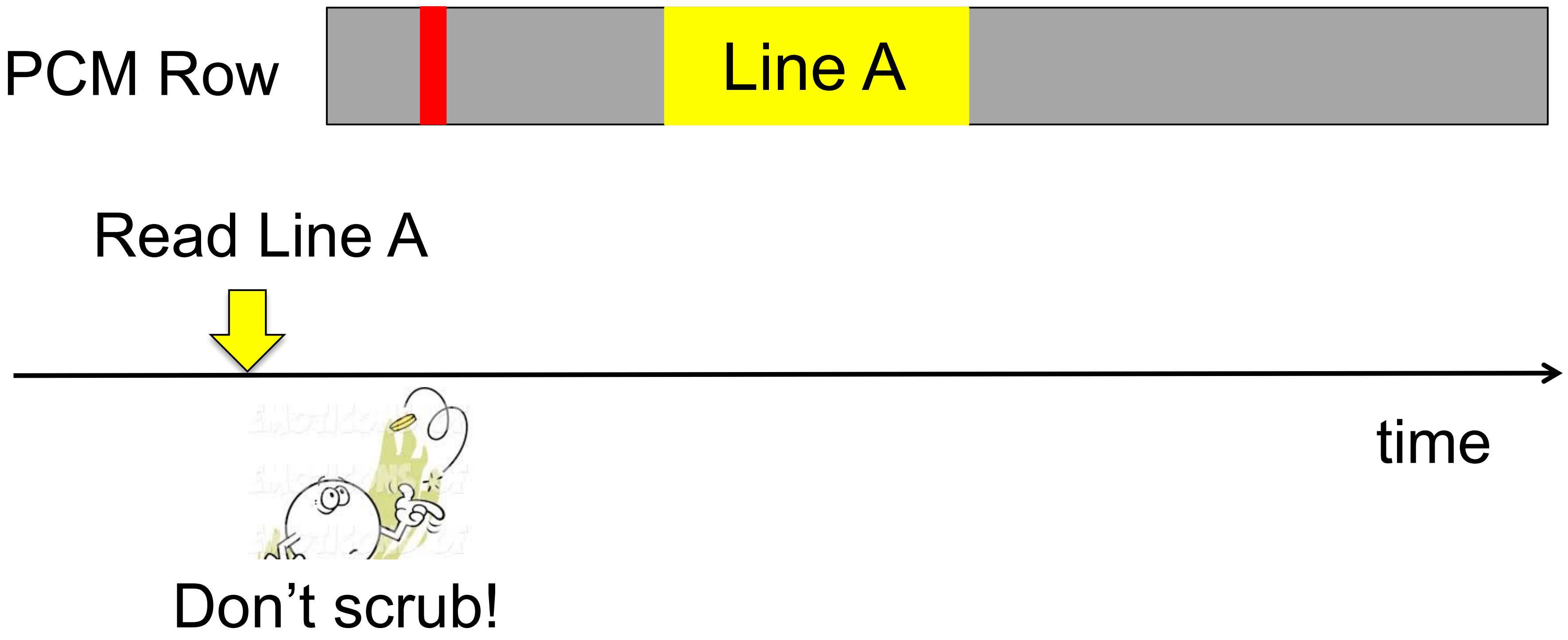

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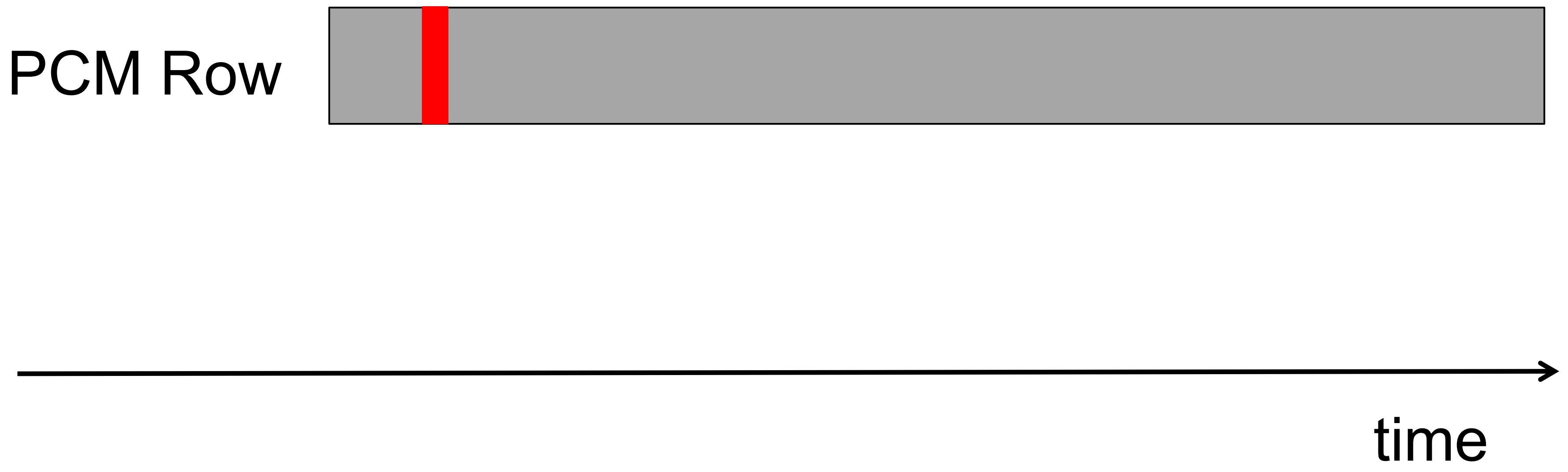

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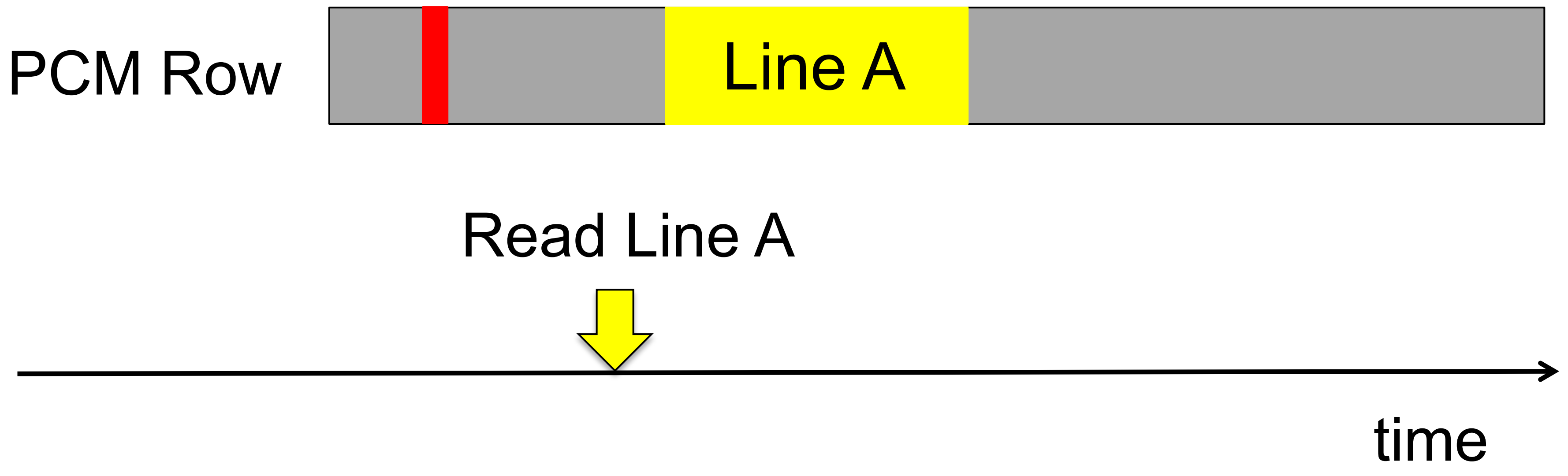

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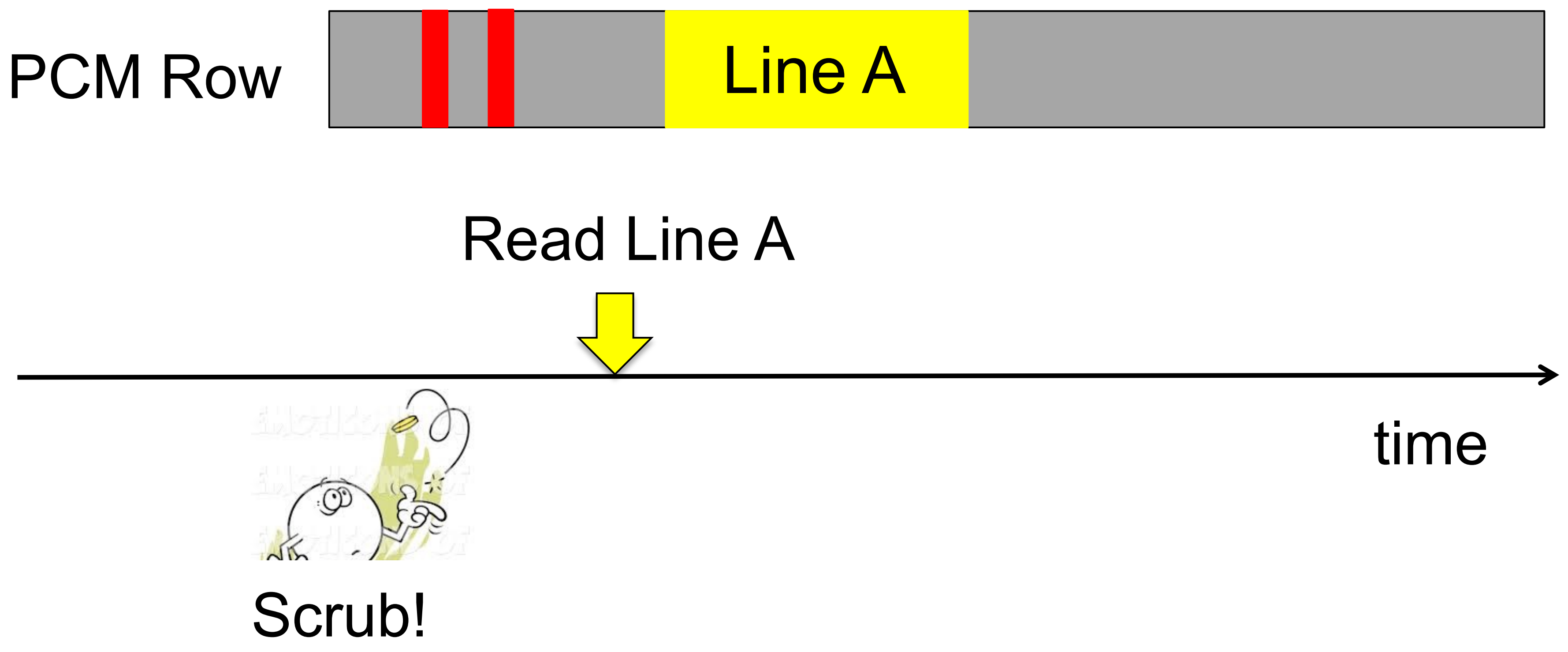

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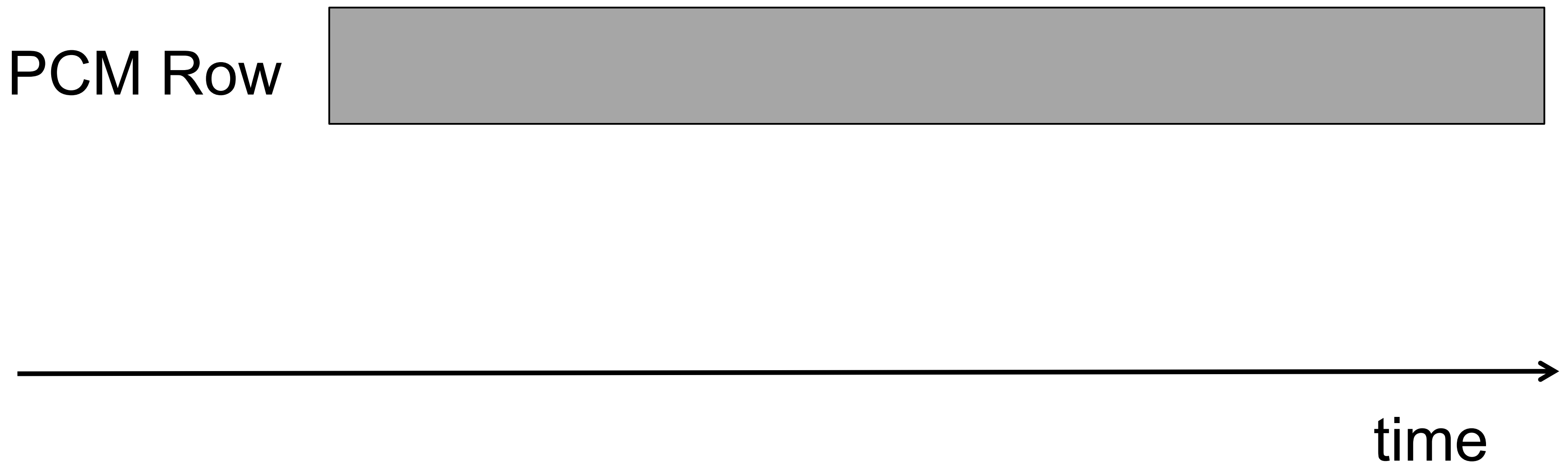

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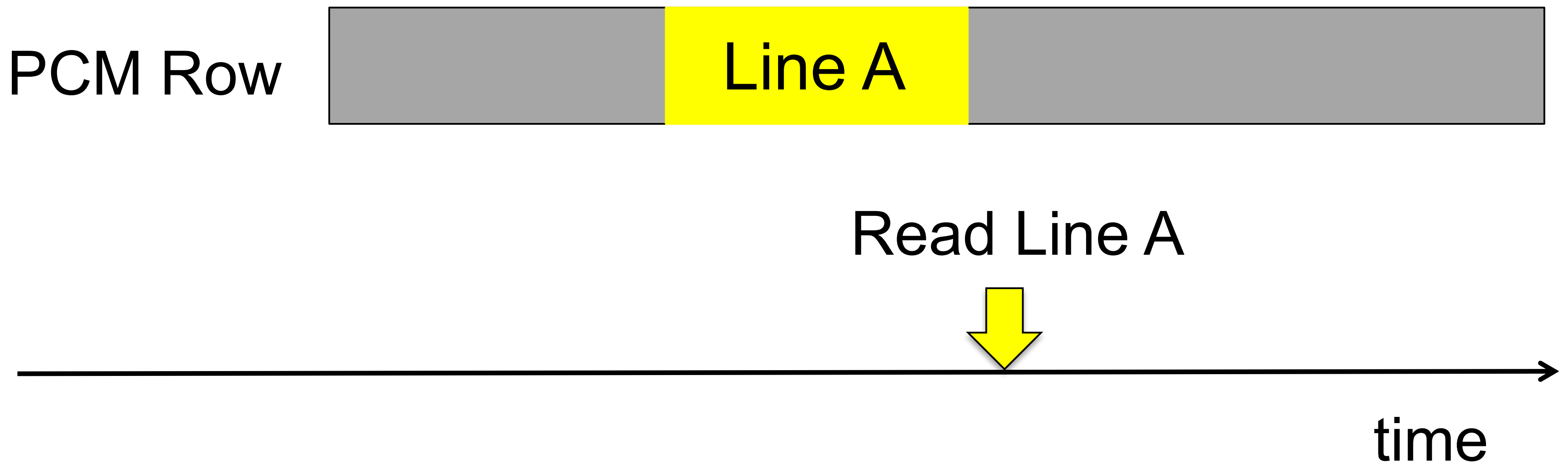

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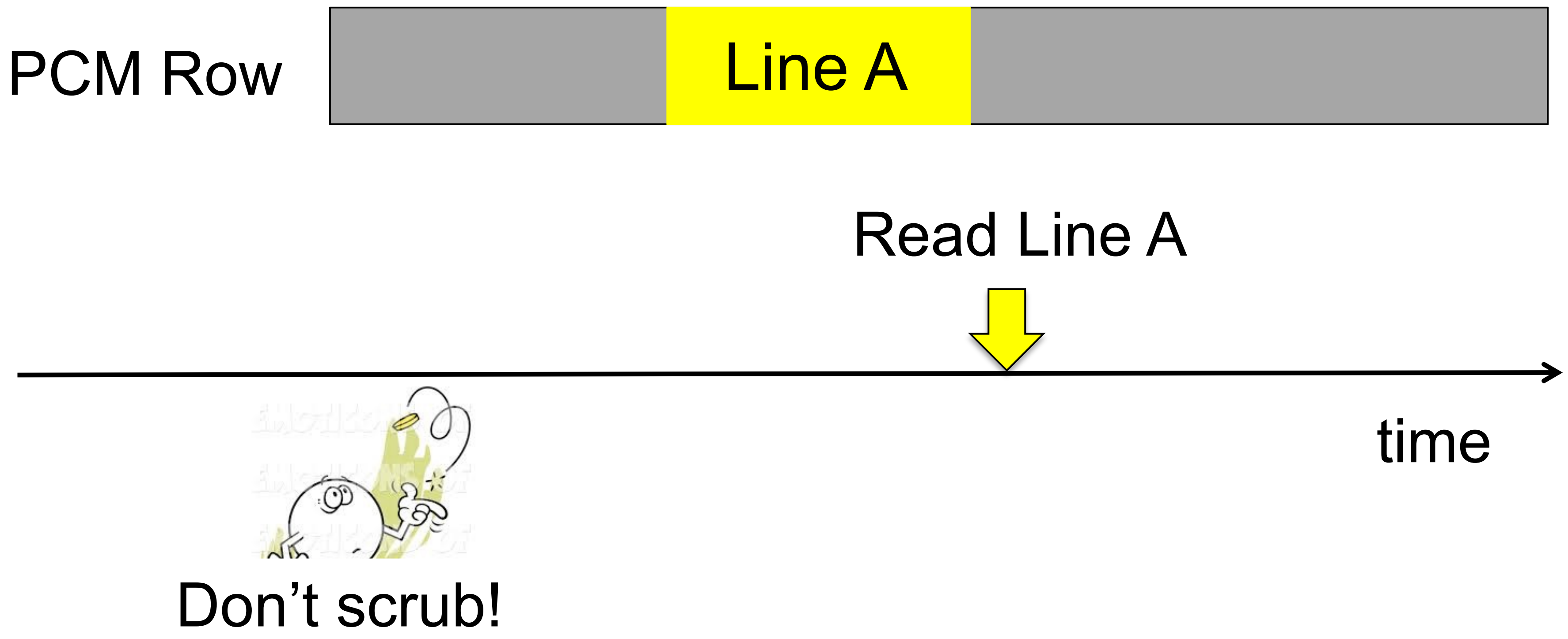

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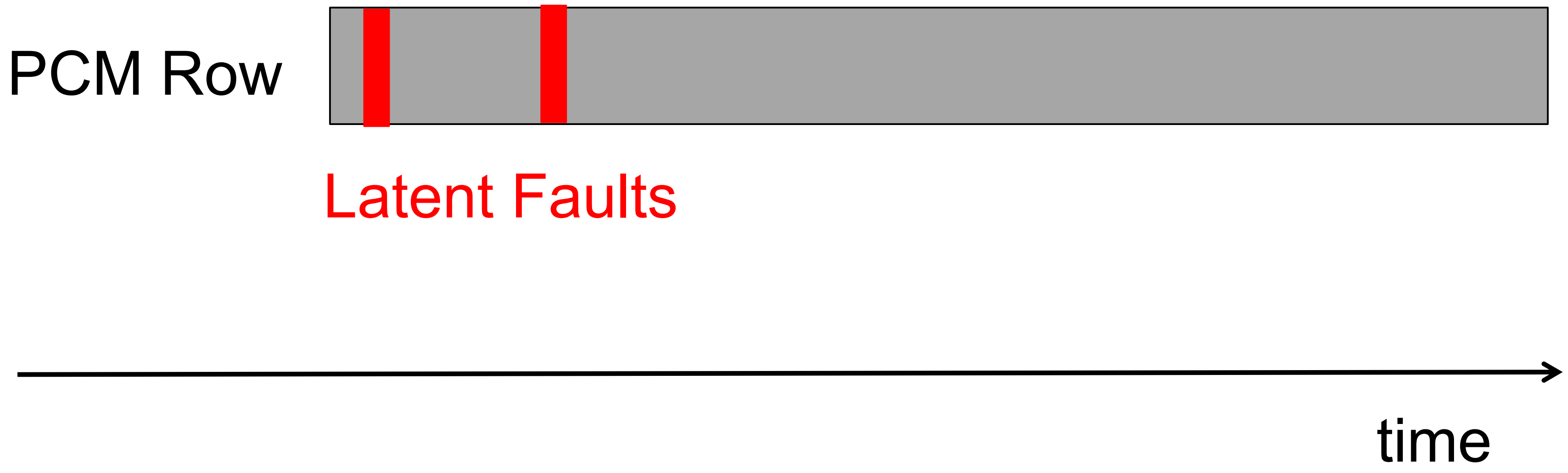

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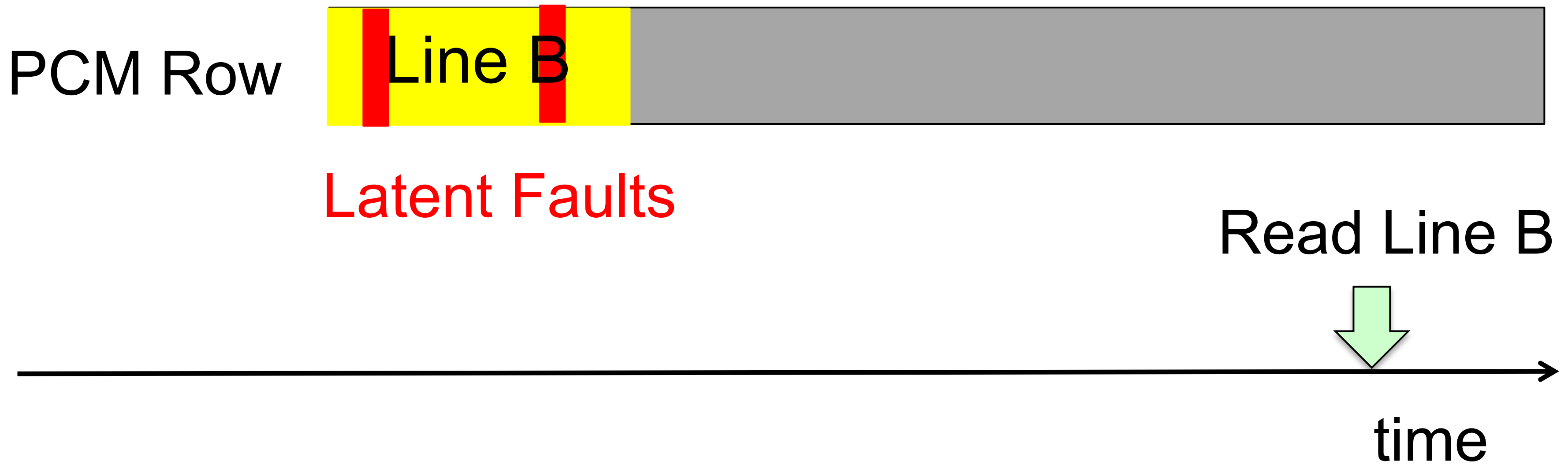

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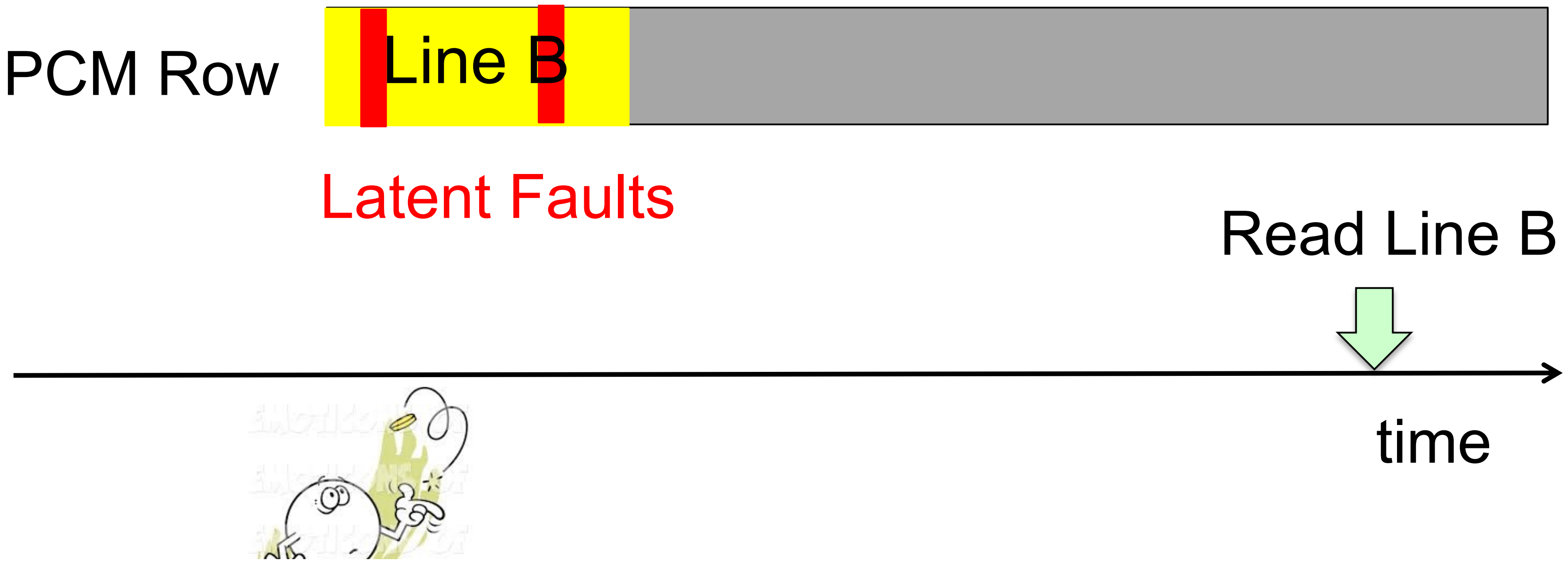

Don’t scrub!

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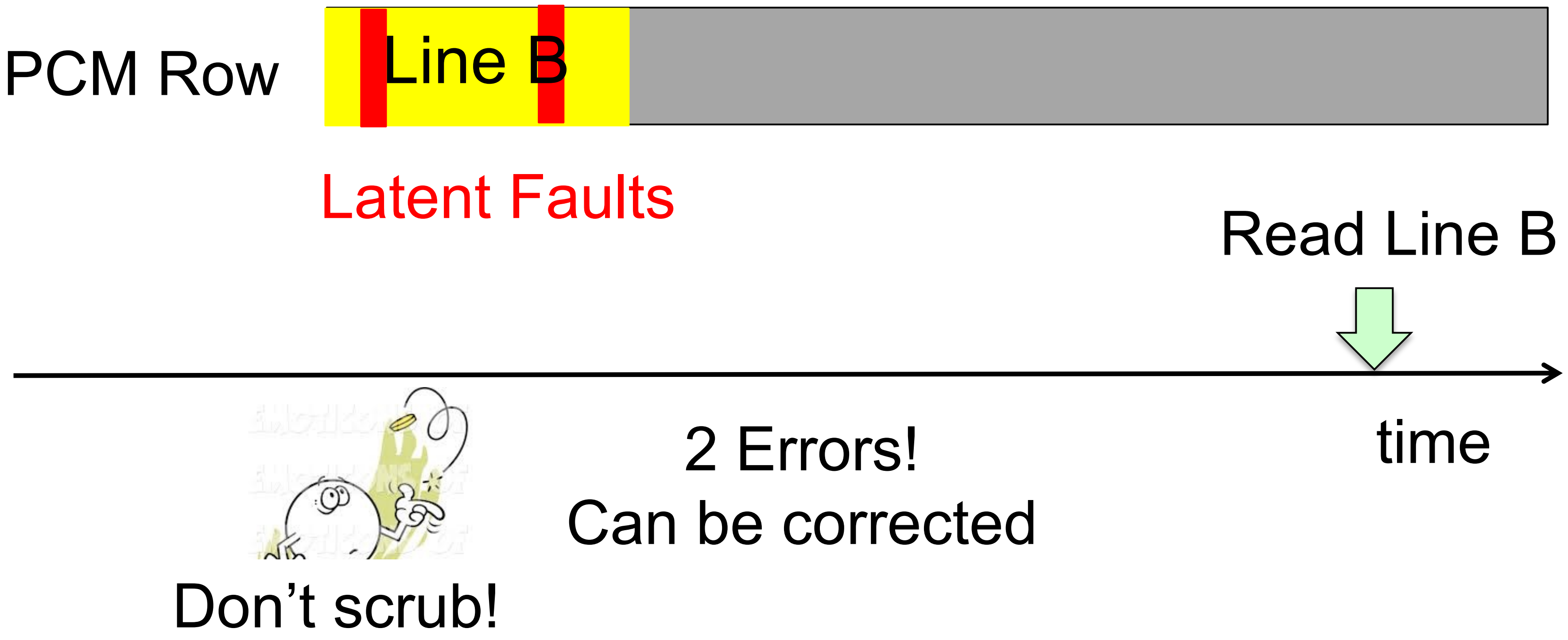

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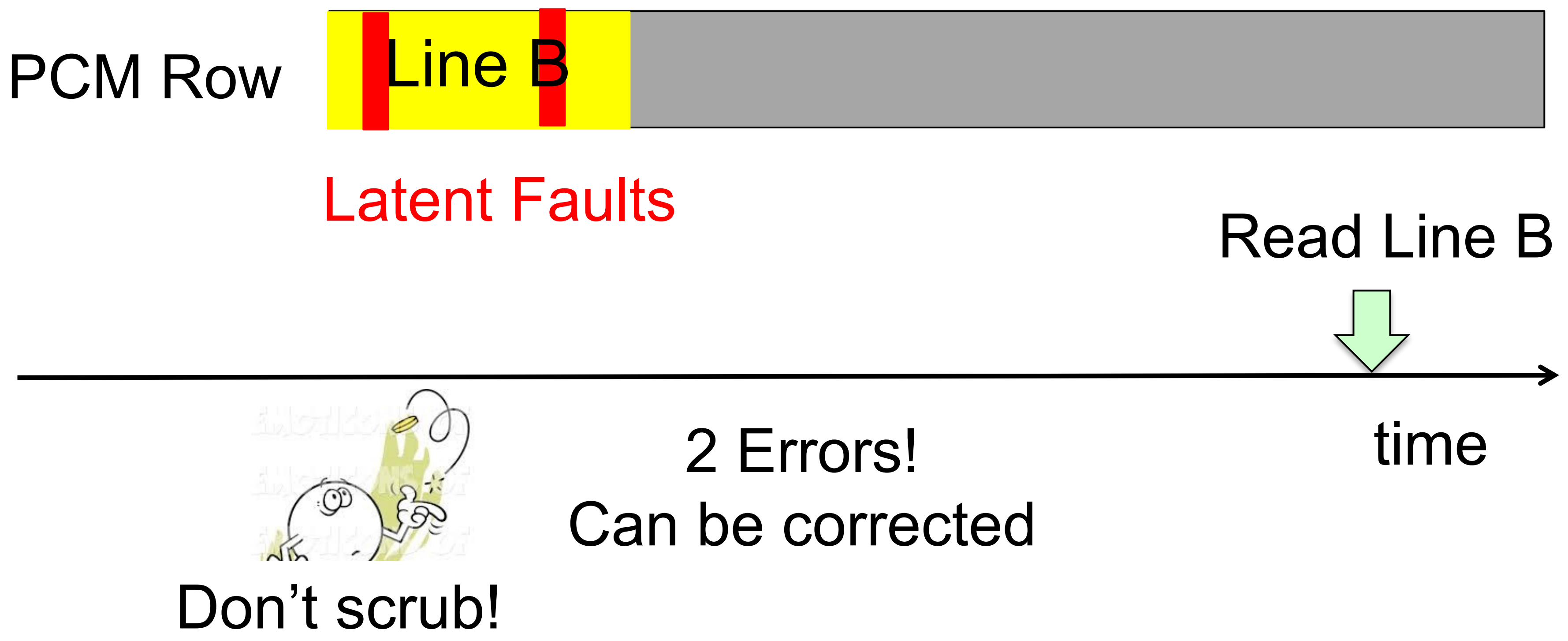

Probabilistic Scrub improves reliability by 10^5 times with negligible impact on performance

END OF BACKUP