AVATAR: A VARIABLE-RETENTION TIME AWARE REFRESH FOR DRAM

DSN-45
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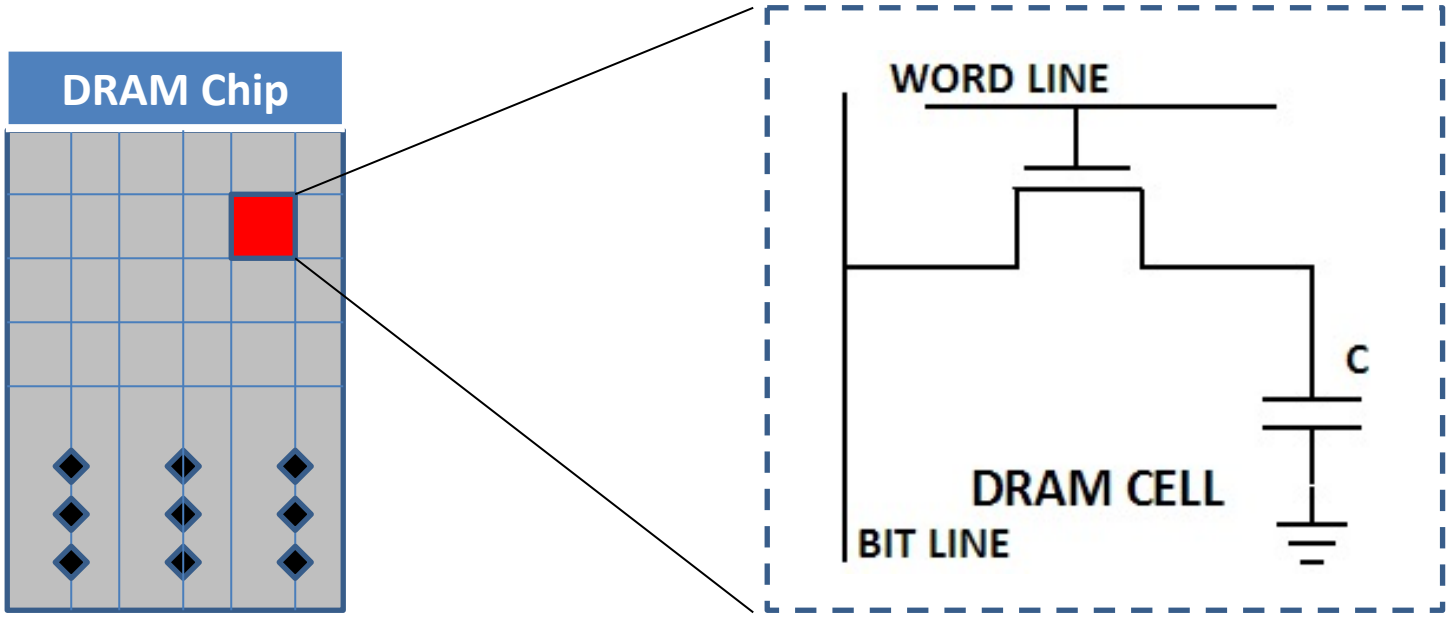
Onur Mutlu

DRAM BACKGROUND

Dynamic Random Access Memory (DRAM) stores data as charge on capacitor



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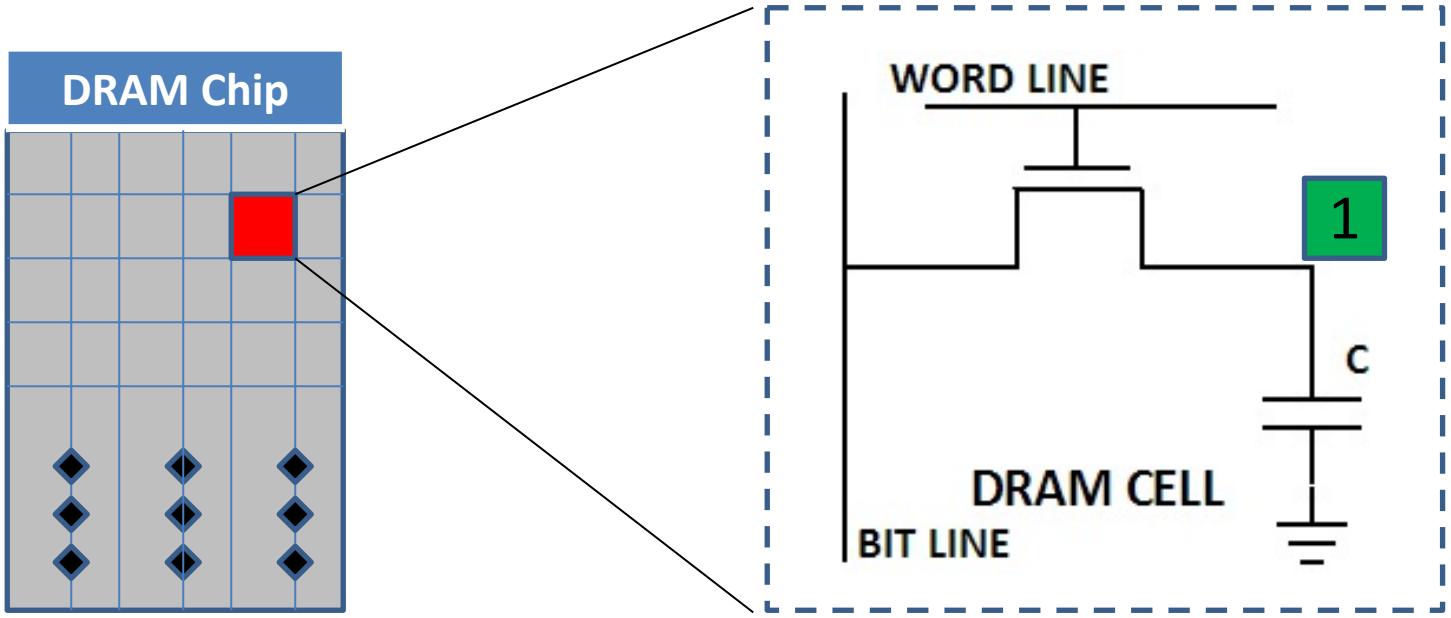

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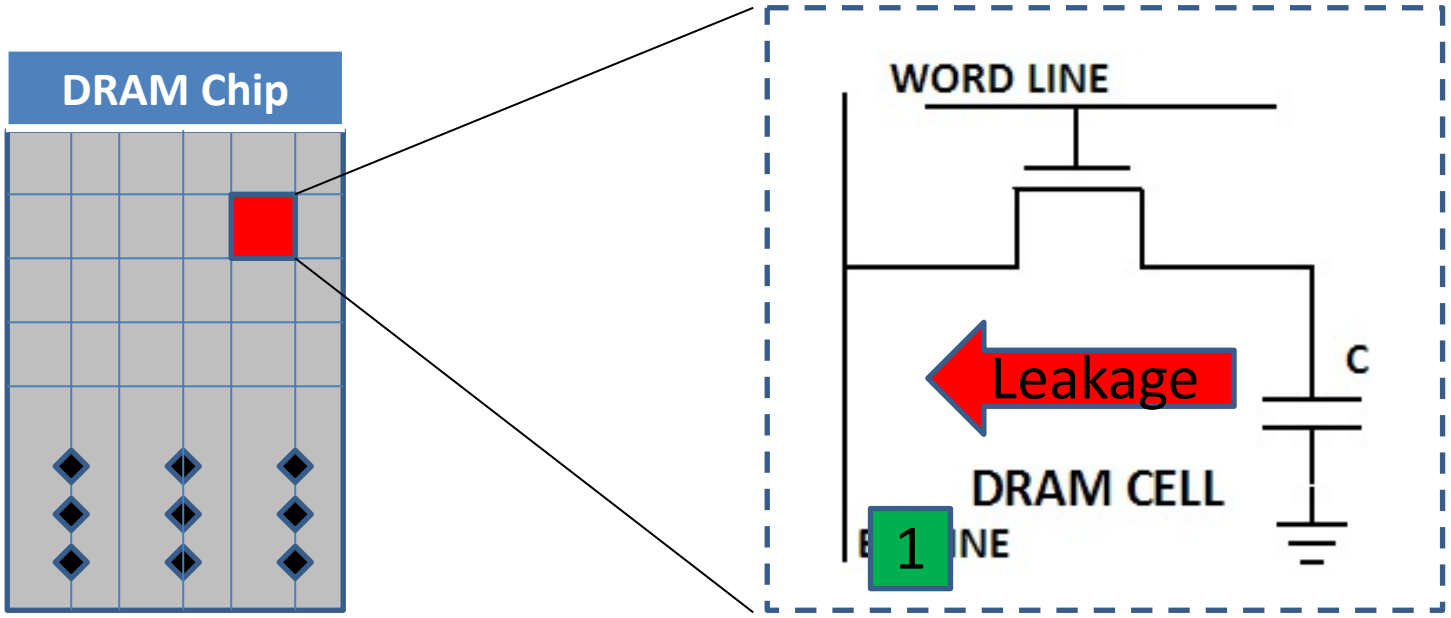
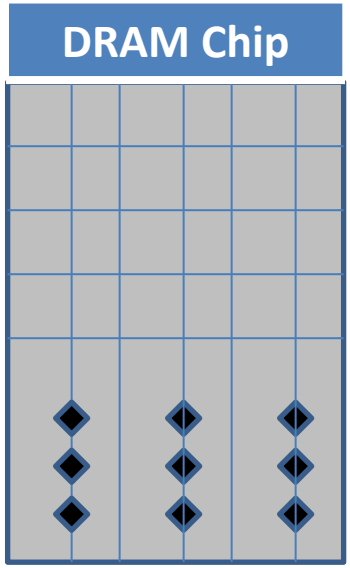


DRAM is a volatile memory → charge leaks quickly

DRAM REFRESH

Retention Time: The time for which cell/memory retains data

DRAM maintains data by “refresh” operations at row granularity



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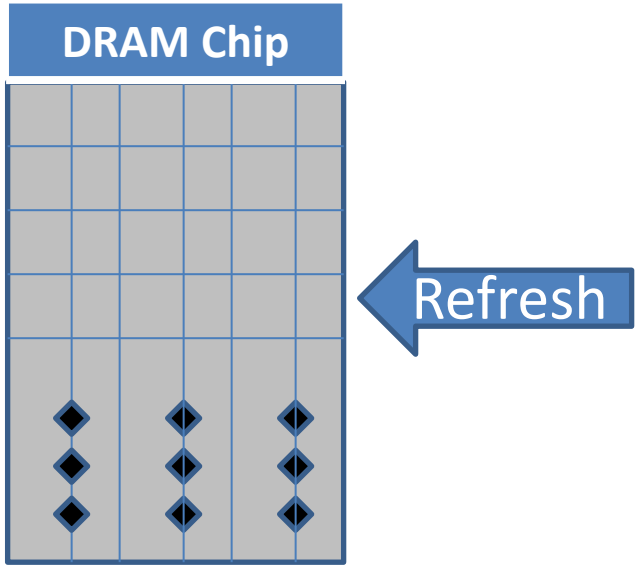

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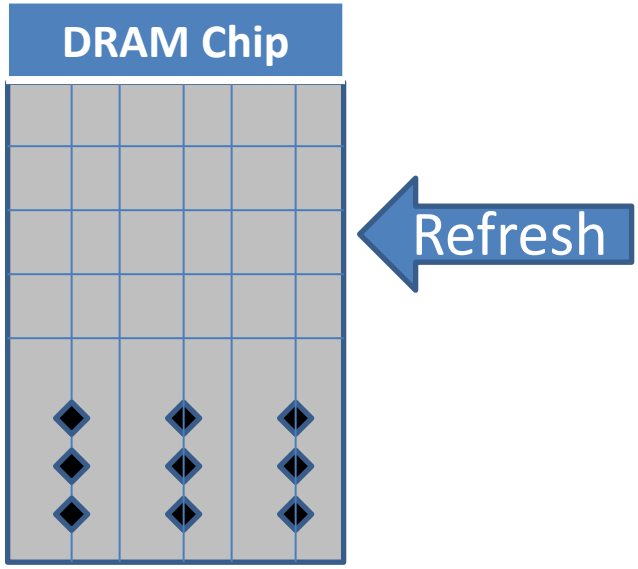

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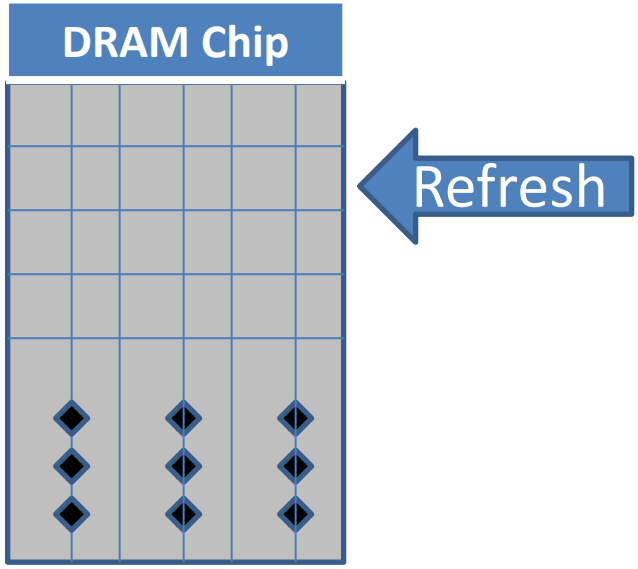

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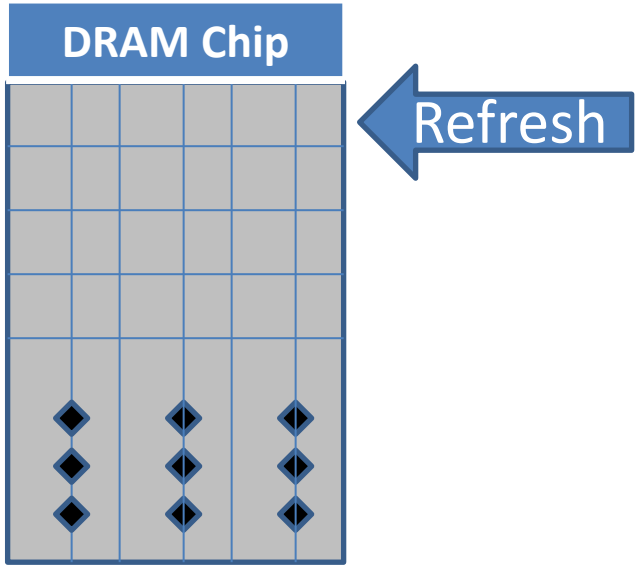

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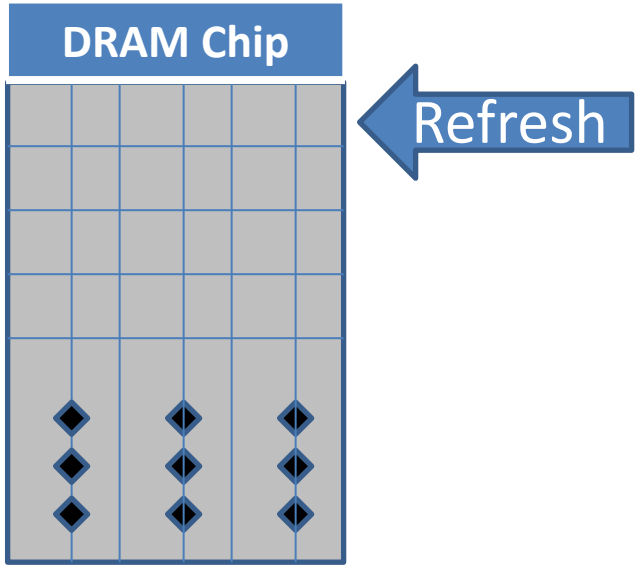
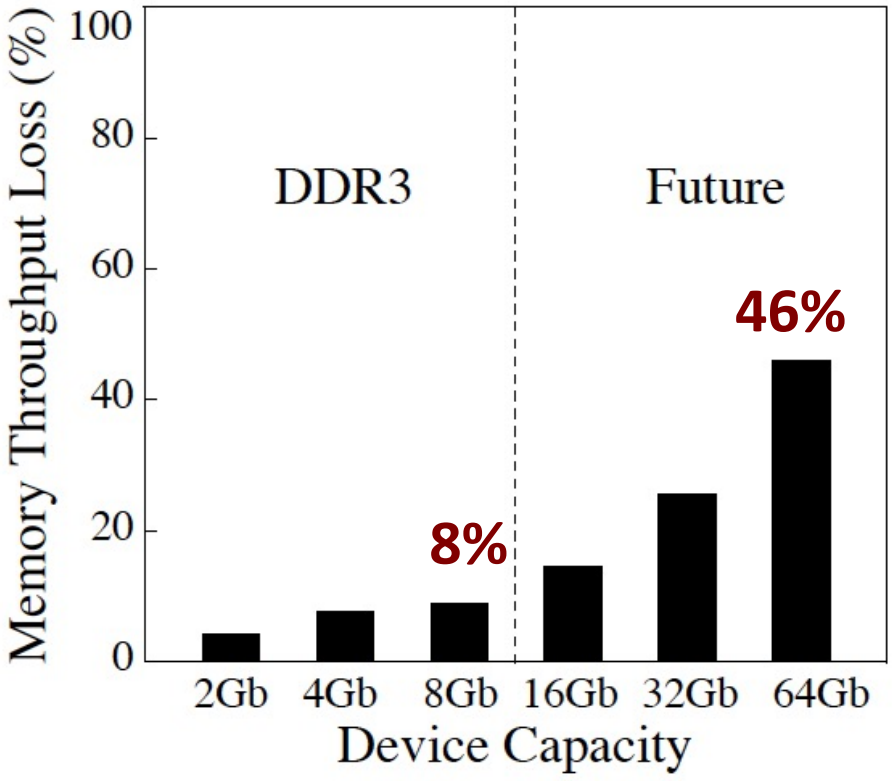


Refresh period determined by "worst-case" cell: 64ms (JEDEC)

DRAM relies on refresh (64ms) for data integrity

"REFRESH WALL" FOR DRAM SYSTEMS

Refresh cost proportional to capacity ➔ Exponentially increasing



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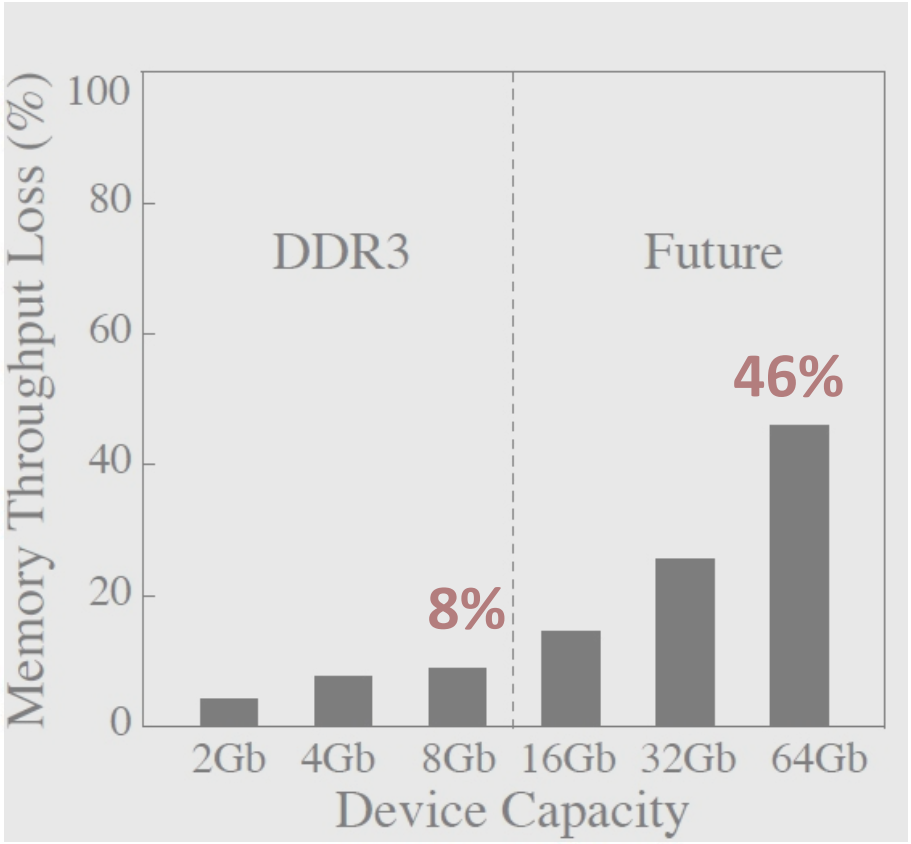

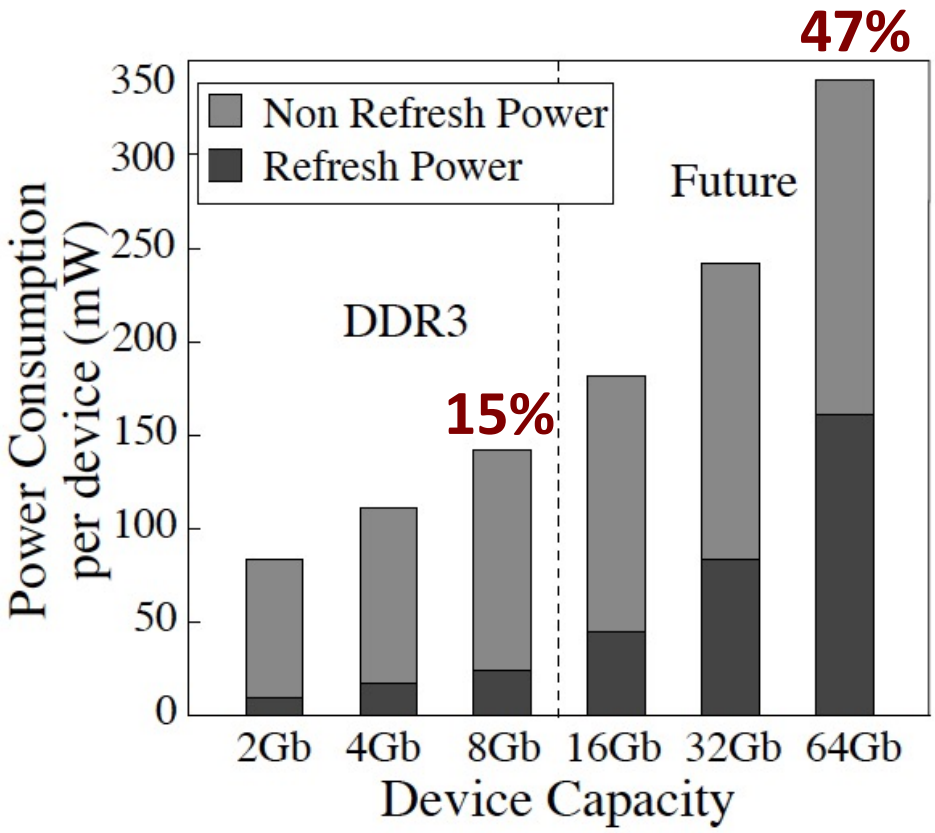

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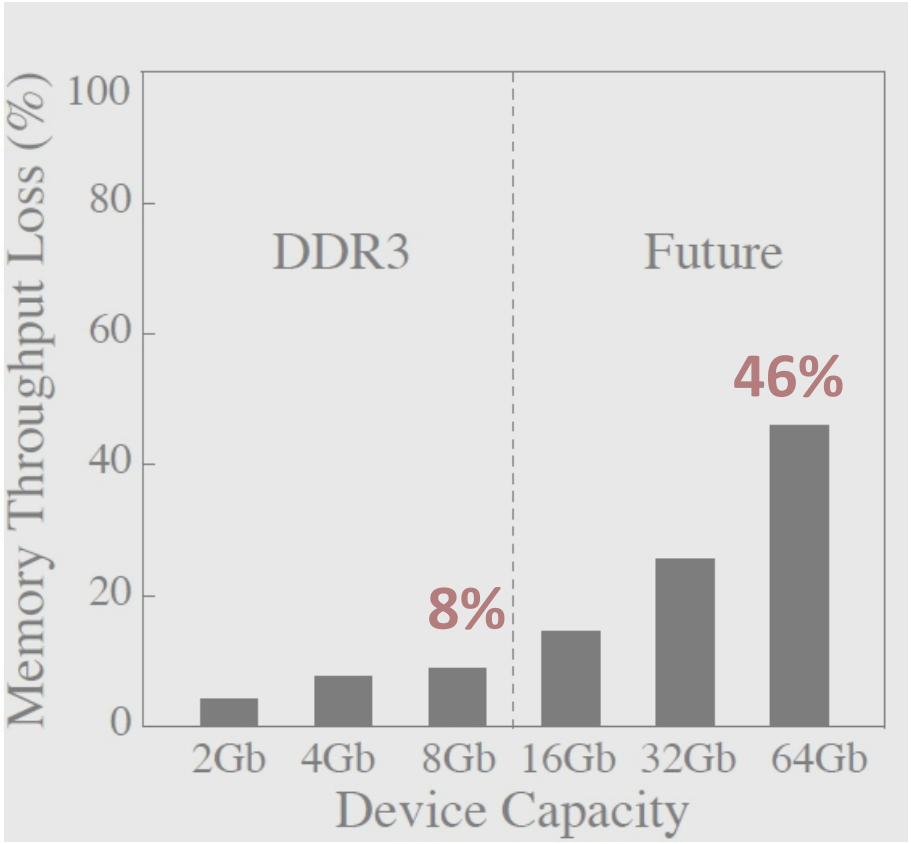

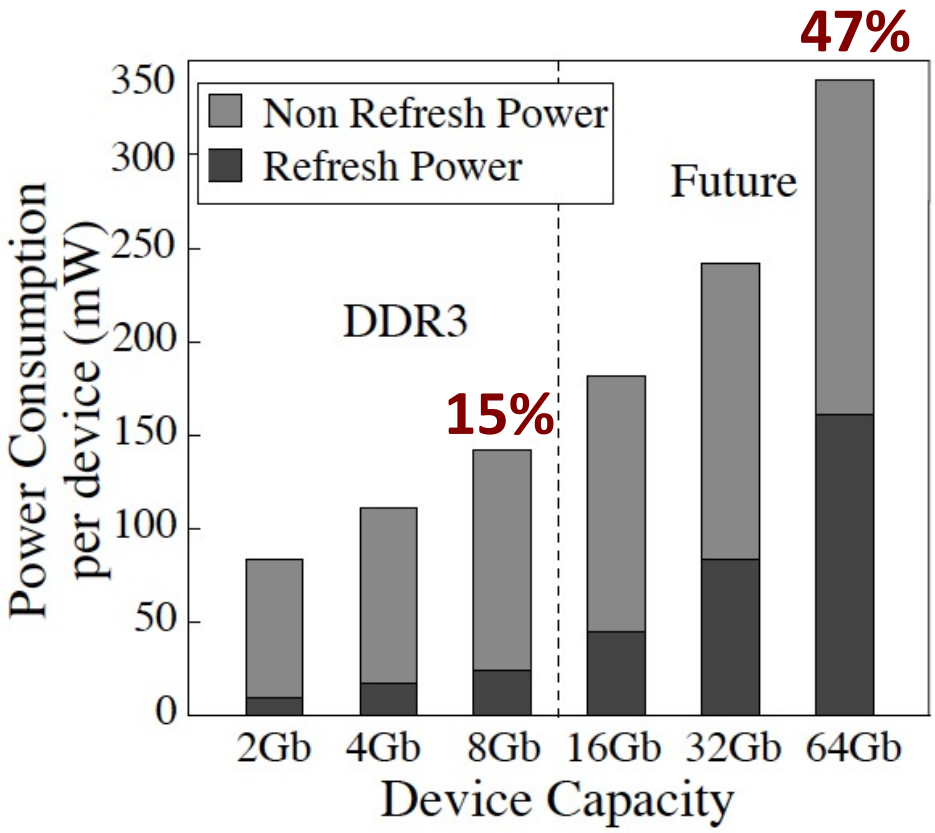

Refresh consumes significant time and energy

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NOT ALL RETENTION TIME IS CREATED EQUAL

Retention time of cells vary significantly: most cells >> 64ms

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Exploit variability in retention time ➔ Multirate Refresh

Normal Refresh (64ms) & Slow Refresh (e.g. 256ms+)

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Row contains a cell with retention time < period of Slow Refresh

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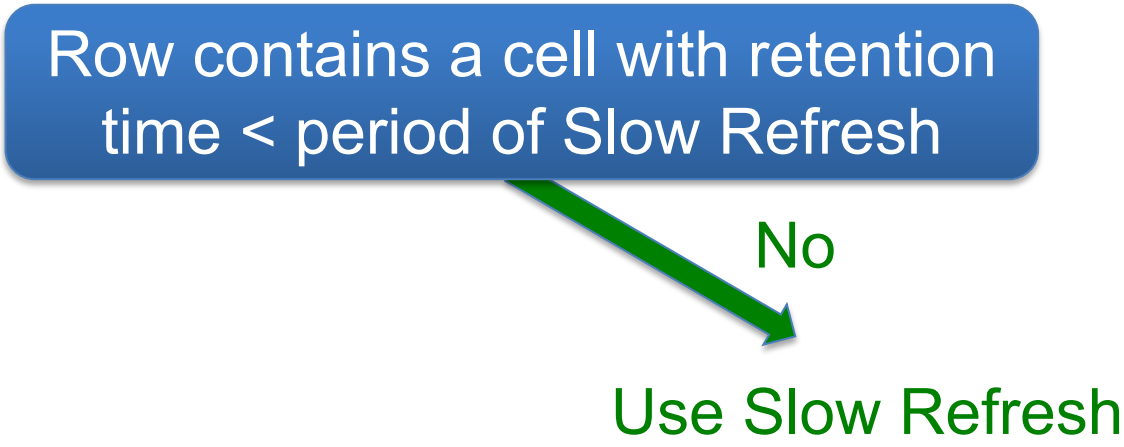

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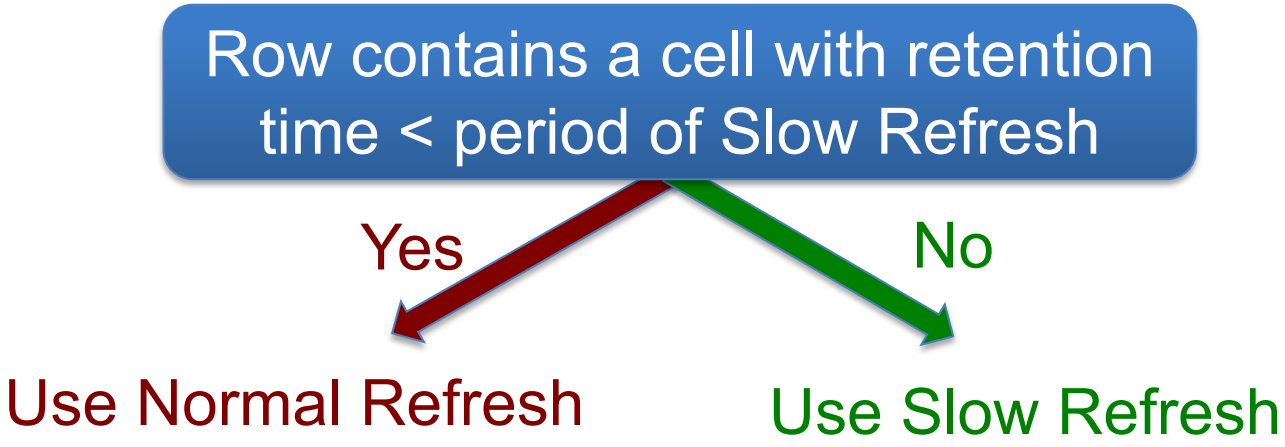

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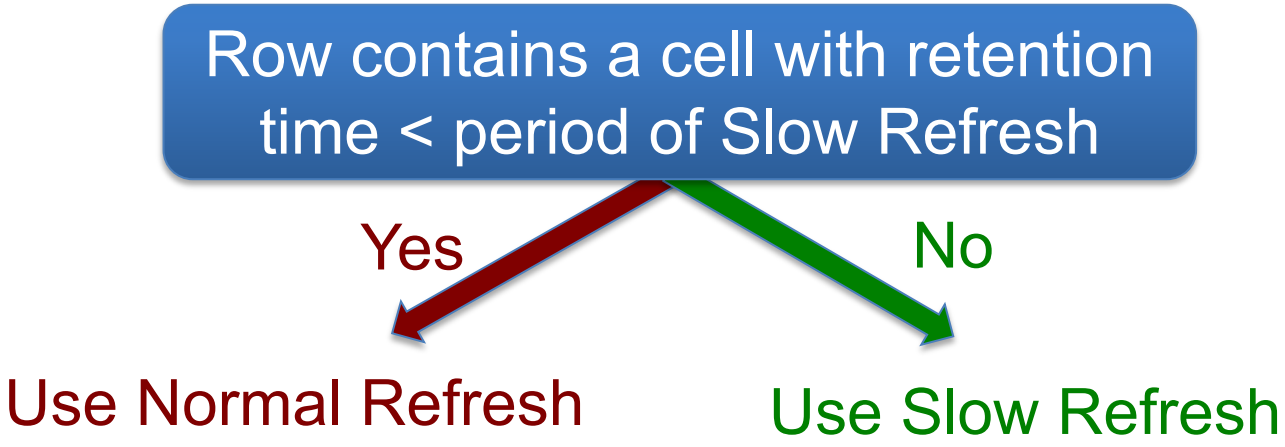

Efficient DRAM refresh by exploiting variability

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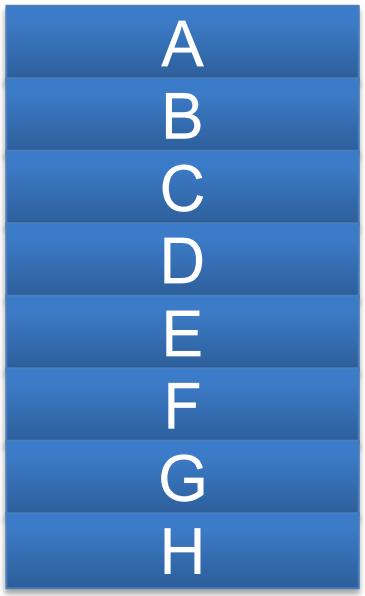
MULTI RATE REFRESH: DESIGN & EFFECTIVENESS

DRAM Rows



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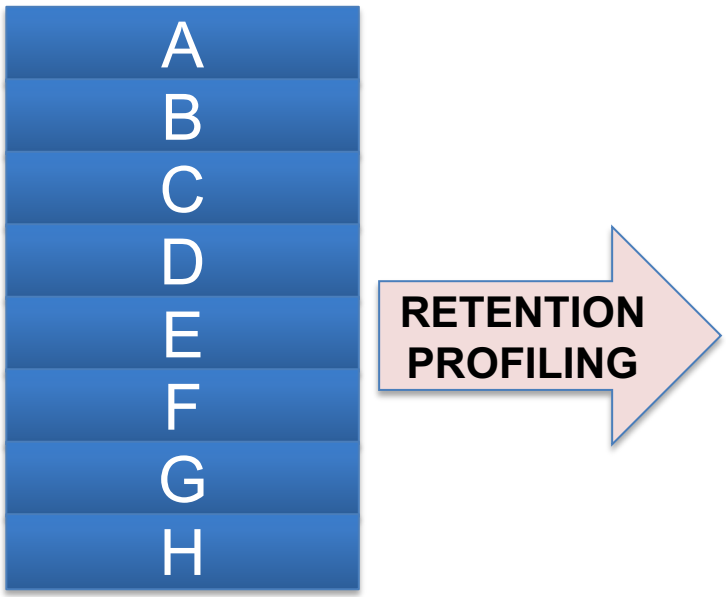

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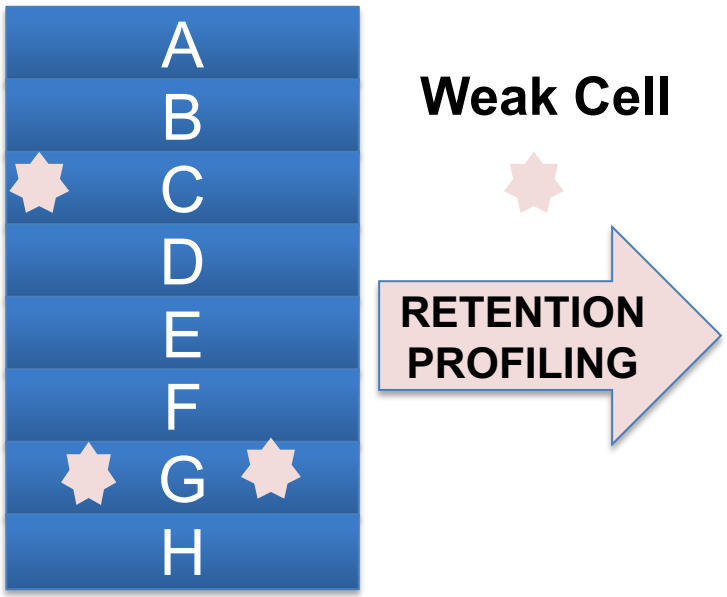

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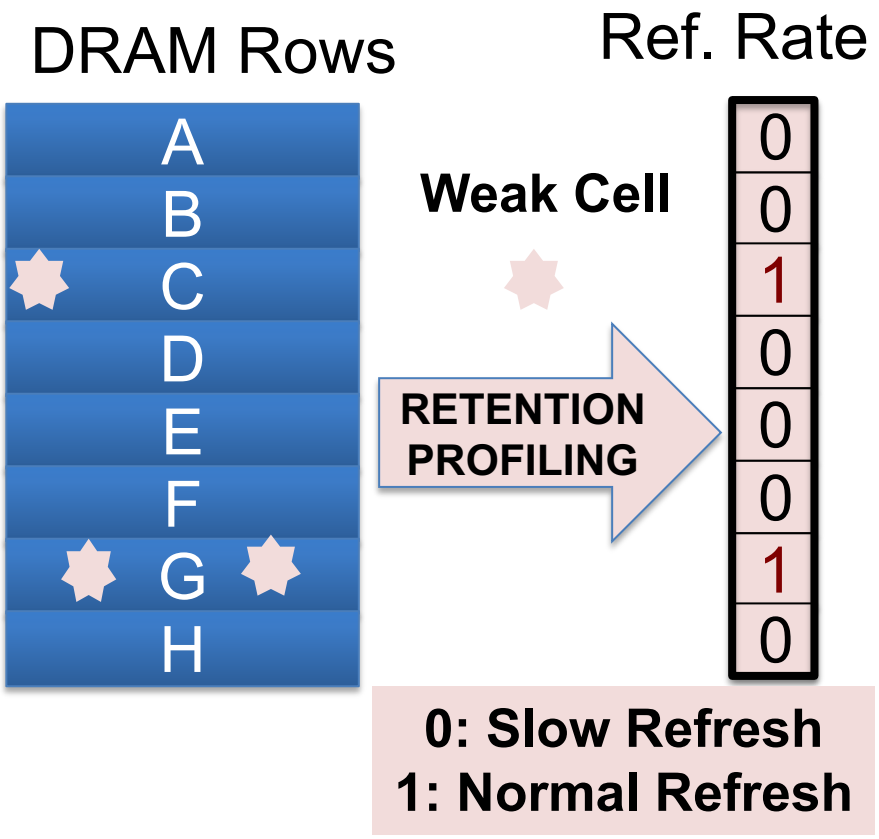

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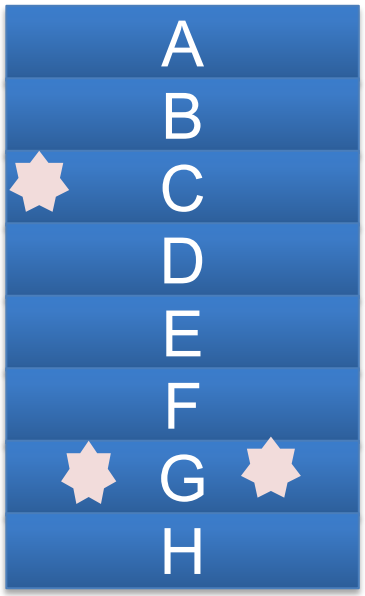


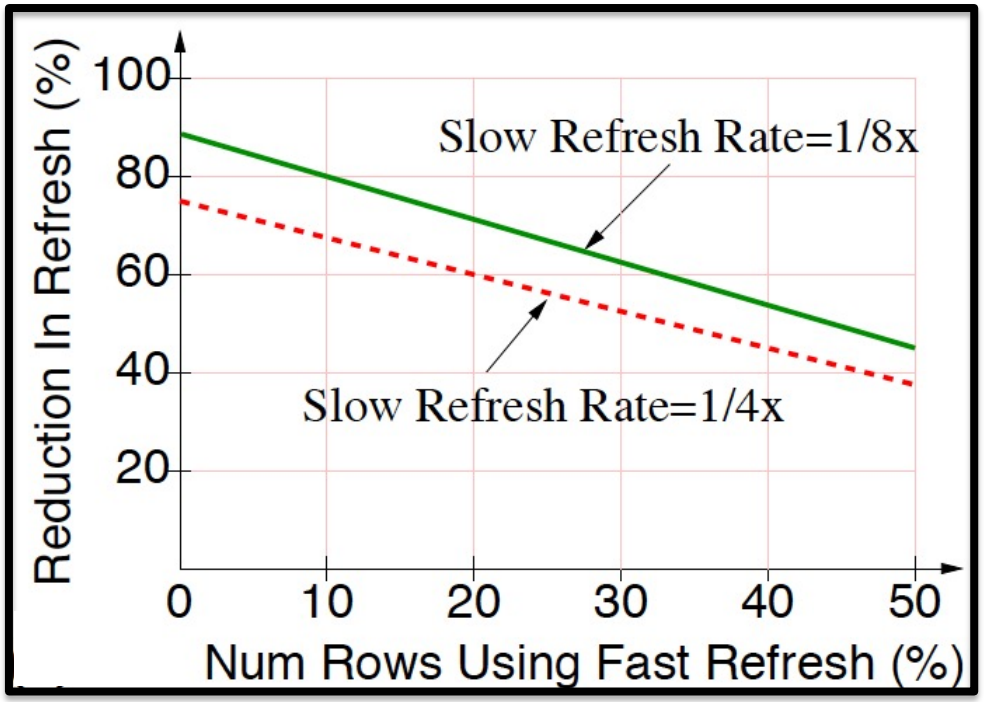
Weak Cell

RETENTION PROFILING

Ref. Rate Table

0
0
1
0
0
0
1
0

0: Slow Refresh
1: Normal Refresh



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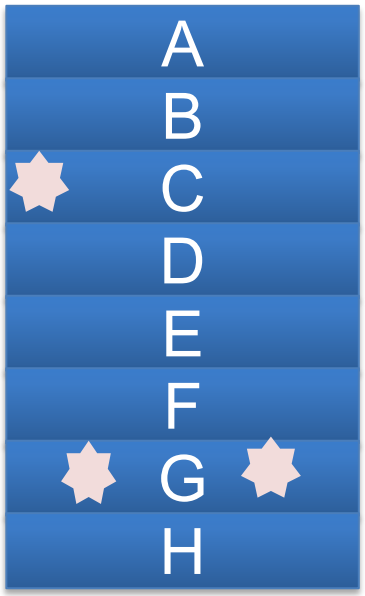

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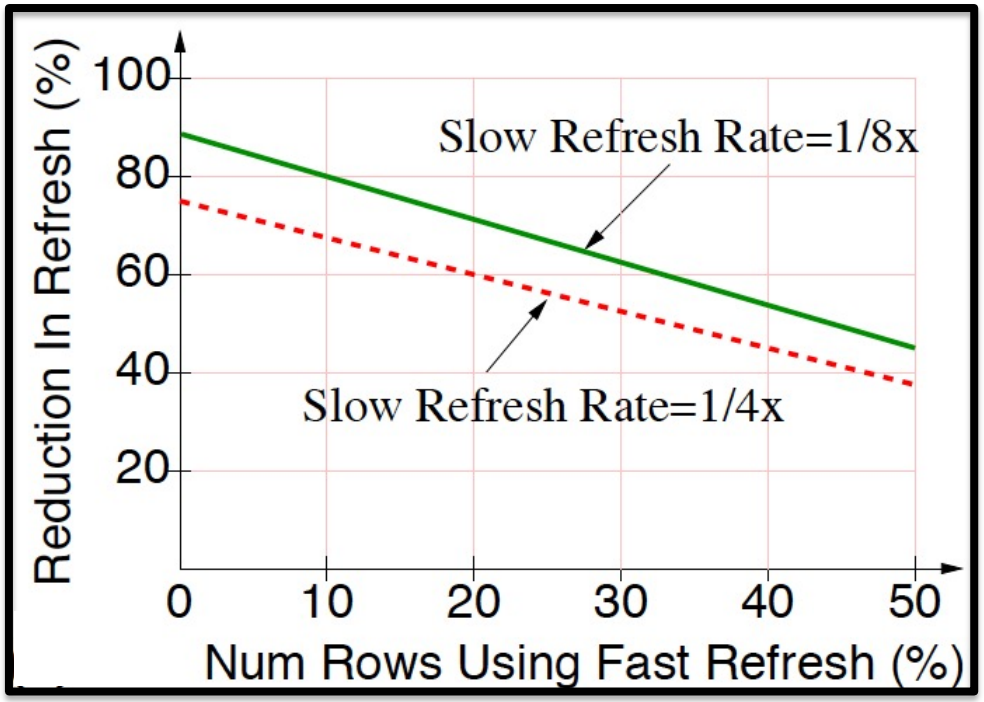
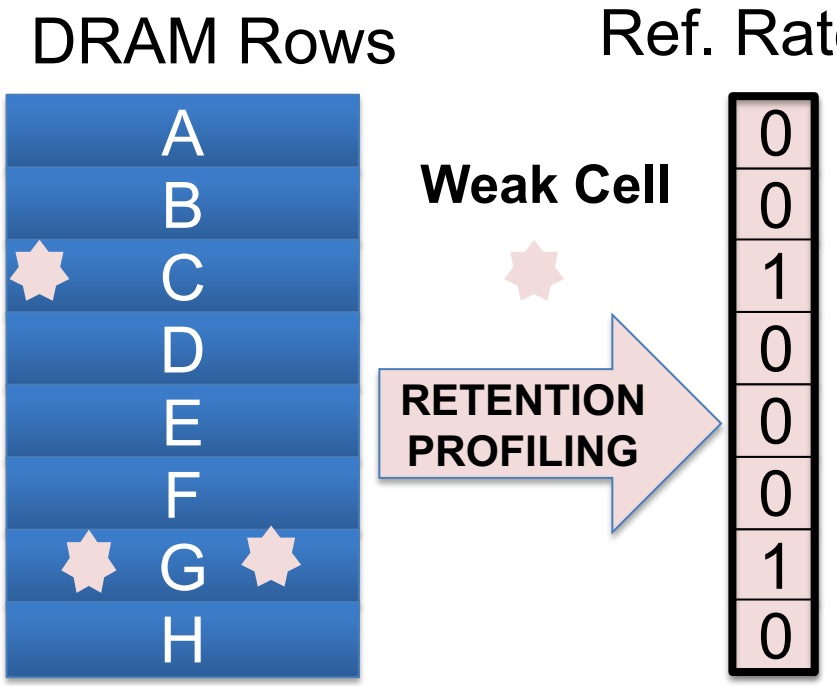


Multi rate refresh can reduce refresh by 70%+

VARIABLE RETENTION TIME (VRT): THE NEMESIS

Multirate refresh relies on retention time to remain unchanged

Retention time can vary at runtime due to VRT



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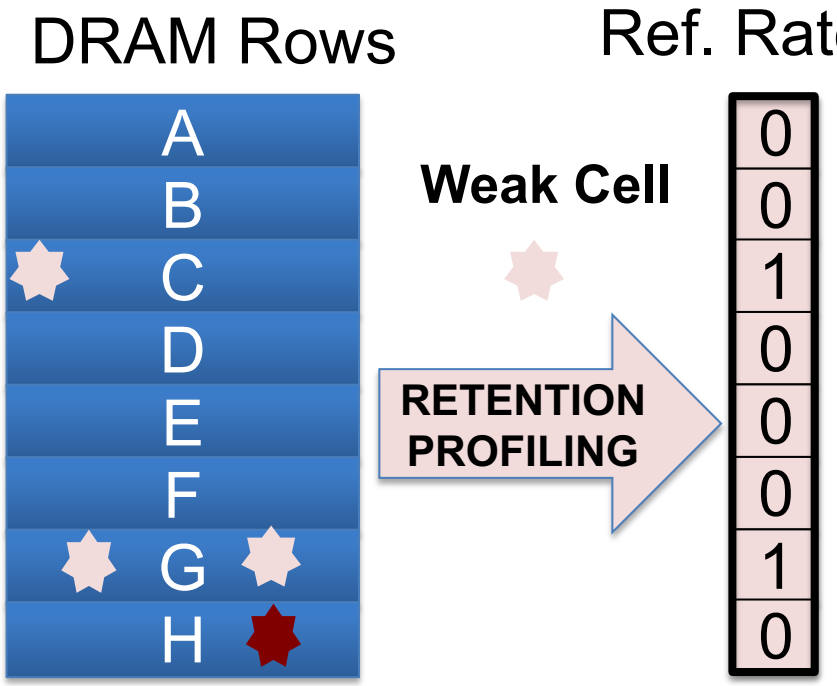

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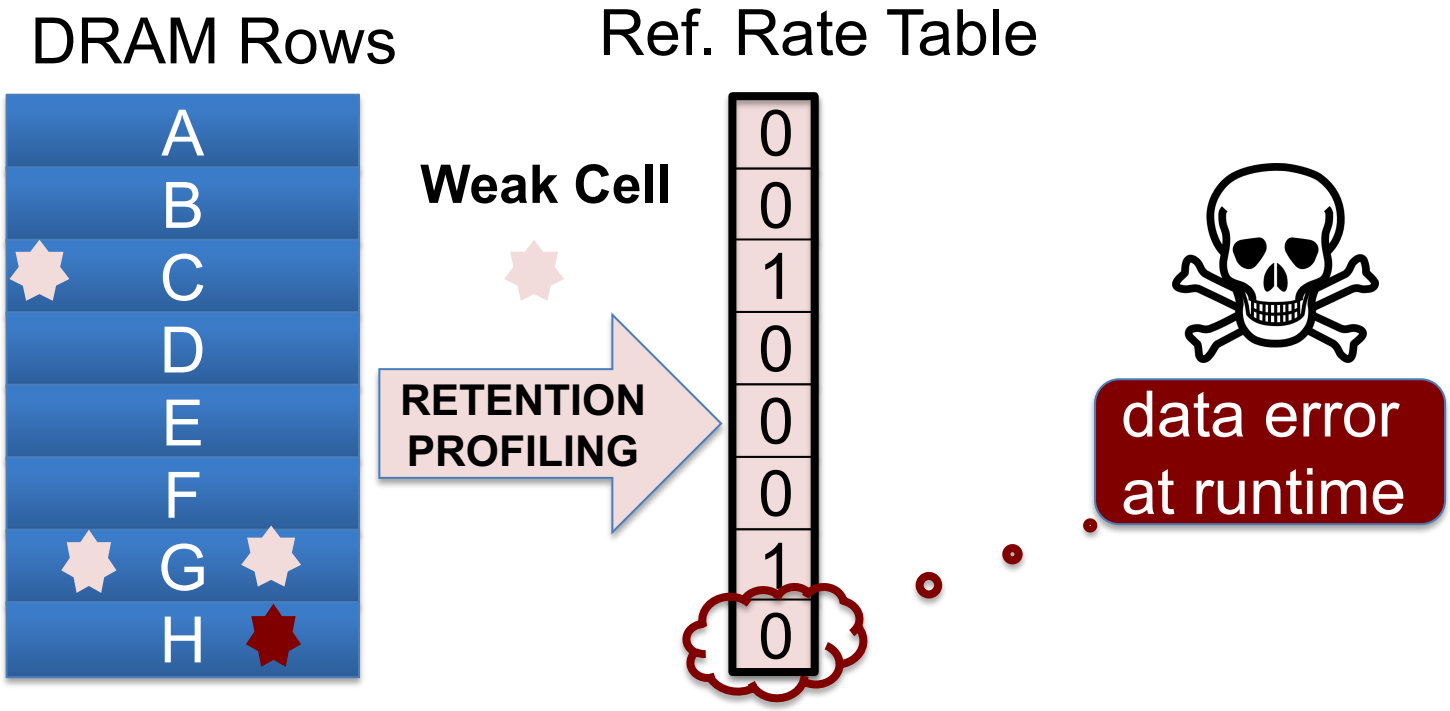

VRT renders multi-rate refresh unusable in practice

GOALS

VRT considered one of the biggest impediment to DRAM scaling
-- [Samung & Intel, Memory Forum 2014]

Our study investigates the following questions:

1. Can we analyze VRT using architecture level models?
2. Can we overcome VRT simply by using ECC DIMM?
3. If not, what is a low cost solution to mitigate VRT?

OUTLINE

- Background
- VRT: mechanism, measurement, model
- Can't we fix VRT by simply using ECC DIMM?
- AVATAR
- Results
- Summary

WHY DOES VRT OCCUR? WHEN IS IT HARMFUL?

VRT caused by fluctuations in Gate Induced Drain Leakage.

External factors: mechanical stress, high temperature etc.

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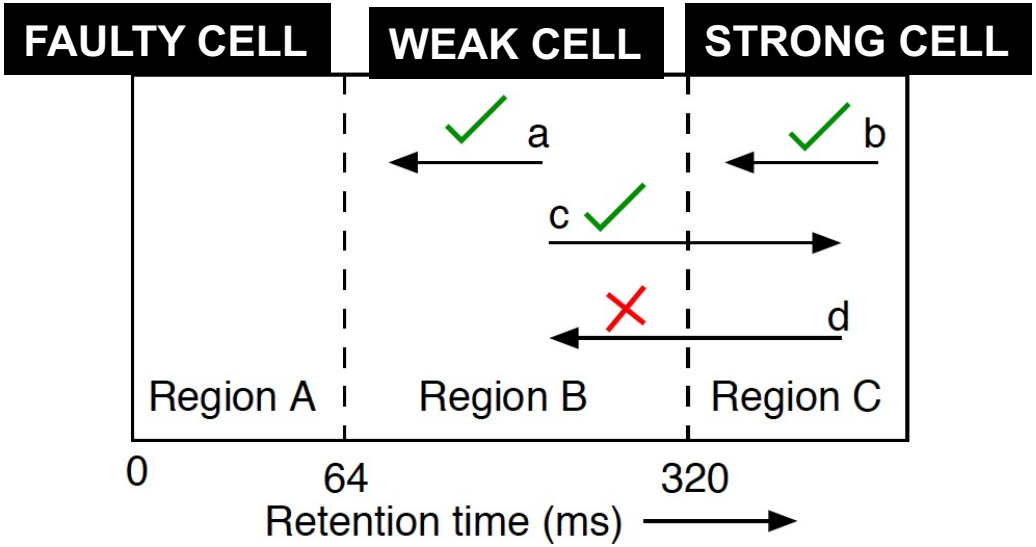
Not all VRT is harmful



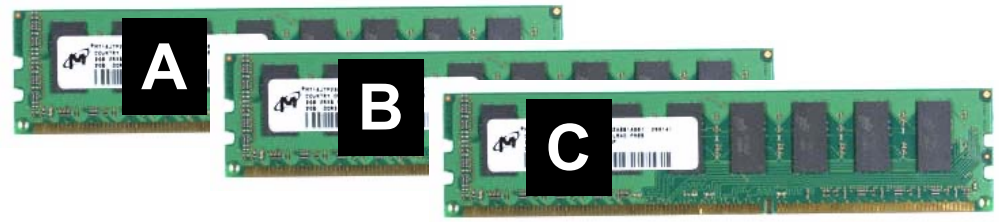
VRT problematic when strong cell becomes weak

EXPERIMENTAL SETUP

Test platform: DDR3 testing platform Xilinx ML605 FPGA development board in temperature controlled setting

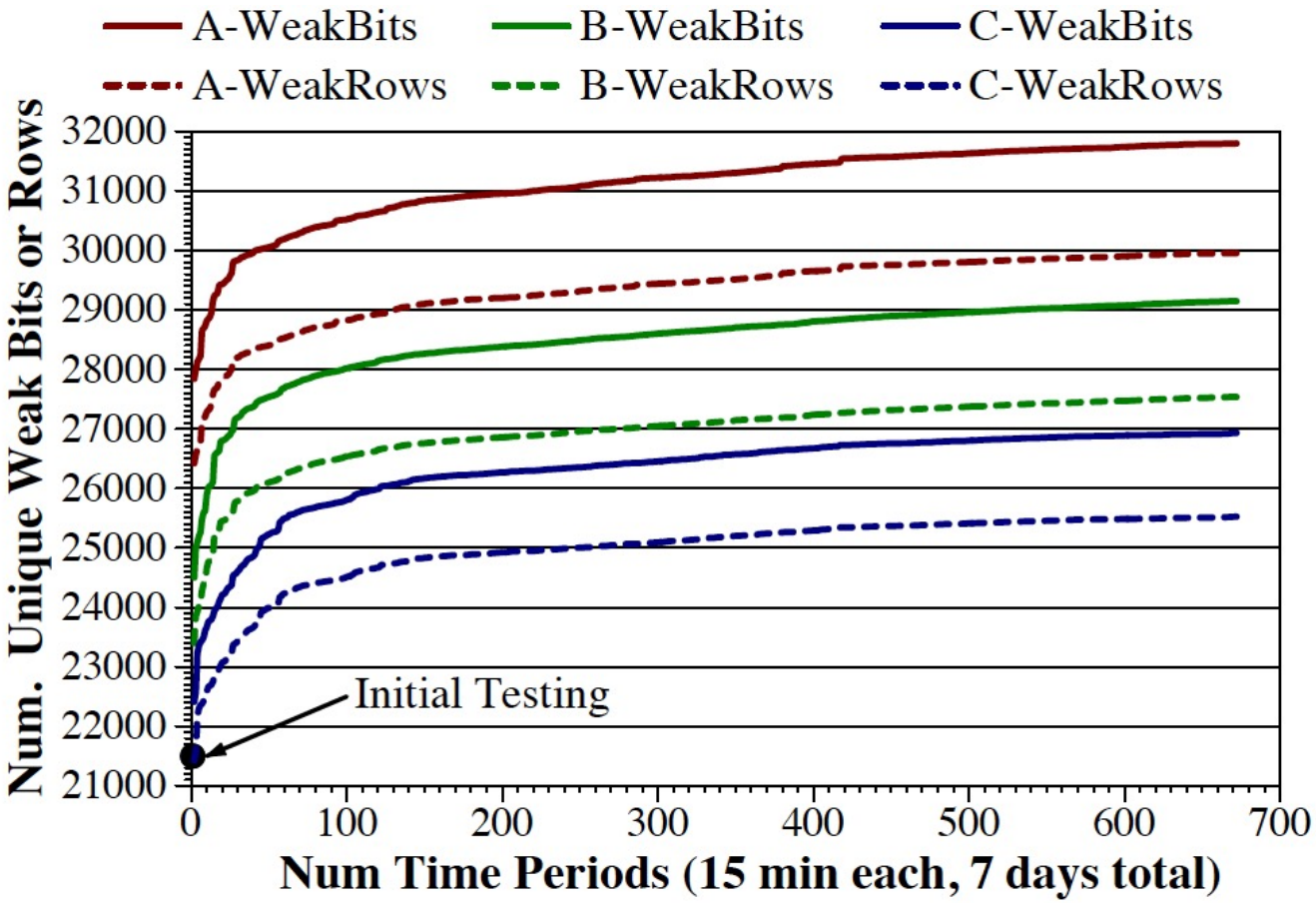
Slow Refresh: Studied refresh of 4s at 45C, corresponds to 328ms at 85C [khan+ SIGMETRICS'14, Liu+ ISCA'13]

Test: Write specific pattern, read pattern, log id of erroneous cell
Statistics collected every 15 minutes, over 7 days (672 rounds)



Three (2GB) modules, one each from different DRAM vendor

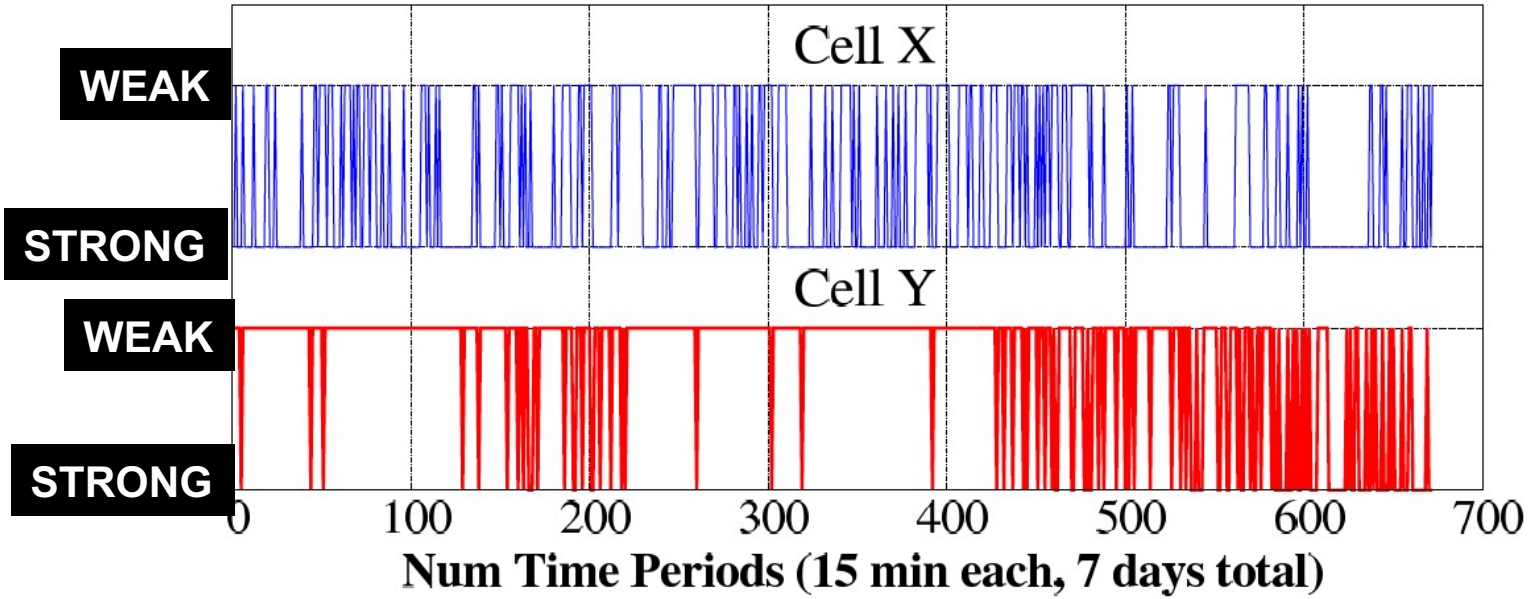
1: POPULATION OF WEAK CELLS INCREASES



Even after several days of testing, VRT causes new (previously unidentified) cells to cause failures

2: VRT-CELLS CAN SWITCH RANDOMLY

Cell with retention time < 328ms ➔ Weak Cell, else Strong Cell

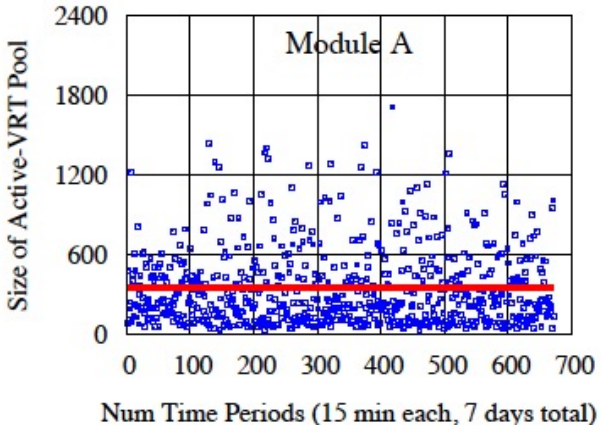


A VRT cell can randomly and frequently transition between strong and weak states

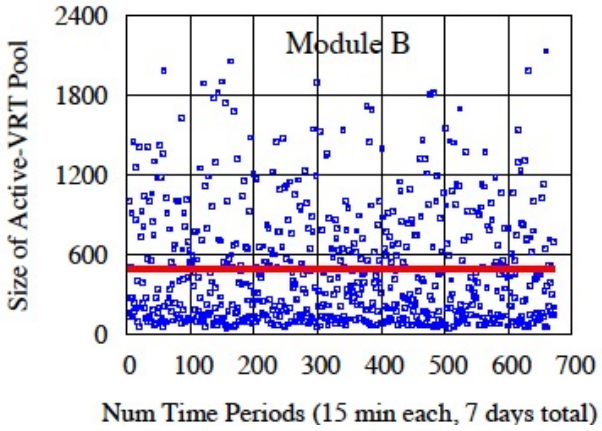
3: SIZE OF ACTIVE-VRT POOL VARIES

Active-VRT Cell: Cell that failed during the given 15-min round

Active-VRT Pool (AVP): Group of Active VRT Cells



Avg=347



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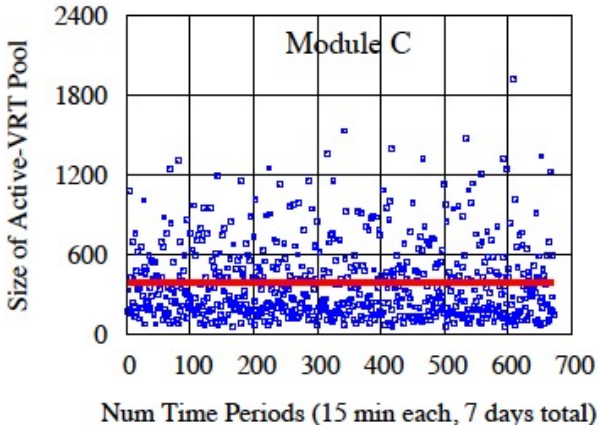


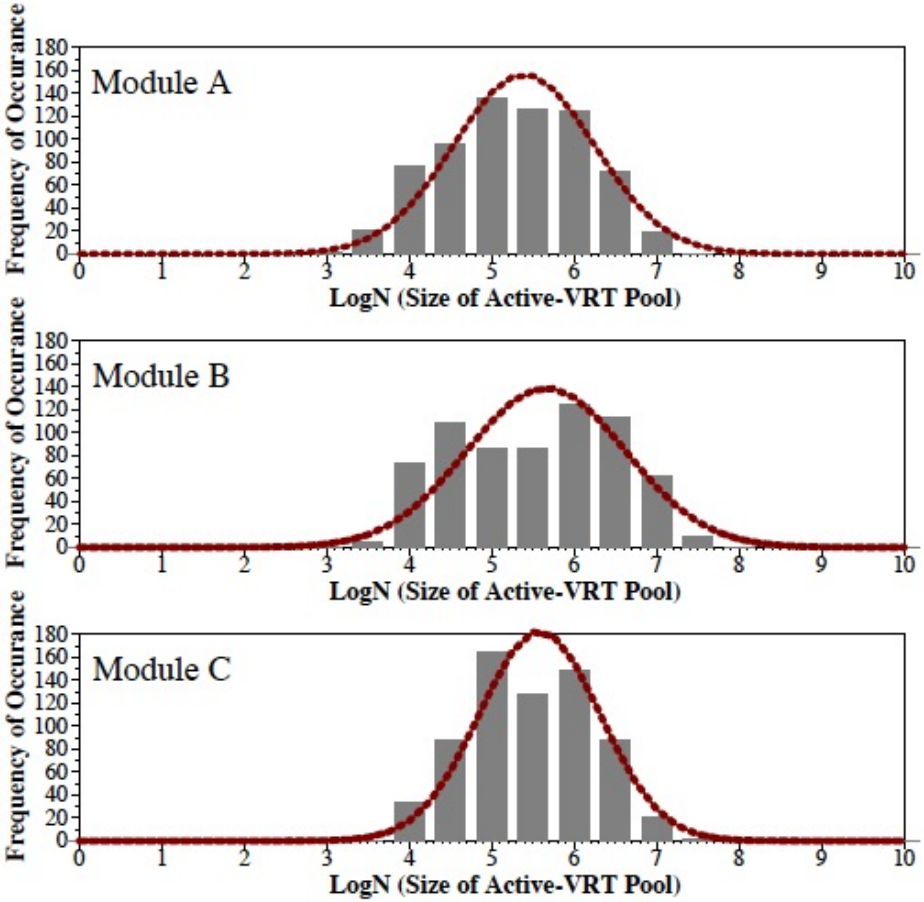
Avg=388

The size of AVP varies dynamically for all modules

MODELING THE DYNAMIC SIZE OF AVP

Predicting the exact AVP size is difficult, but it can be modeled

Observation:
AVP size tends to follow lognormal distribution

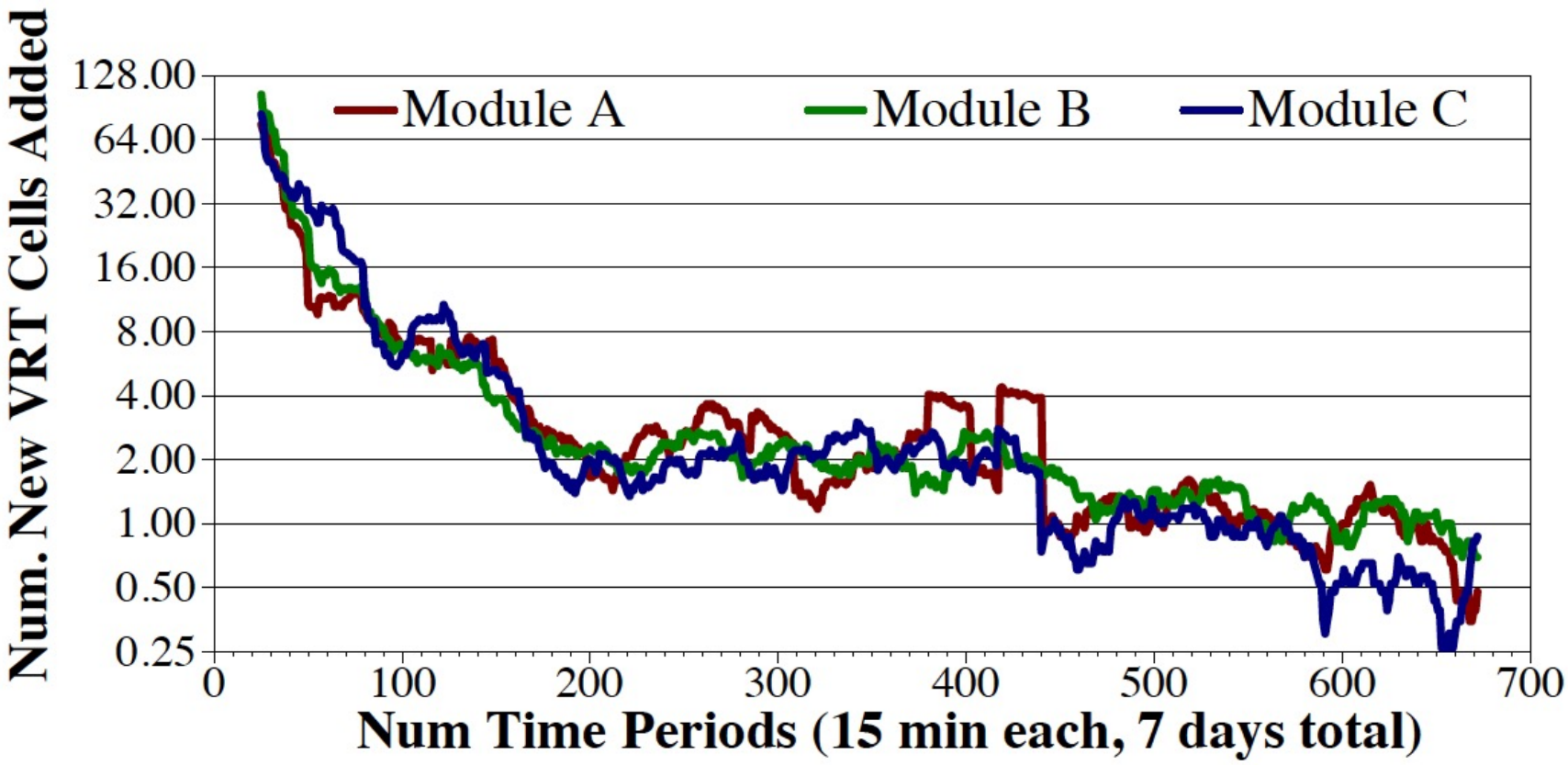


AVP size modeled using lognormal distribution

4: RATE OF NEW VRT CELLS STEADIES

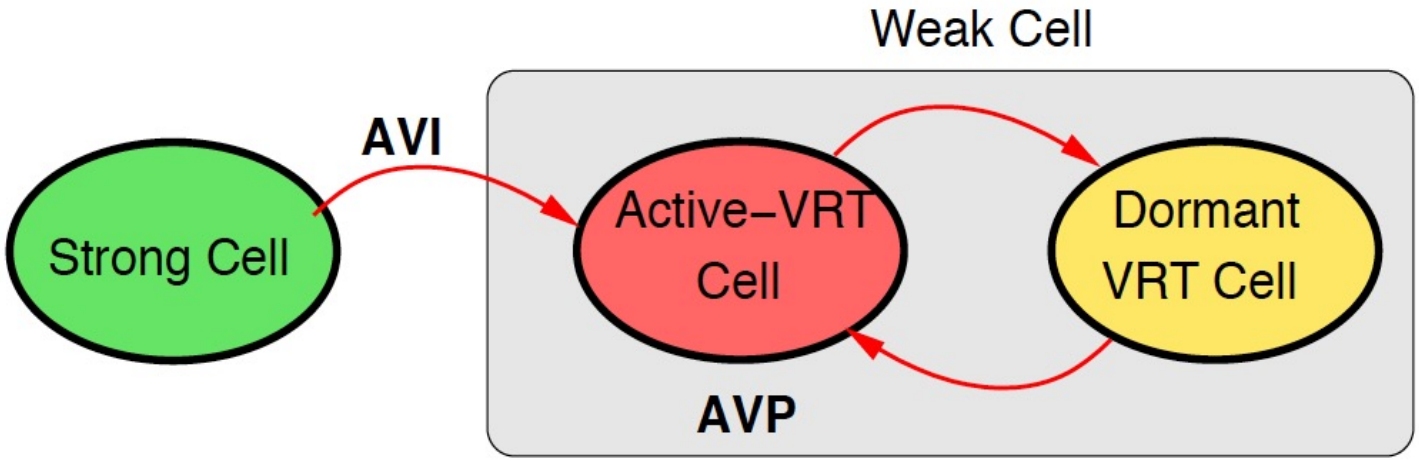
Active-VRT Injection (AVI) Rate

The rate at which new cells become Active-VRT cells



AVP reduces to ~1 new cell per 15-min period

ARCHITECTURE MODEL FOR CELL UNDER VRT



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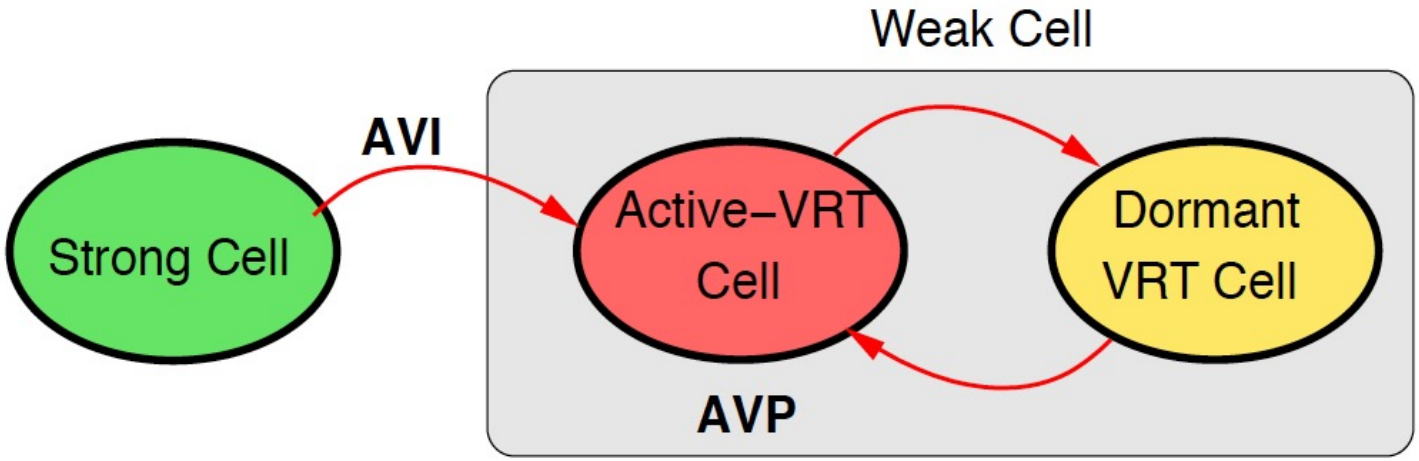

Two key parameters:

Active-VRT Pool (AVP): How many VRT cells in this period?

Active-VRT Injection (AVI): How many new (previously undiscovered) cells became weak in this period?

Model has two parameters: AVP and AVI

ARCHITECTURE MODEL FOR VRT

```
Input: Mu,Sdev, for the logn of Active-VRT pool
Input:  K, rate of discovering new VRT cells
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Insert K new elements in Pool
Remove K elements from Pool
P[TimePeriod] = System Failure Probability
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```

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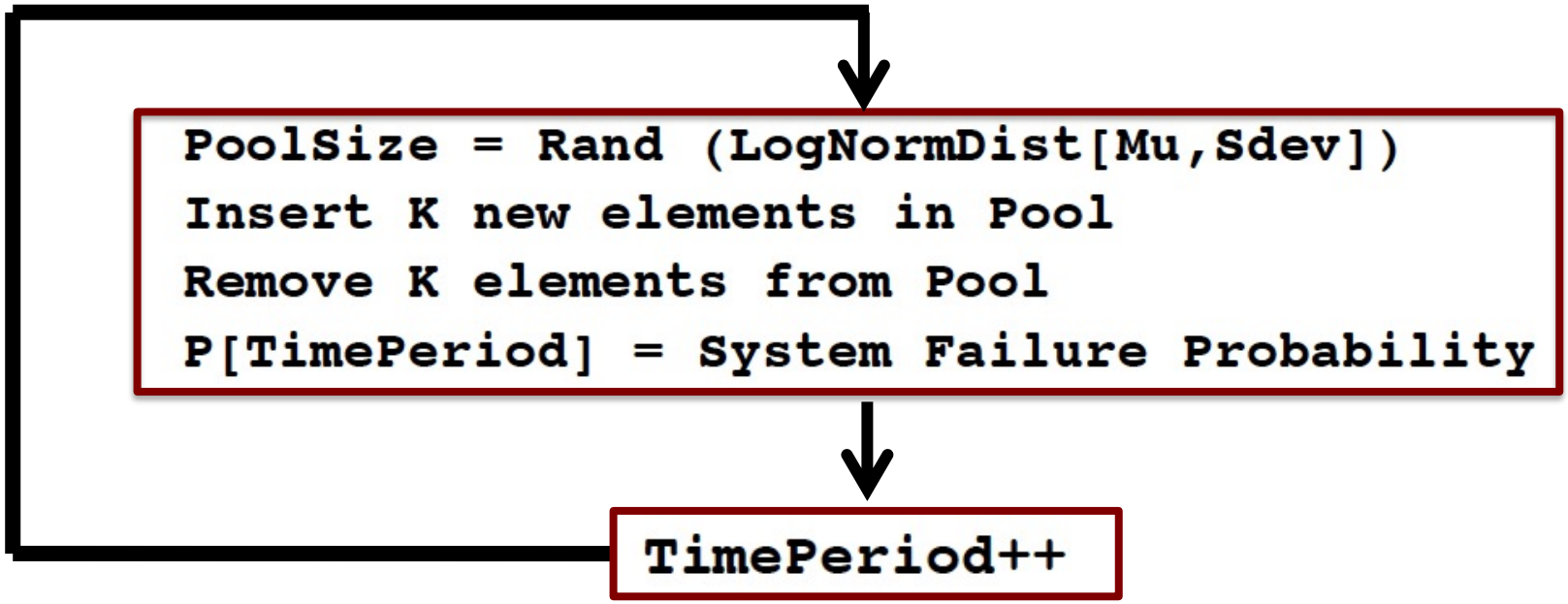

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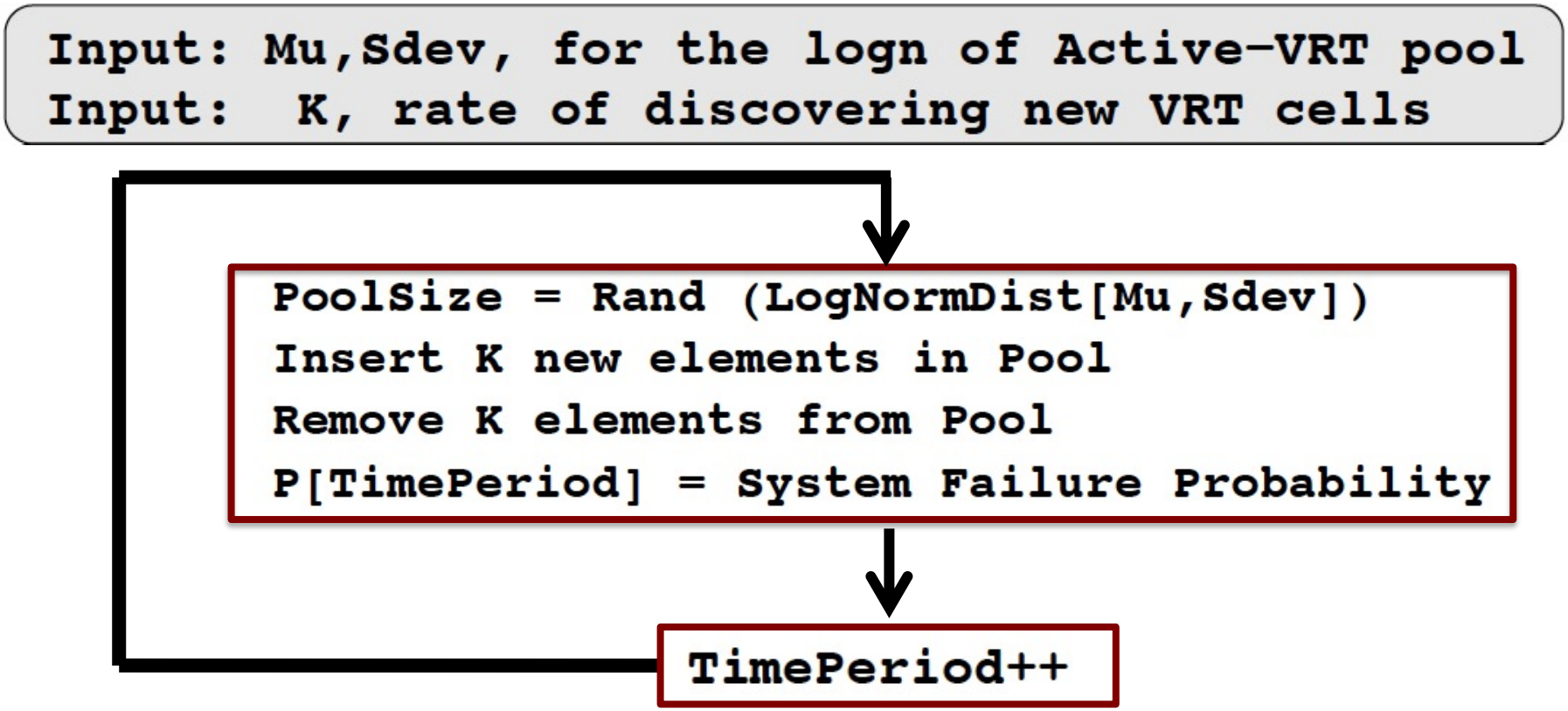

Parameter scaling for larger systems: 2GB DIMM to 8GB DIMM
AVP size increased by 4x: from ~400 to ~1600
AVI rate increased by 4x: from 1 to 4

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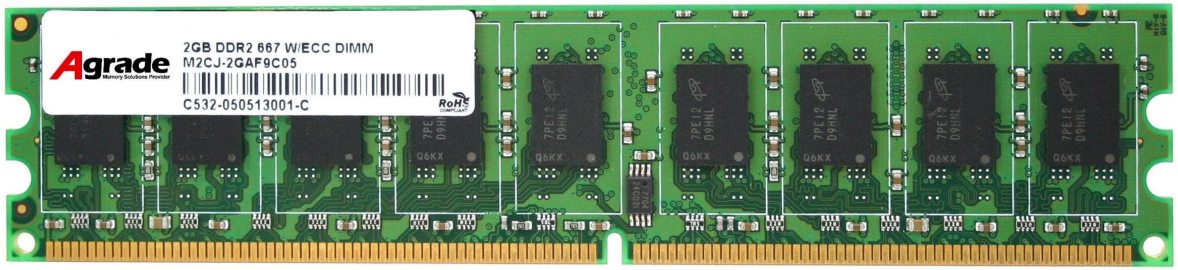
BACKGROUND ON ECC DIMM

ECC DIMM can tolerate 1 error per word (8 bytes)



Typically used to tolerate soft error but can also be used to fix a bit error due to VRT

A multi-bit error per word ➔ uncorrectable error

What is time to double error per word under VRT?

ANALYTICAL MODEL FOR ECC DIMM

W words in memory (strong rows only)

P words have 1 bit error already (AVP)

K new weak cells get injected in given time quanta

$$P(DIMM\ has\ no\ uncorrectable\ error) = (1 - \frac{\mathcal{P}}{W})^K$$

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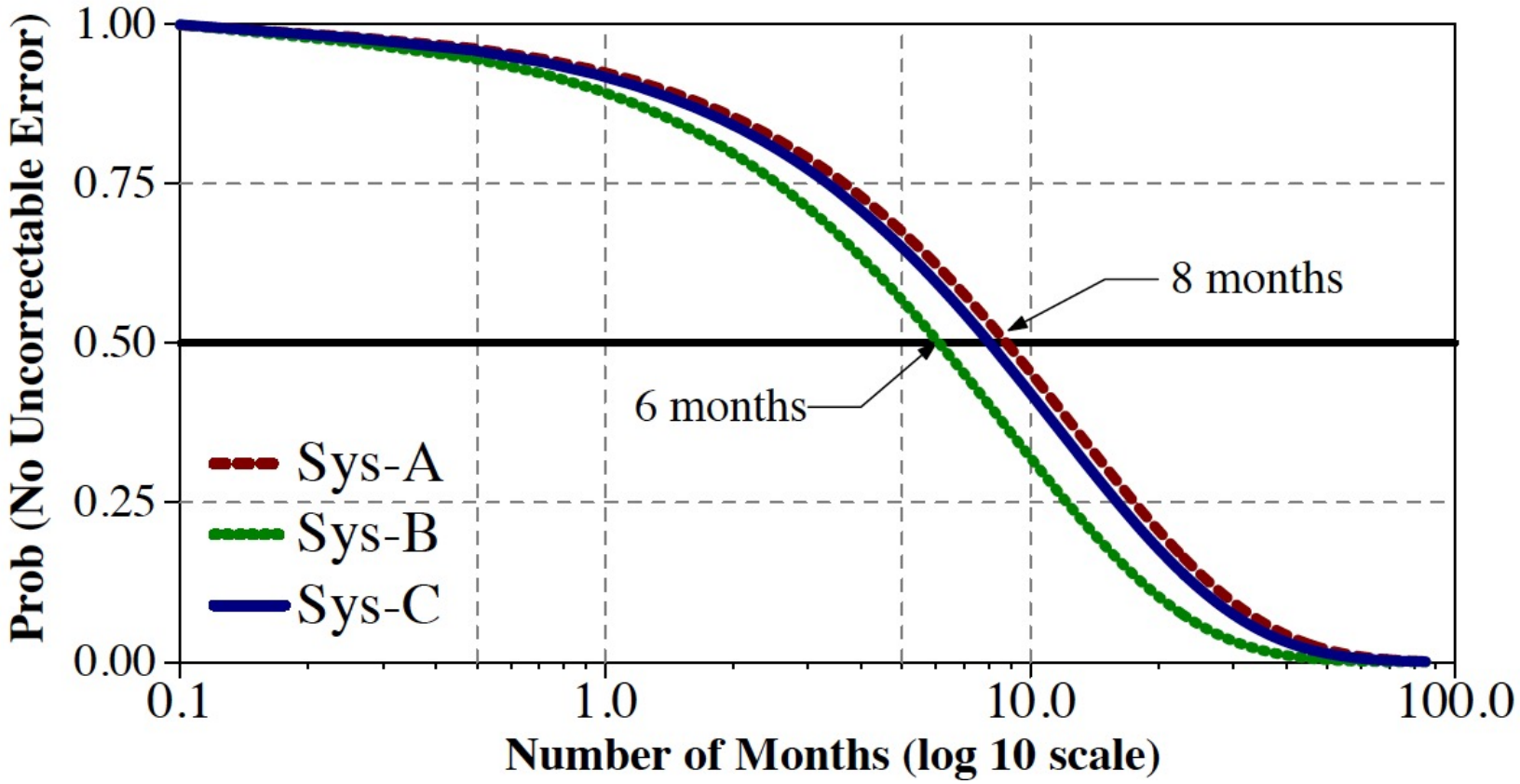
$$P(System\ has\ no\ uncorrectable\ error) = (1 - \frac{\mathcal{P}}{W})^{K \cdot T \cdot D}$$

EVEN WITH ECC-DIMM, ERROR RATE IS HIGH

System: Four channels, each with 8GB DIMM



VRT still causes an error every ~6-8 months

OUTLINE

- Background
- VRT: mechanism, measurement, model
- Can't we fix VRT by simply using ECC DIMM?

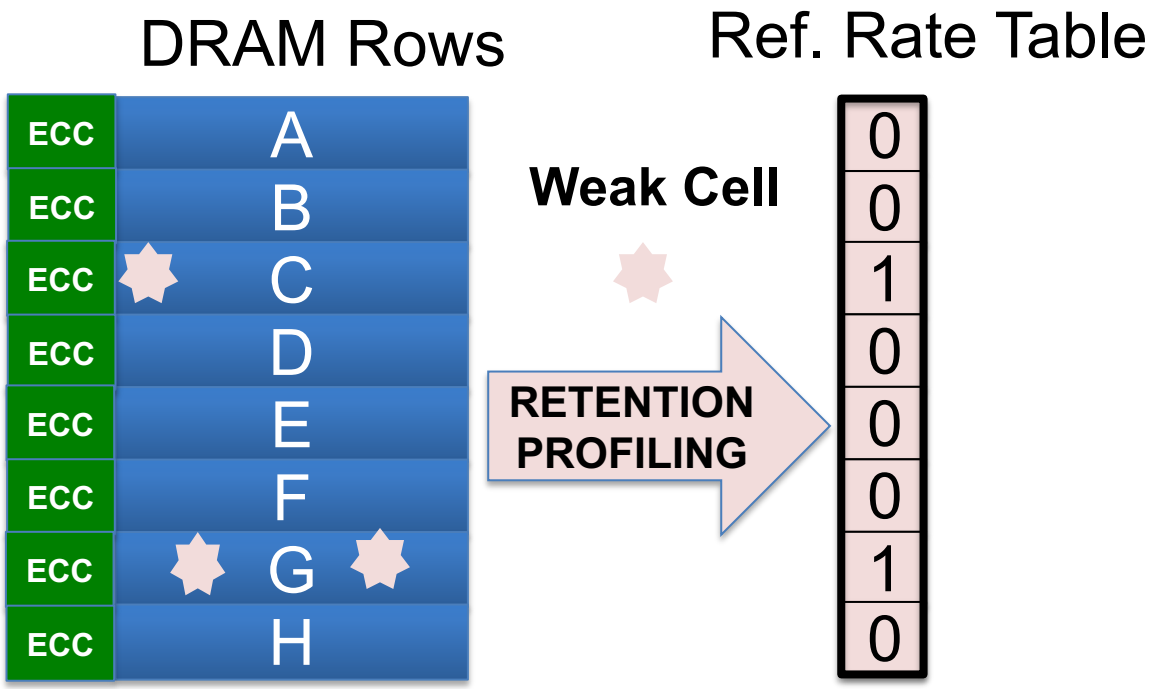
- AVATAR

- Results
- Summary

AVATAR

Insight: Avoid forming Active VRT Pool ➔ Upgrade on ECC error

Observation: Rate of VRT >> Rate of soft error (50x-2500x)



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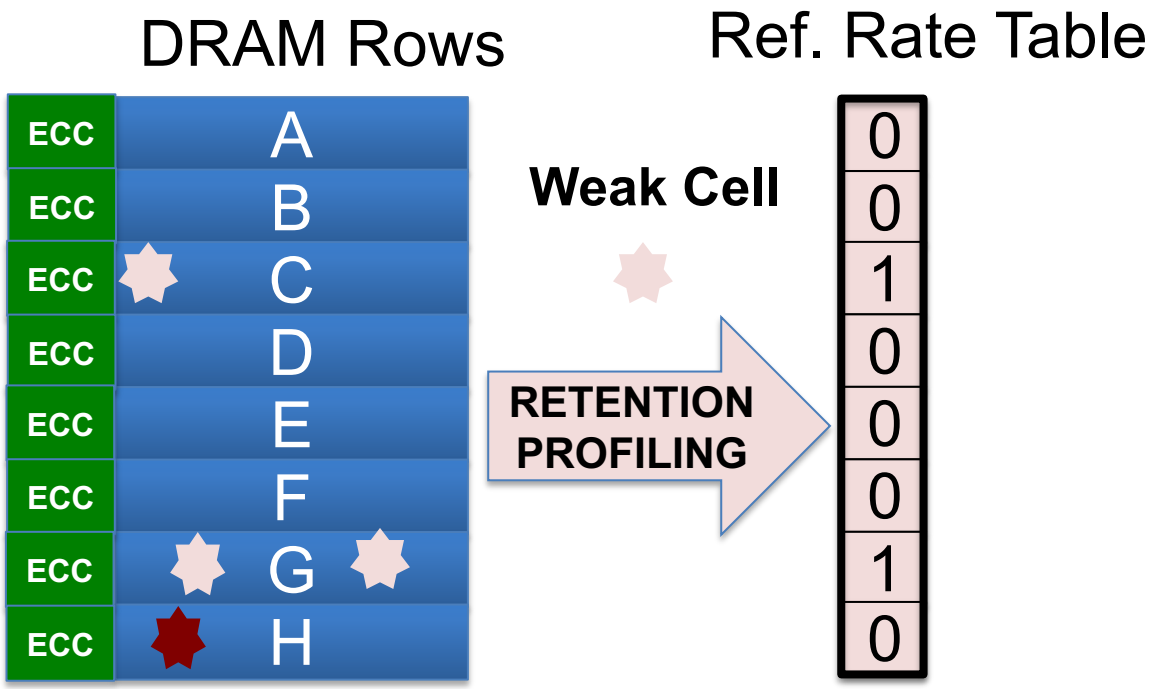

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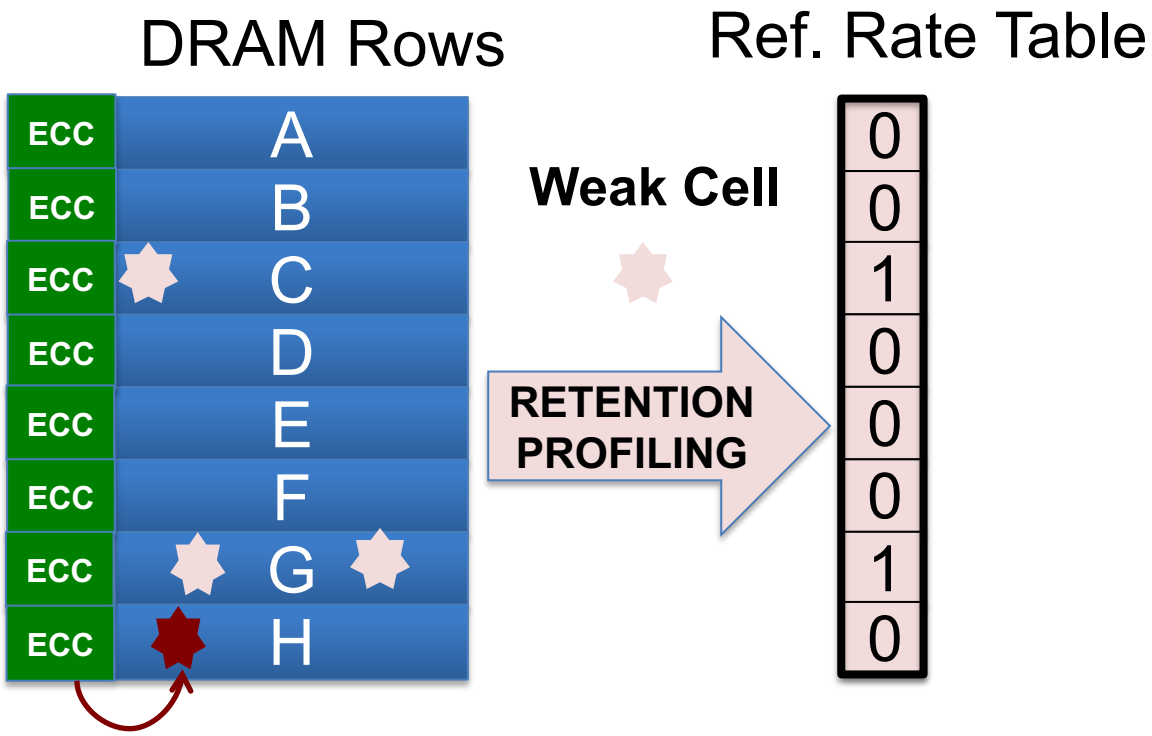

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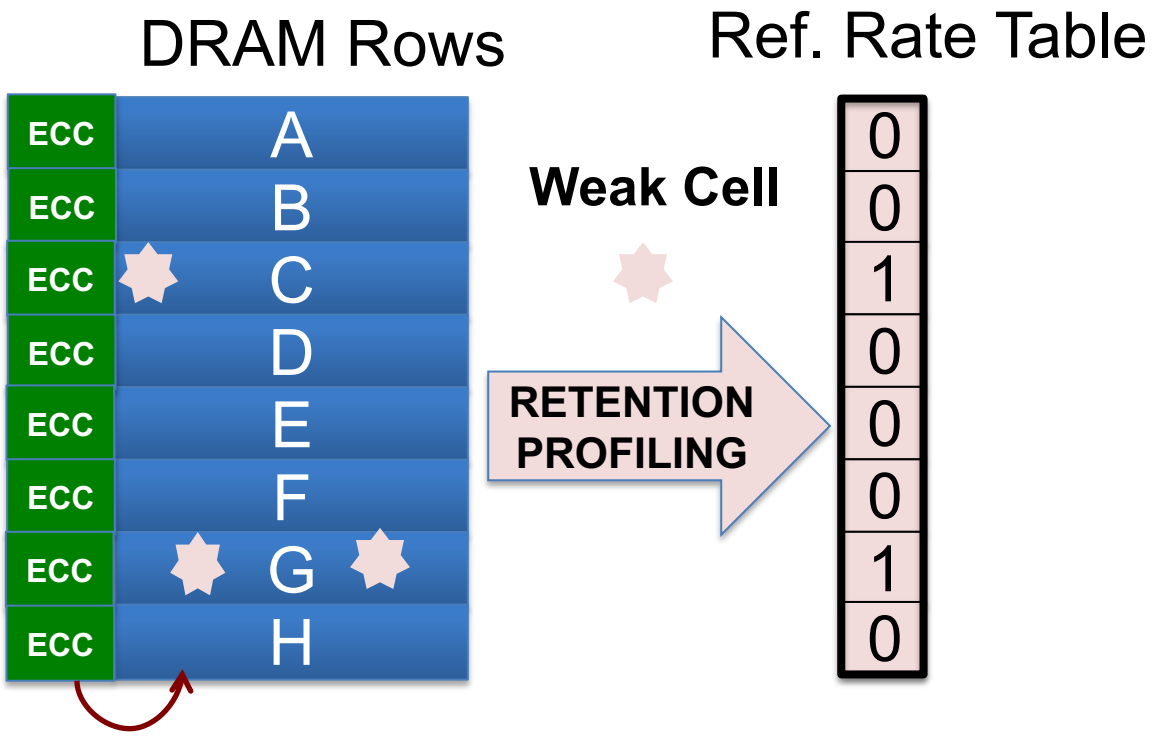

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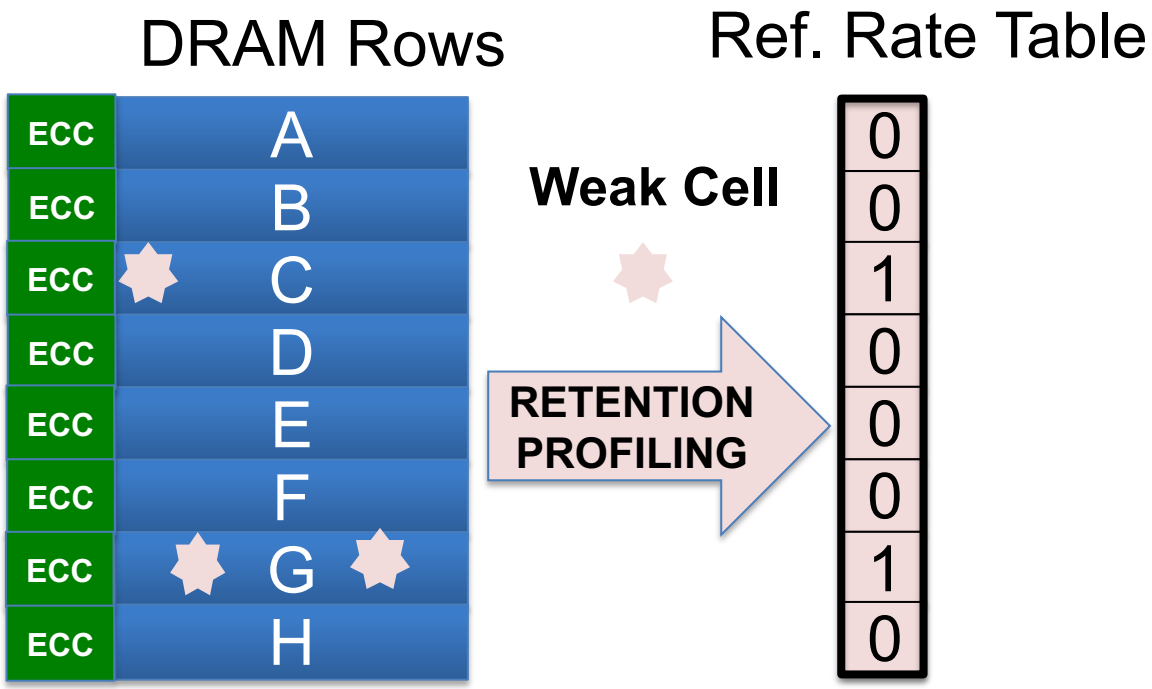

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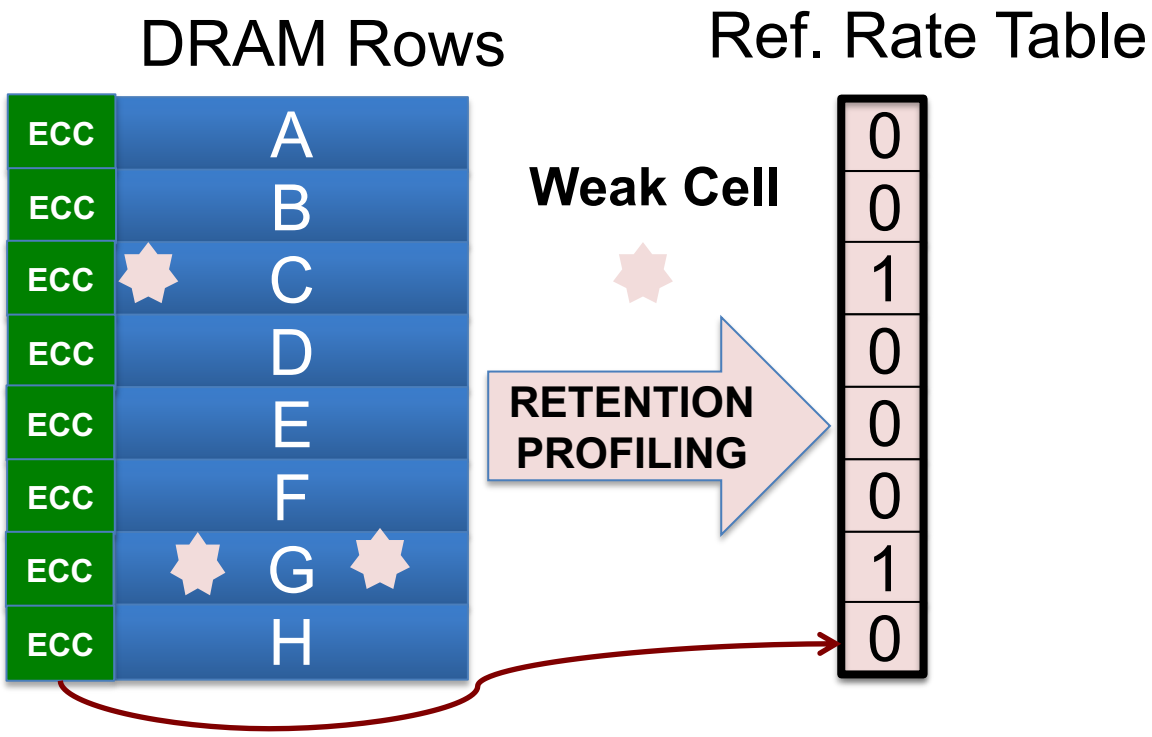

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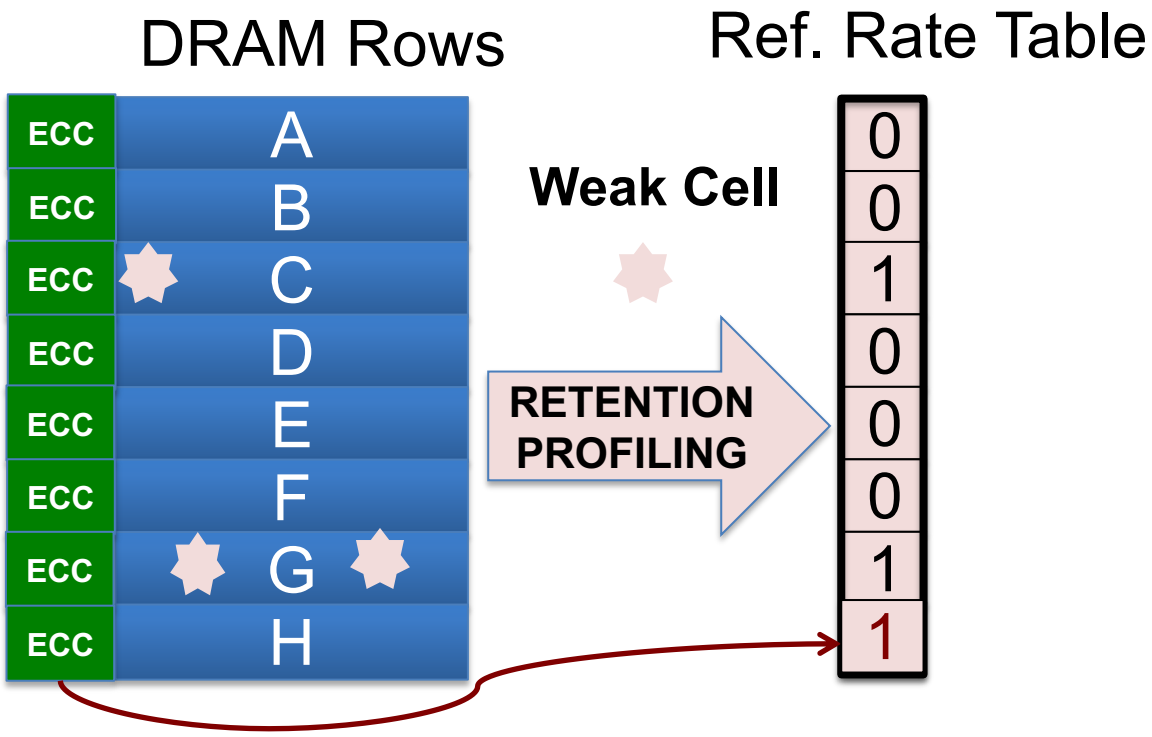

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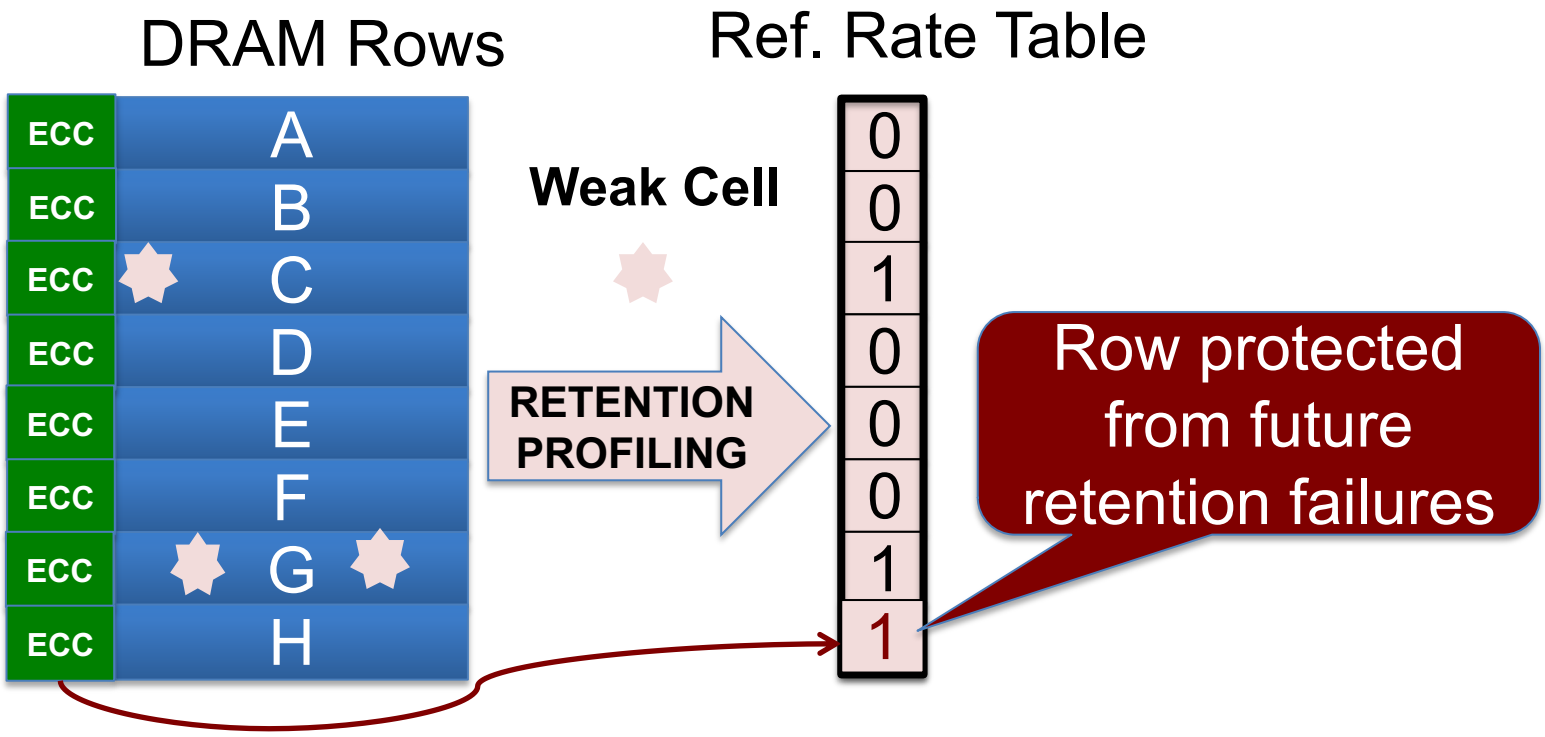

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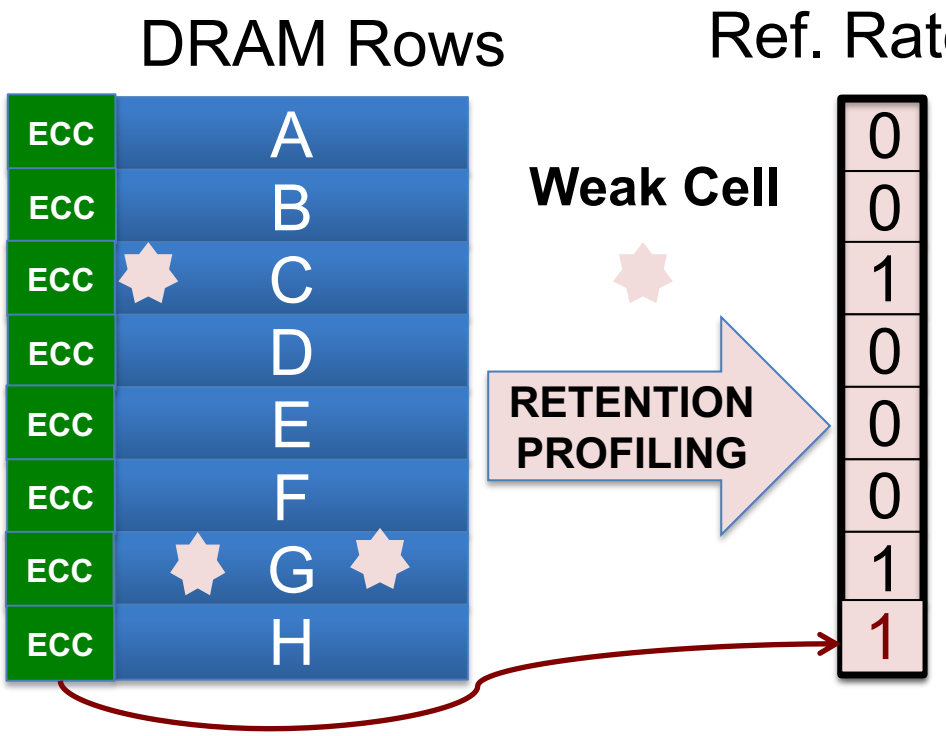

AVATAR mitigates VRT by breaking AVP Pool

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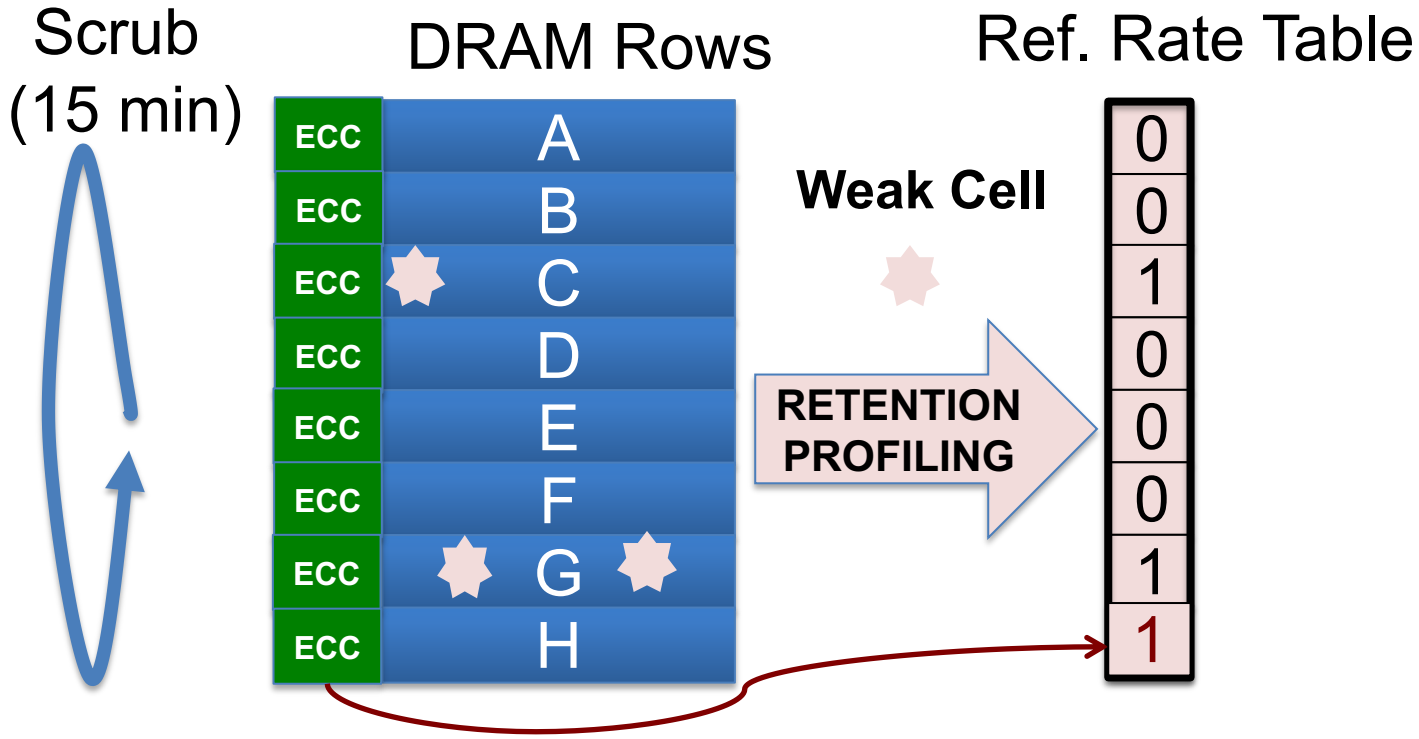

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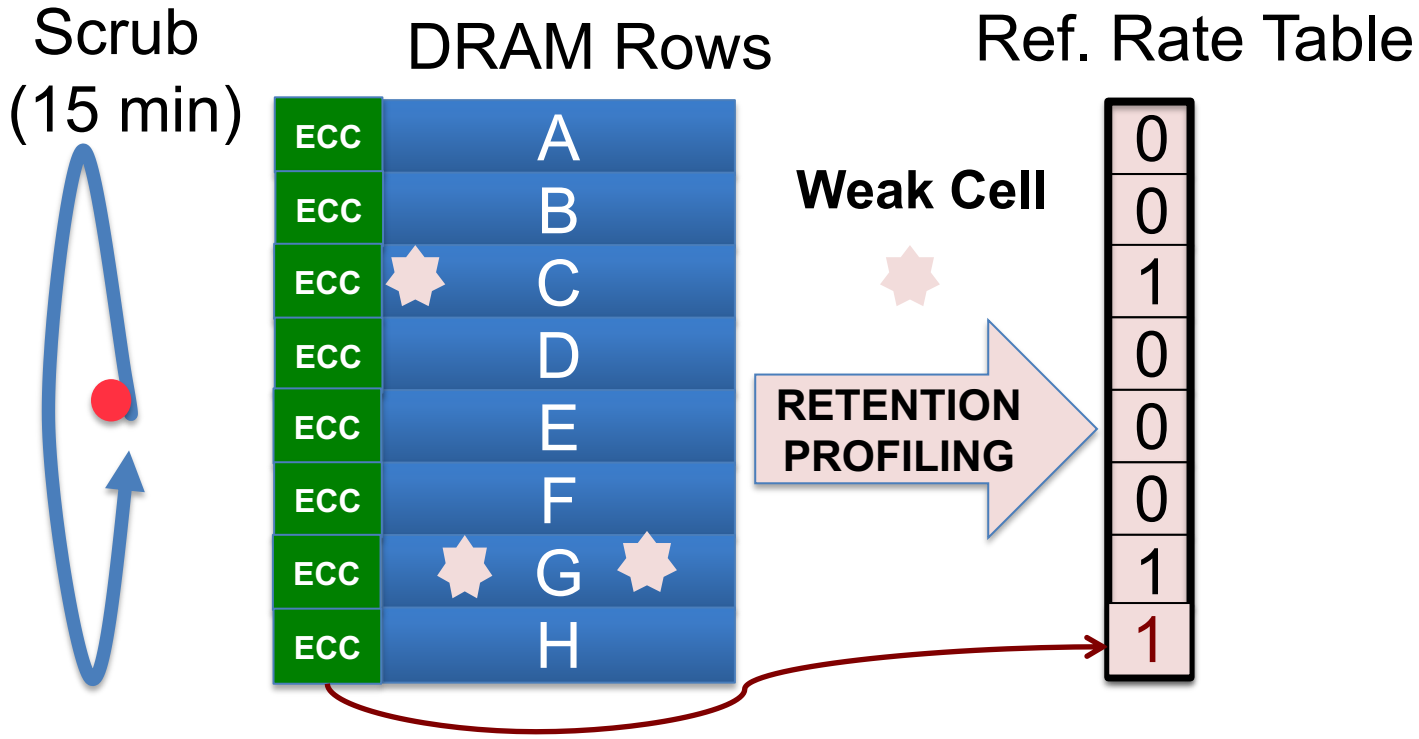

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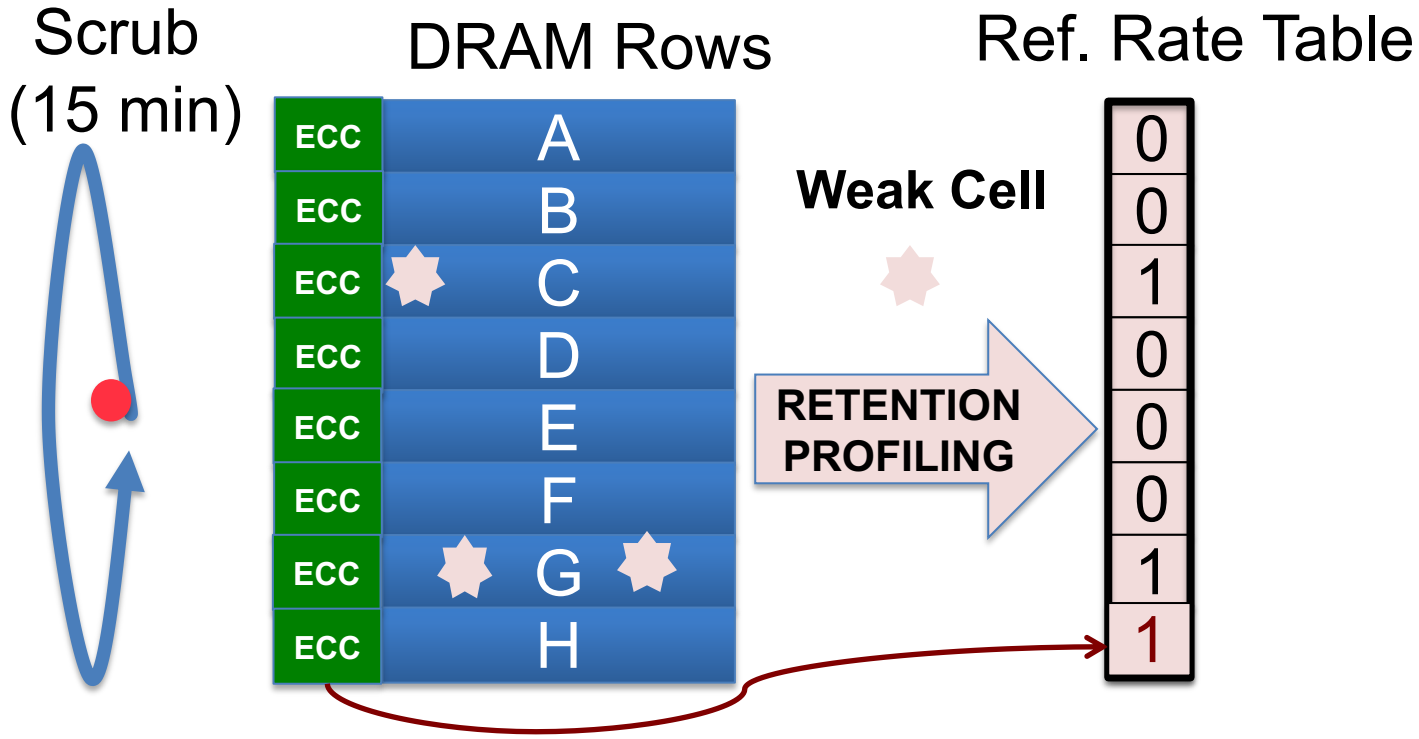

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AVATAR: TIME TO FAILURE

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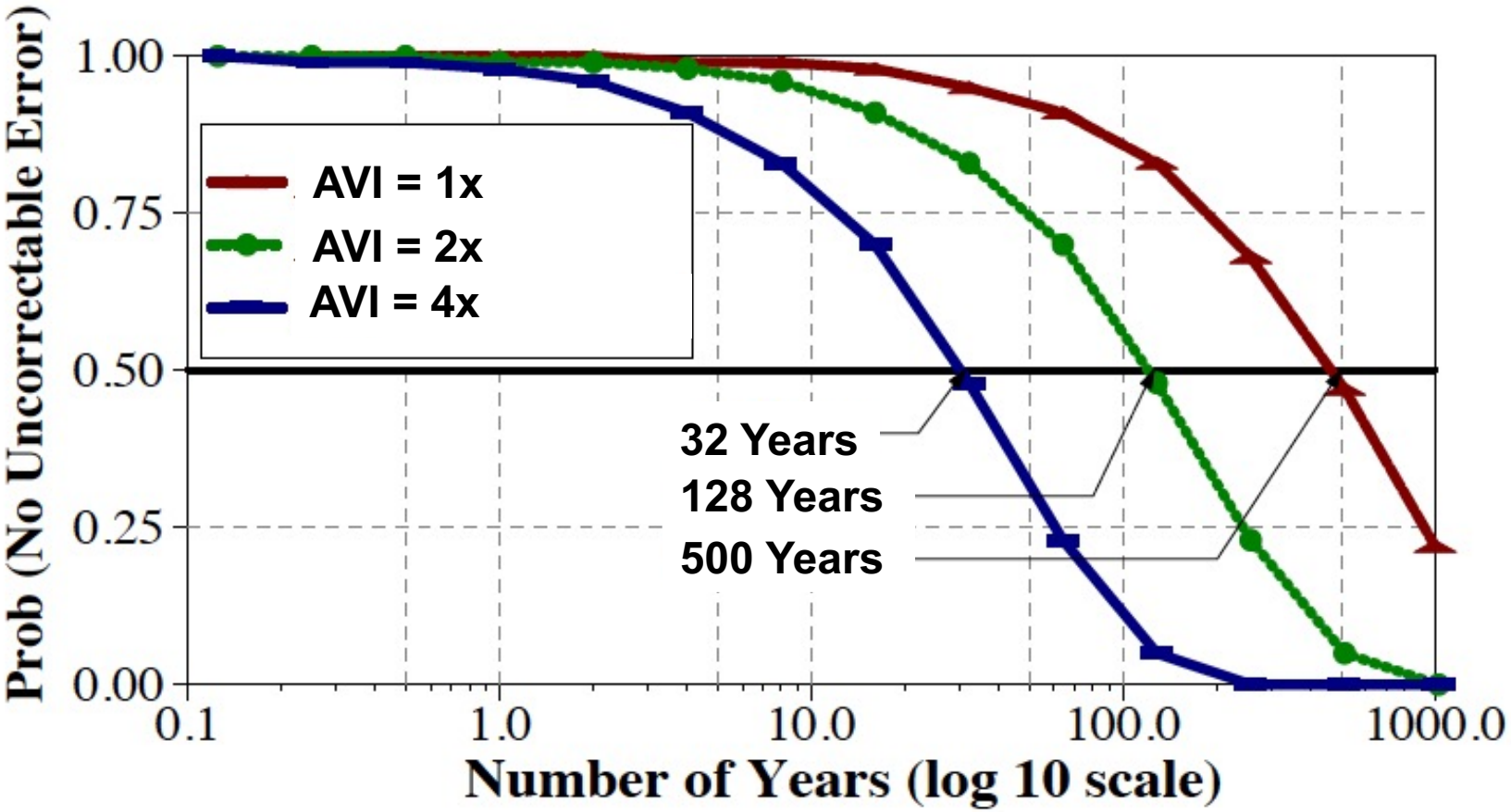

* We include the effect of soft error in the above lifetime analysis (details in the paper)

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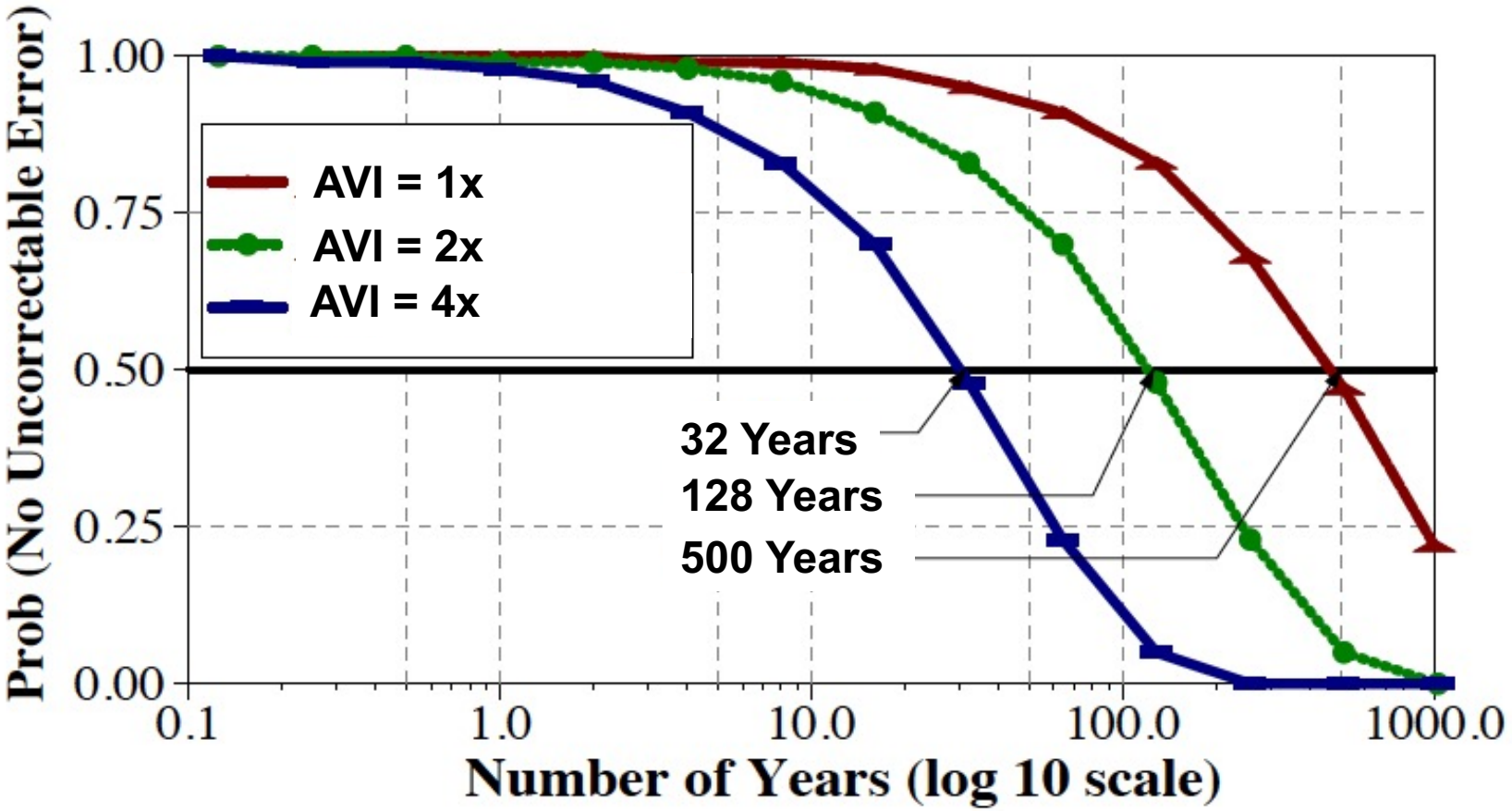

AVATAR increases time to failure to 10s of years

* We include the effect of soft error in the above lifetime analysis (details in the paper)

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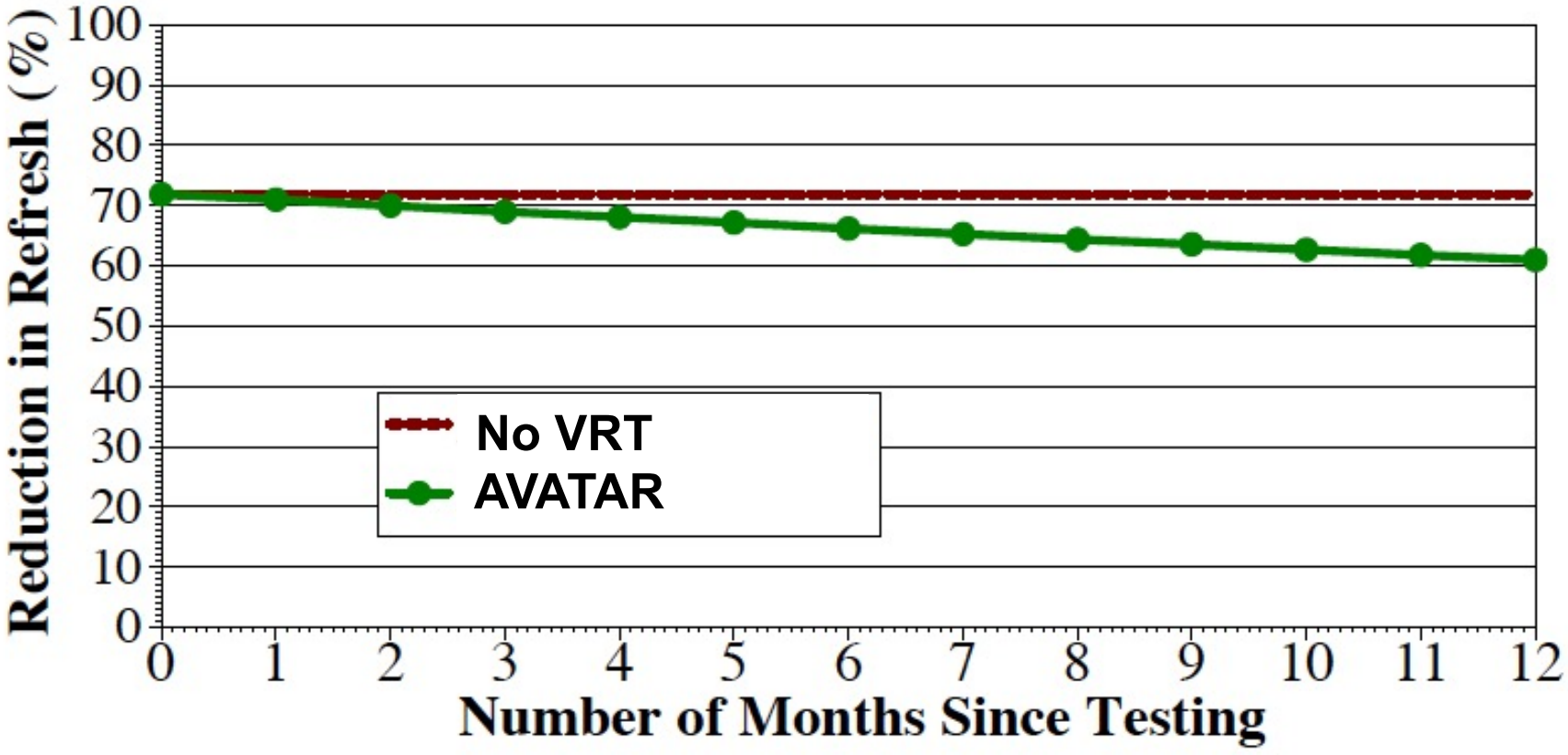
RESULTS: REFRESH SAVINGS



AVATAR reduces refresh by 60%-70%, similar to multi rate refresh but with VRT tolerance

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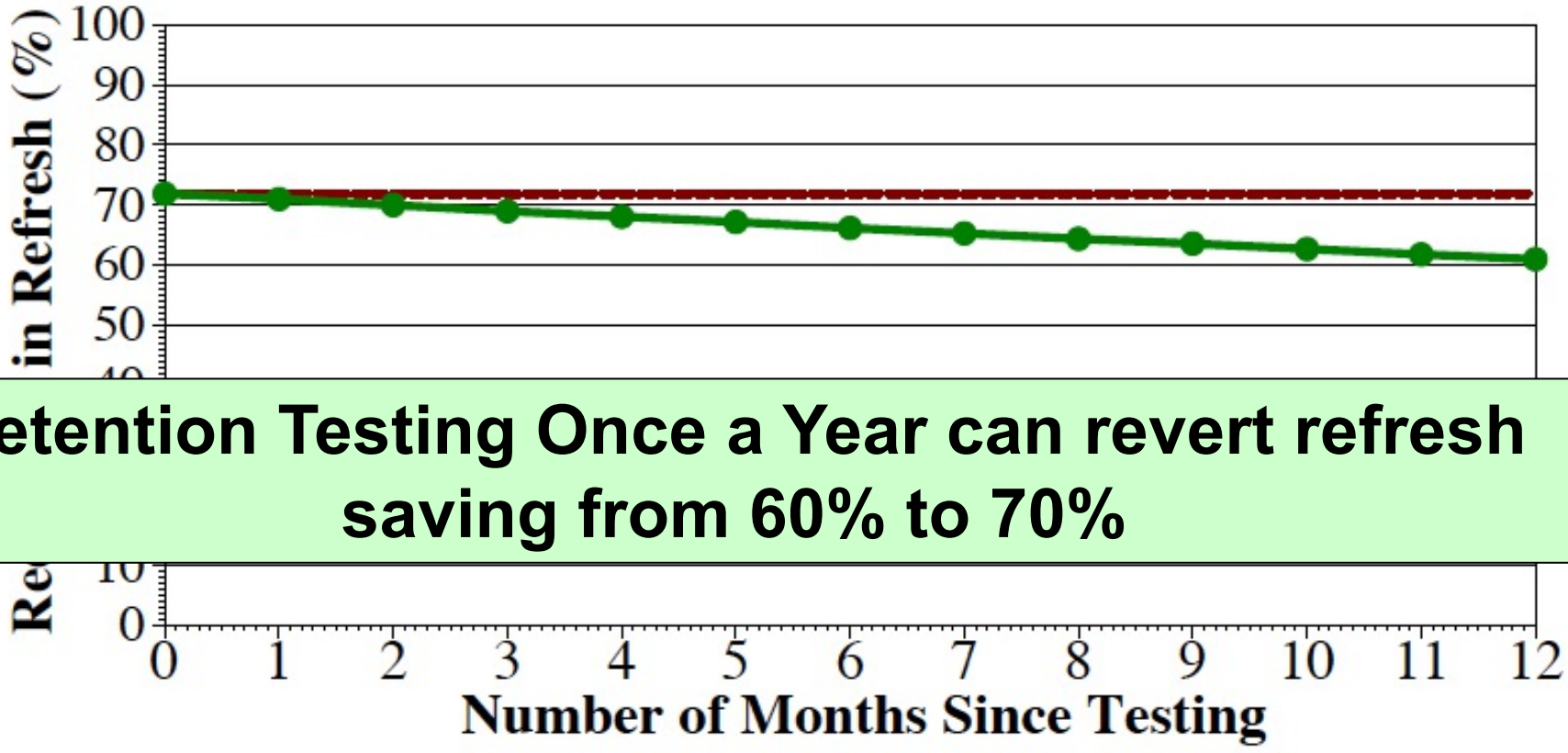
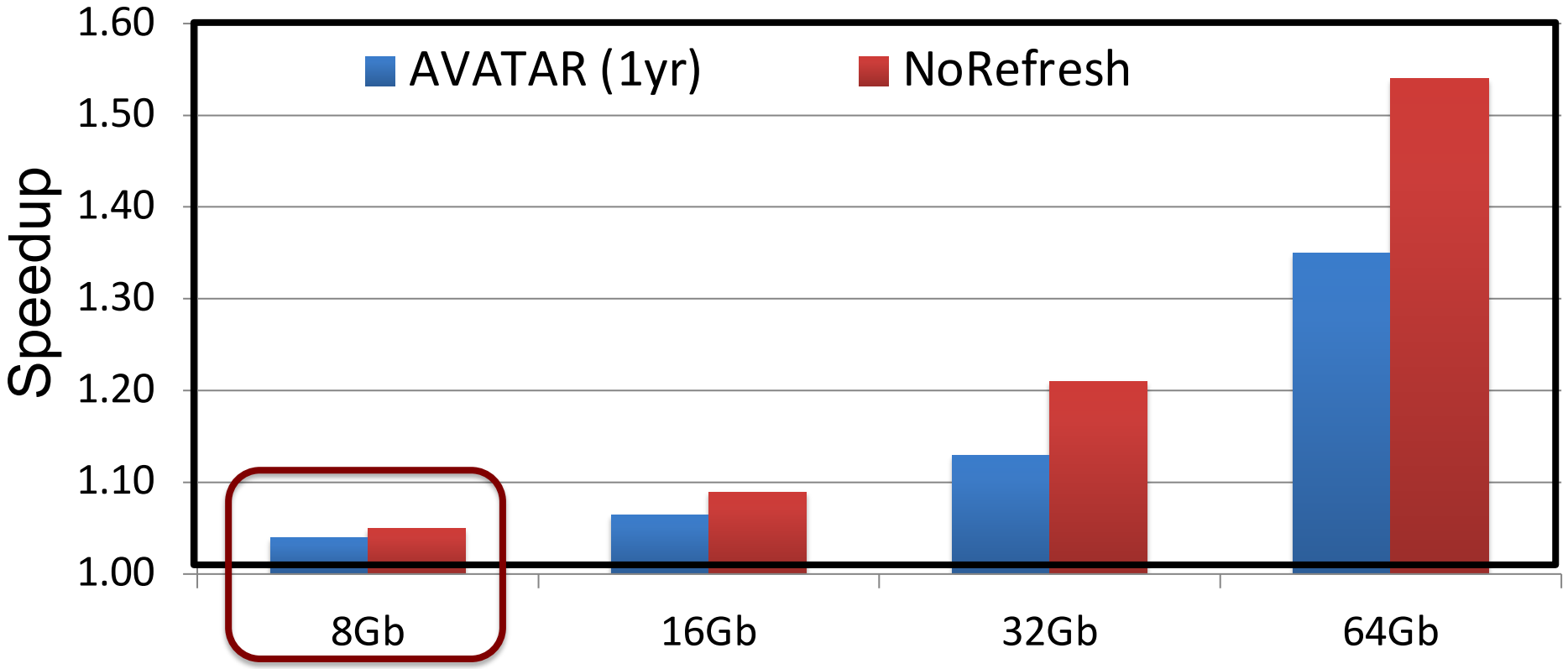


Retention Testing Once a Year can revert refresh saving from 60% to 70%

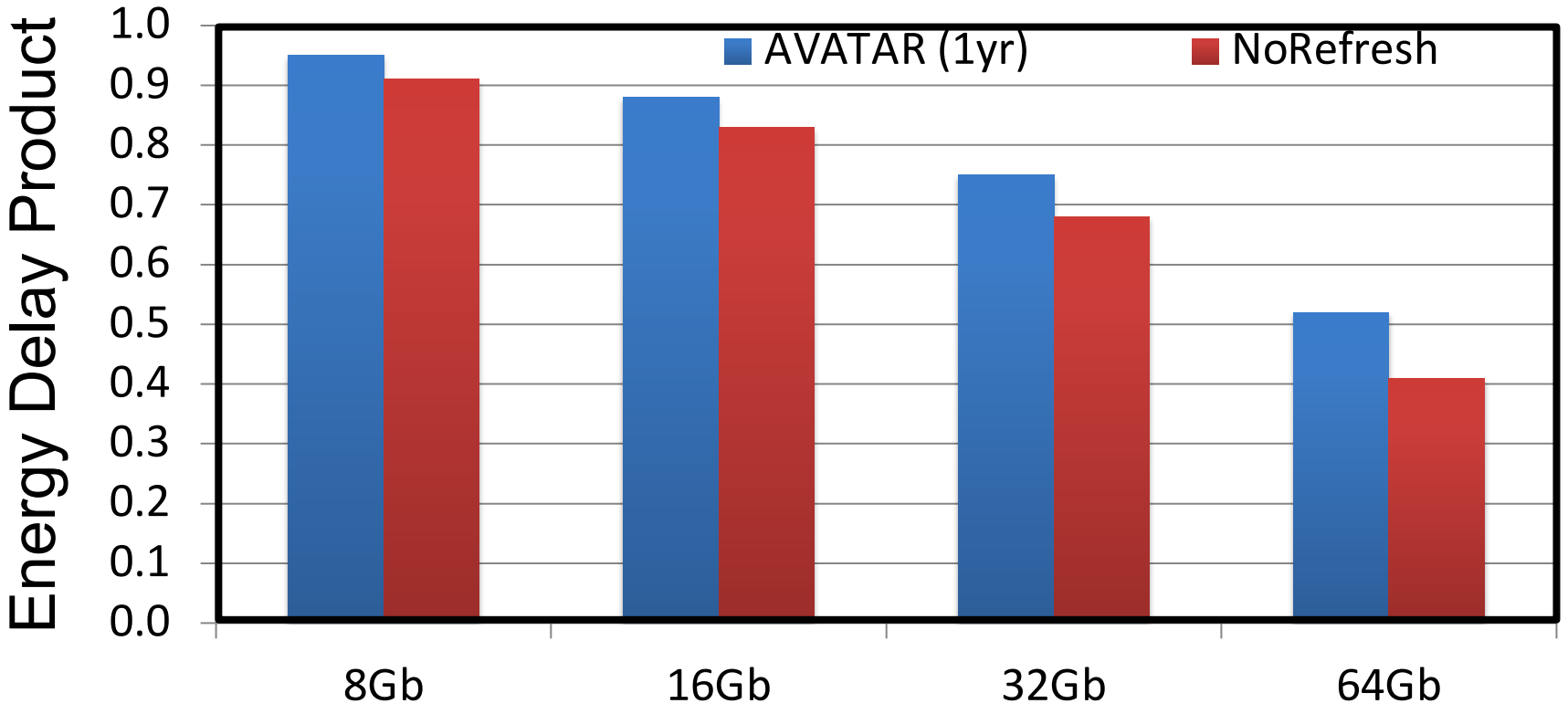
AVATAR reduces refresh by 60%-70%, similar to multi rate refresh but with VRT tolerance

SPEEDUP



AVATAR gets 2/3rd the performance of NoRefresh. More gains at higher capacity nodes

ENERGY DELAY PRODUCT



AVATAR reduces EDP,
Significant reduction at higher capacity nodes

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SUMMARY

Multirate refresh ➔ retention profiling to reduce refresh

Variable Retention Time ➔ errors with multirate refresh

✓Architecture model of VRT based on experiments
✓We show ECC DIMM alone is not enough
✓AVATAR (upgrade refresh rate of row on ECC error)

AVATAR increase the time to failure from 0.5 years to 500 years and incurs the same storage as ECC DIMM