SYNERGY: Rethinking Secure-Memory Design for Error-Correcting Memories

HPCA-2018

Vienna, Austria

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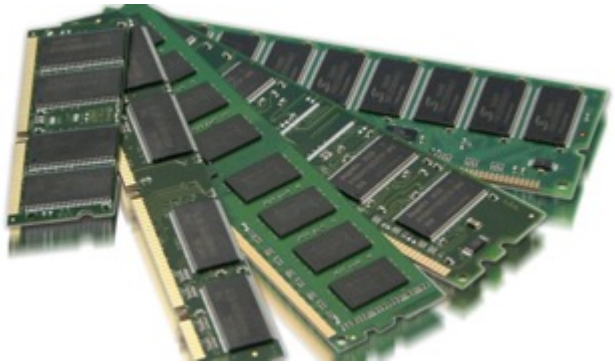
Prashant Nair[1] Prakash Ramrakhyani[2] Wendy Elsasser[2] Moinuddin Qureshi[1]

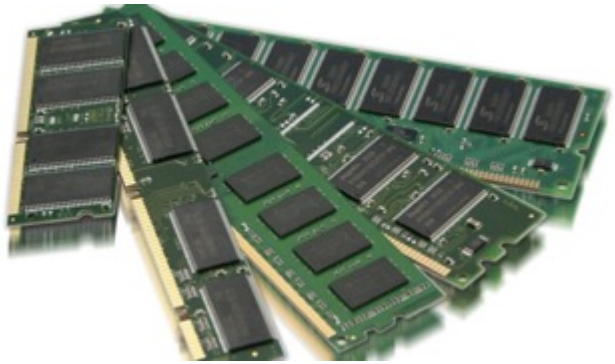
[1] Georgia Tech [2] arm Research

Designing Resilient Memories for Servers



Server memories need protection against **data corruption**

Designing Resilient Memories for Servers



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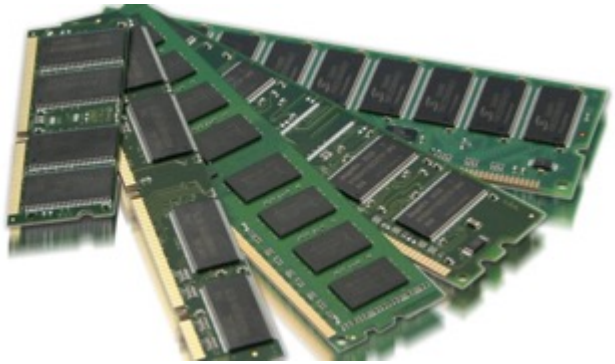

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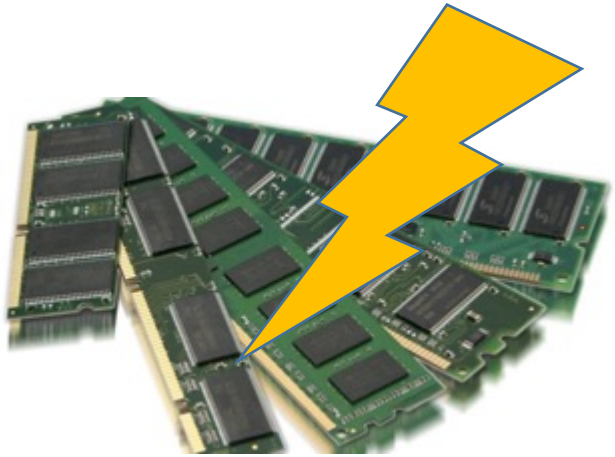

Server memories need protection against **data corruption**

by Malicious ***Attacks***

by Natural ***Errors***

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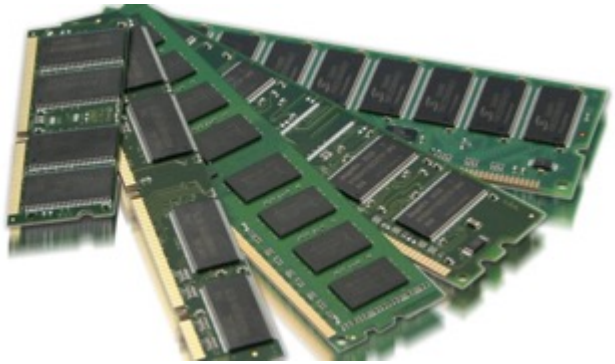
Resilient Memories



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Security

Reliability

by Malicious ***Attacks***

by Natural ***Errors***

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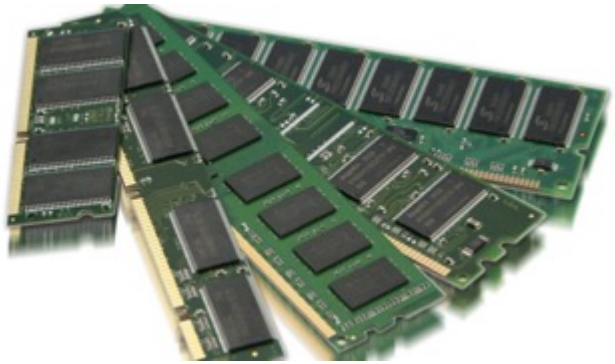

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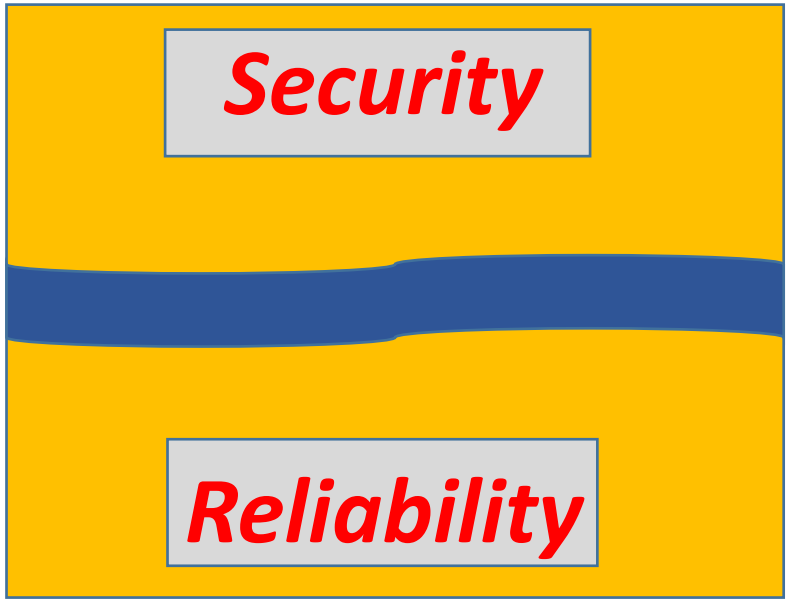

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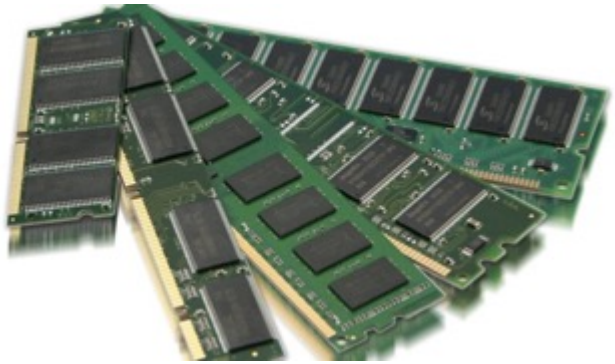

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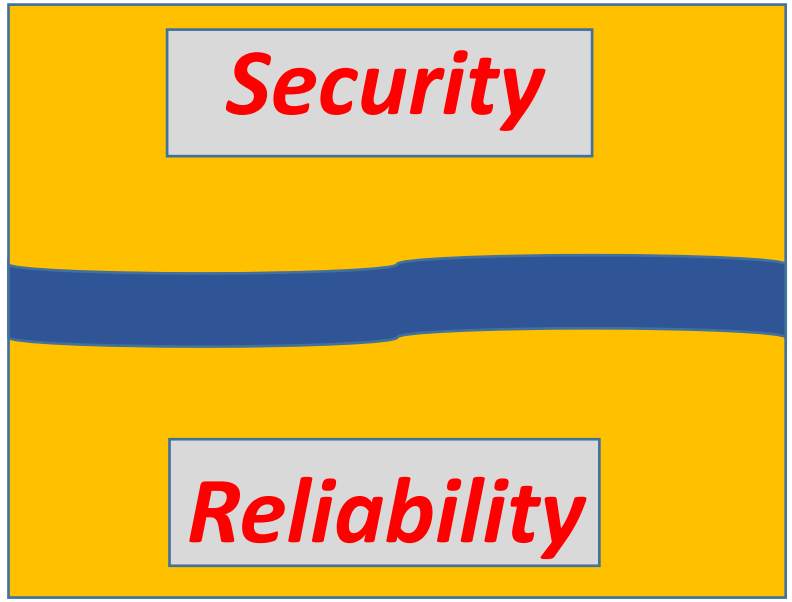

Attack Resilience – *Memory Security*

intel ***SGX***

(Software Guard Extensions)

Designing Resilient Memories for Servers

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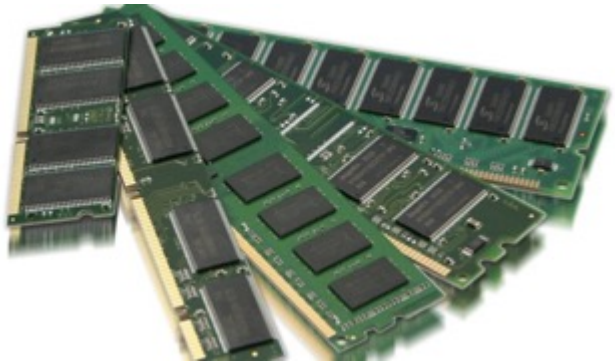

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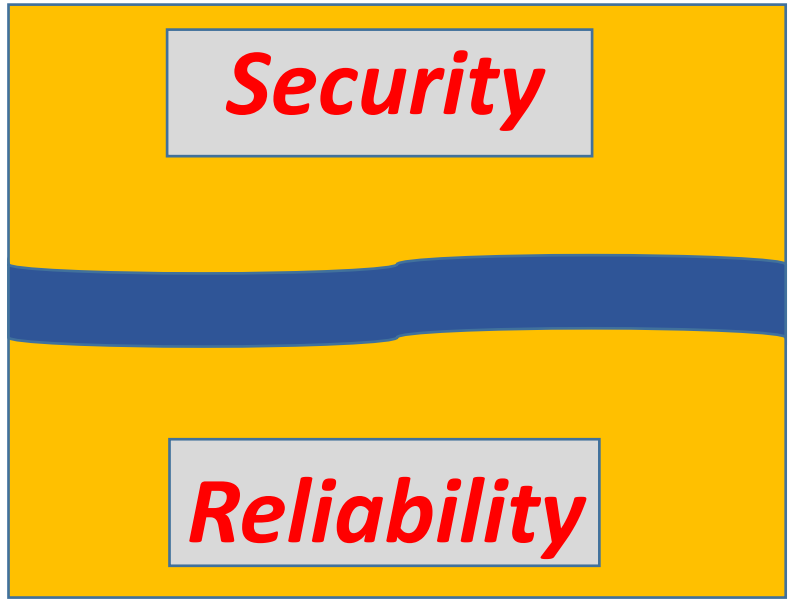

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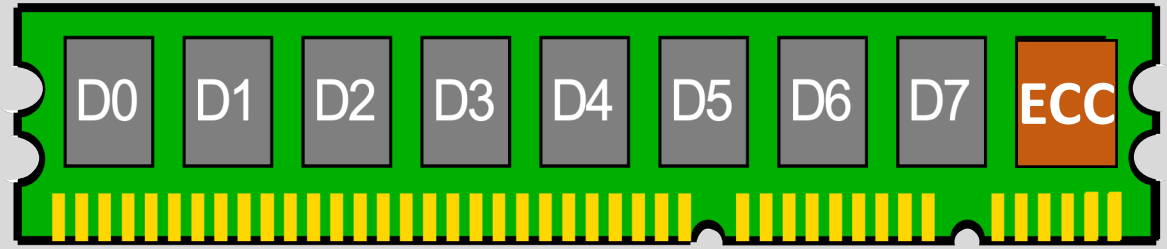
Error Resilience – *ECC-DIMM*



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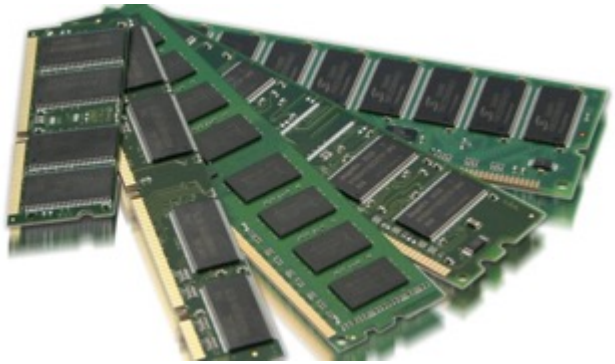

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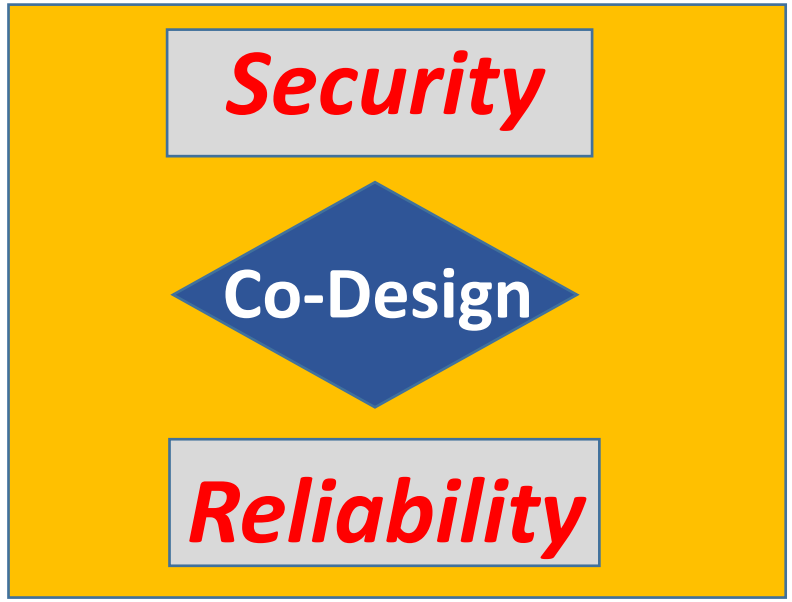
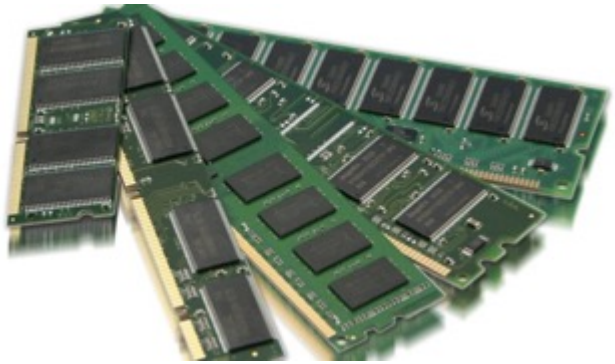


SYNERGY

Co-Design of Security-Reliability

Designing Resilient Memories for Servers

Resilient Memories



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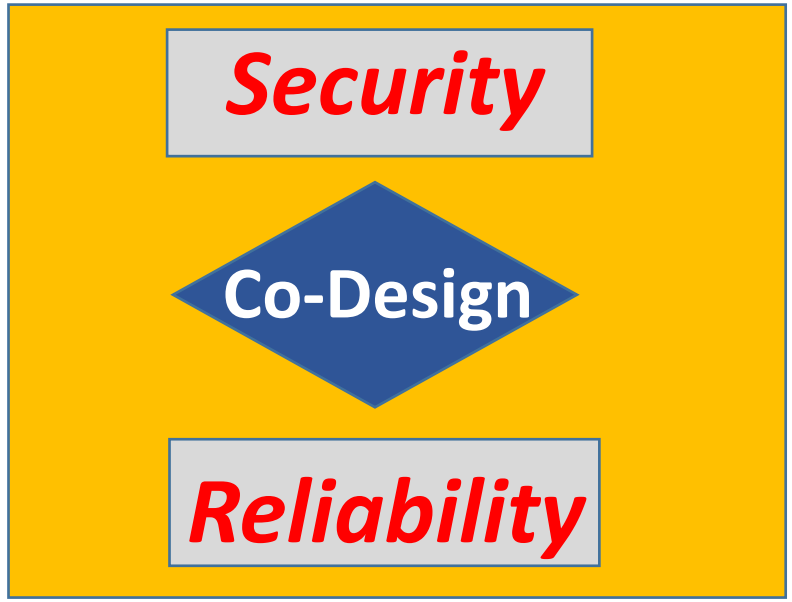

SYNERGY

Co-Design of Security-Reliability

- *Better* **Performance – *20%***
- *Better* **Reliability – *185X***
- *Maintaining* **Security**
- *No Extra* **Storage**

Threat Model for Memory Modules

Unauthorized Reads

Unauthorized Writes

Replay Attack

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Cold Boot Attack

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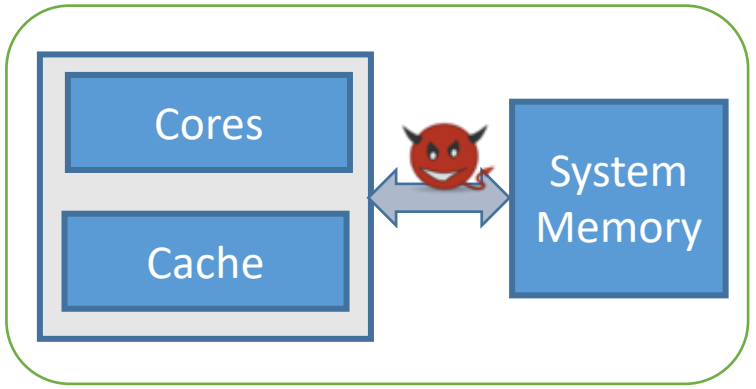

Man-in-the-middle Attack

Threat Model for Memory Modules

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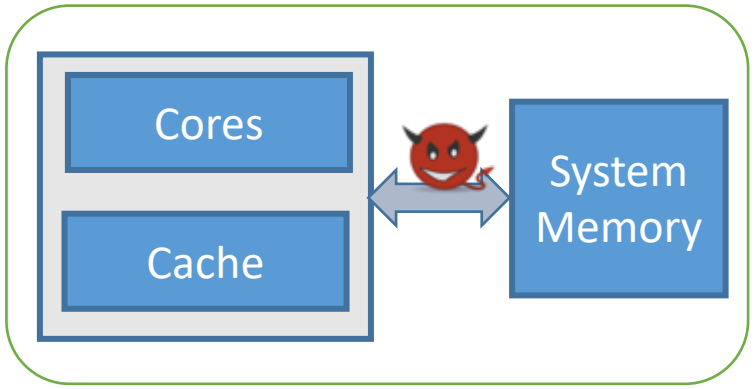

Man-in-the-middle Attack

Secure memory needs to protect against these attacks !

How Do Secure Memories Work ?

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Replay Attack

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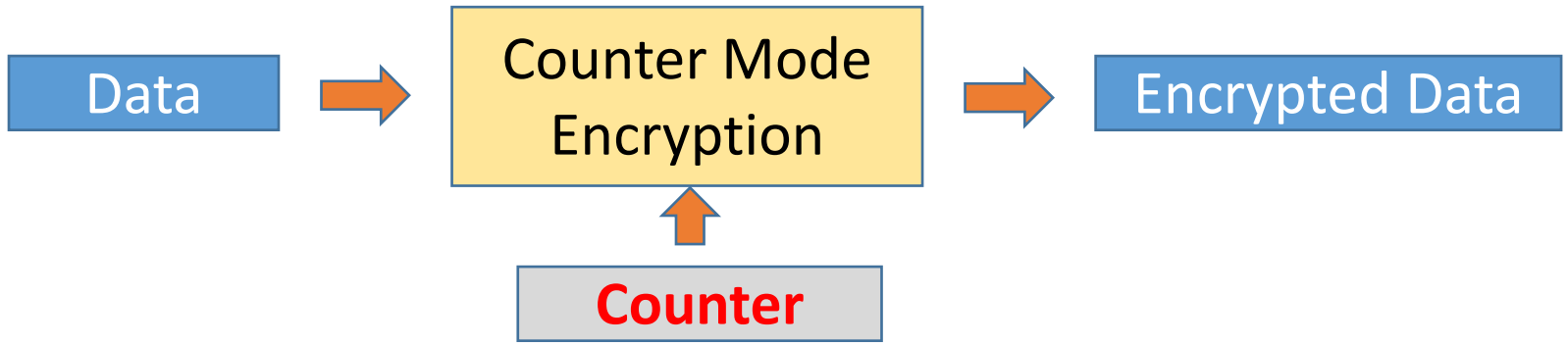

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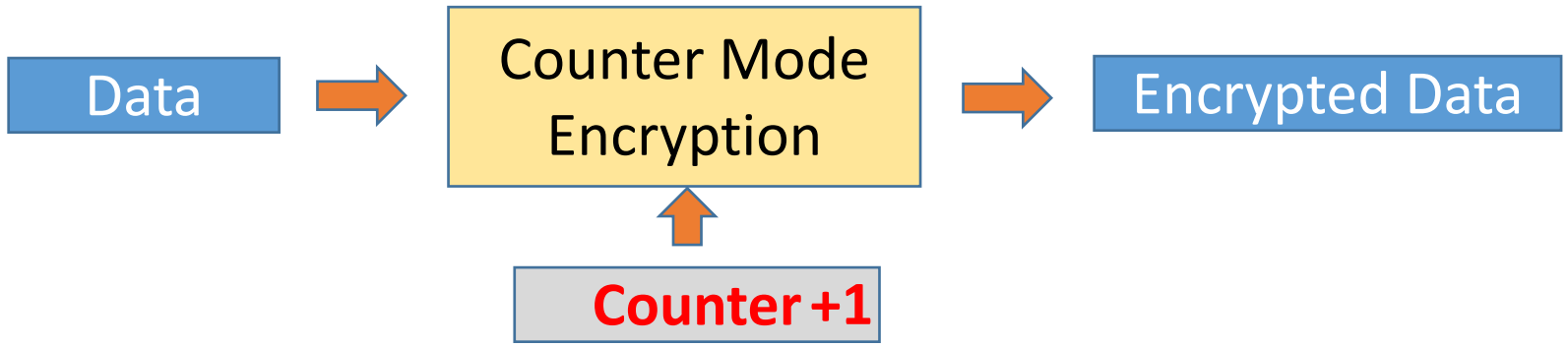

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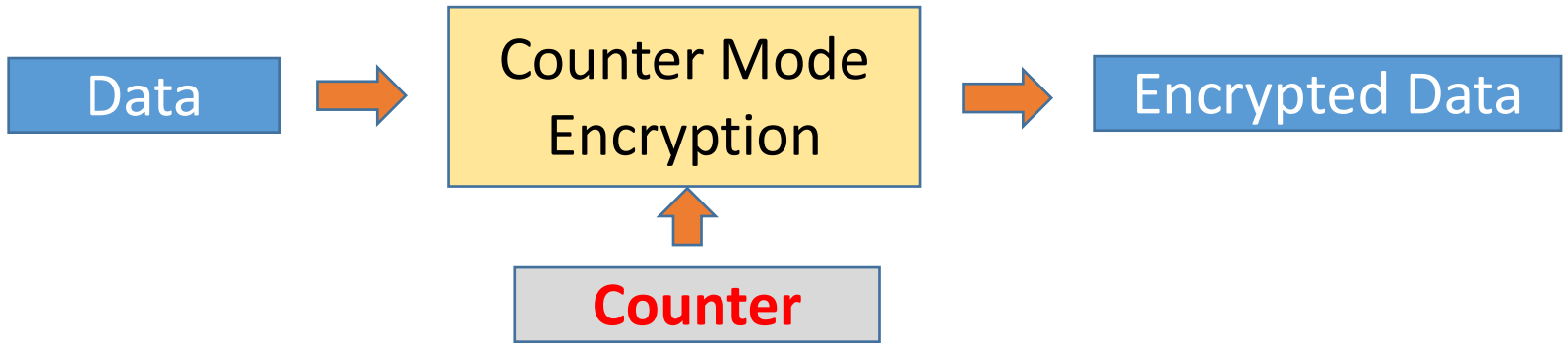

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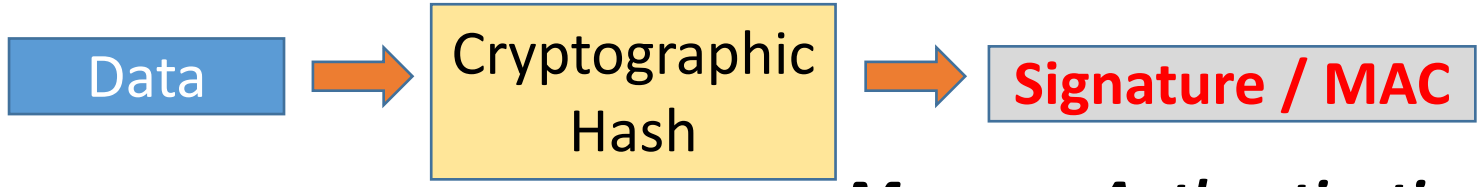

Message Authentication Code

Replay Attack

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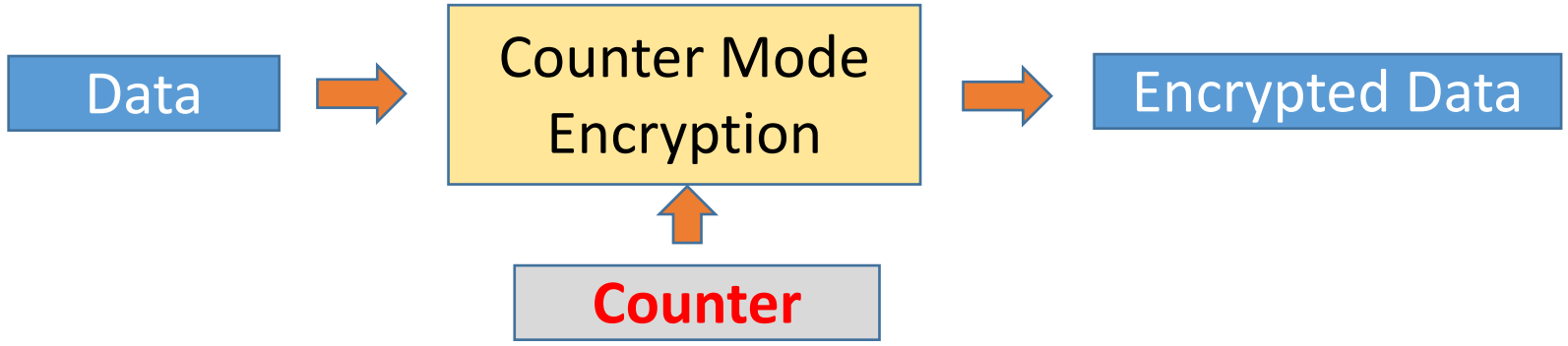

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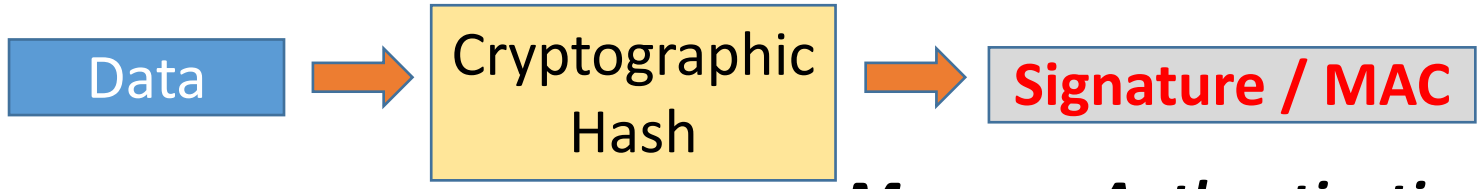

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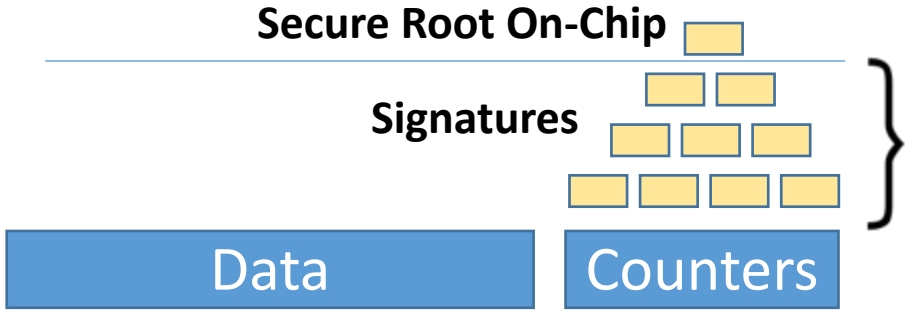

Integrity-Tree

How Do Secure Memories Work ?

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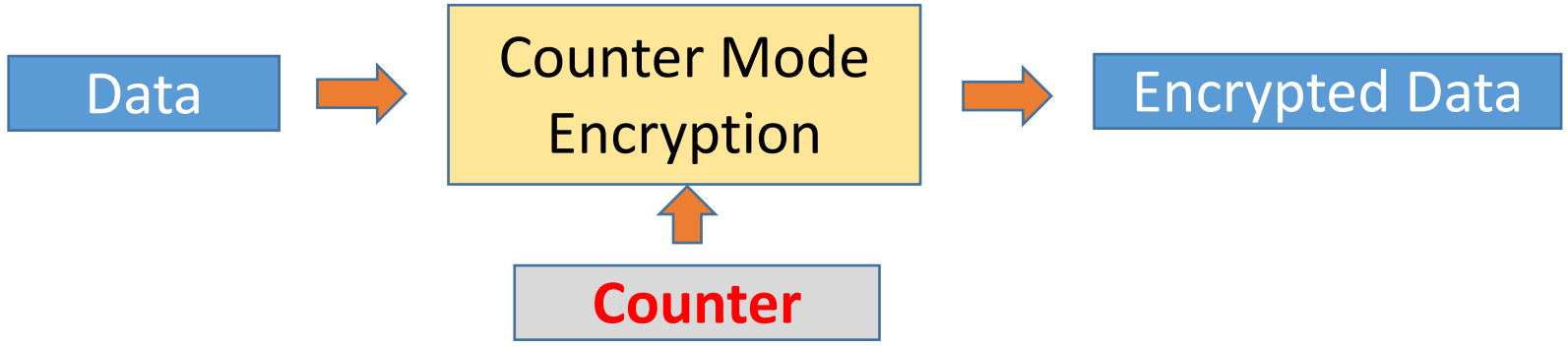

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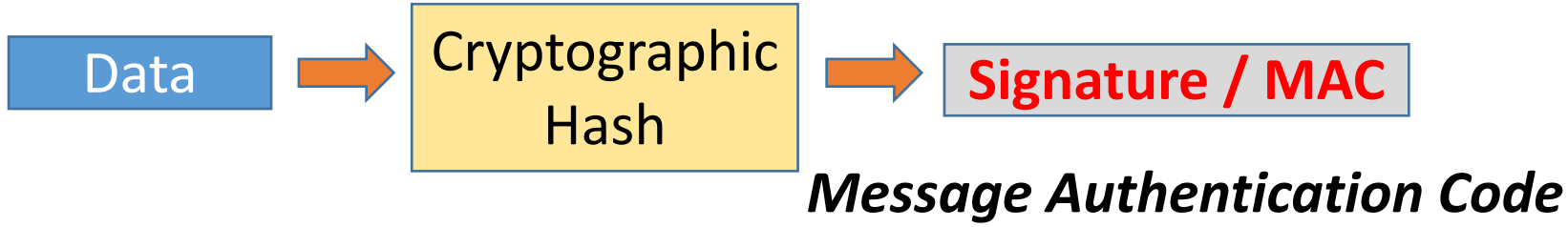

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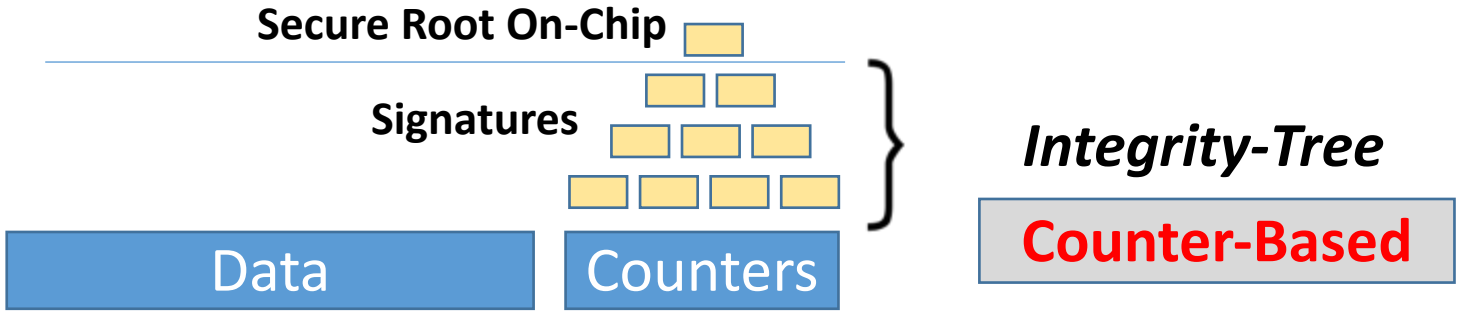

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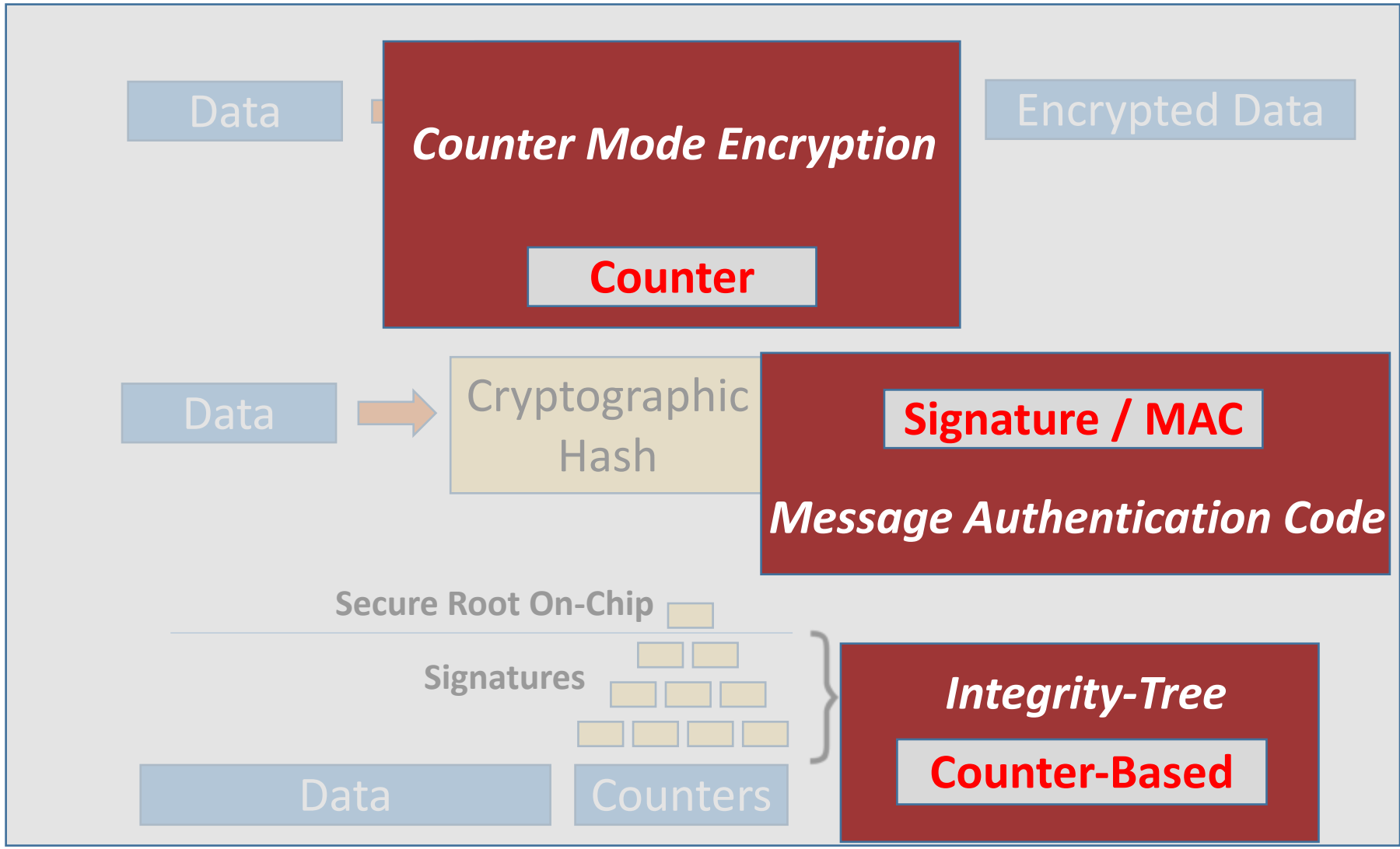
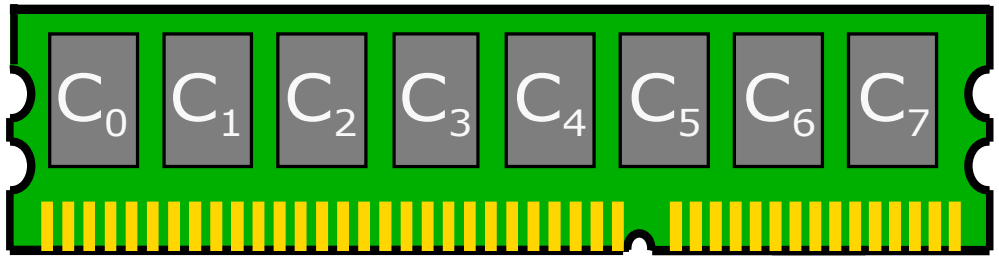
Intel SGX



Problem: Metadata Accesses Consume Memory Bandwidth



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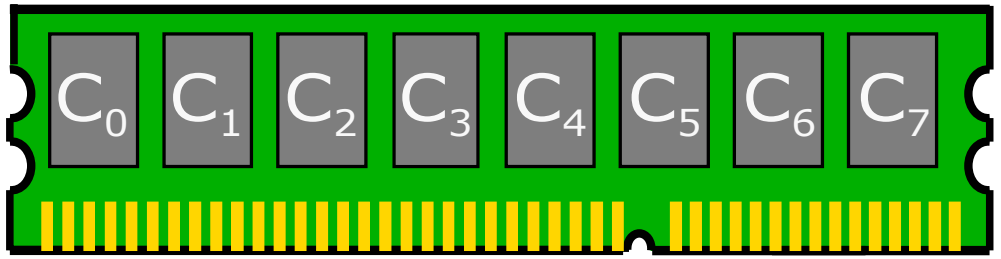

Access Number

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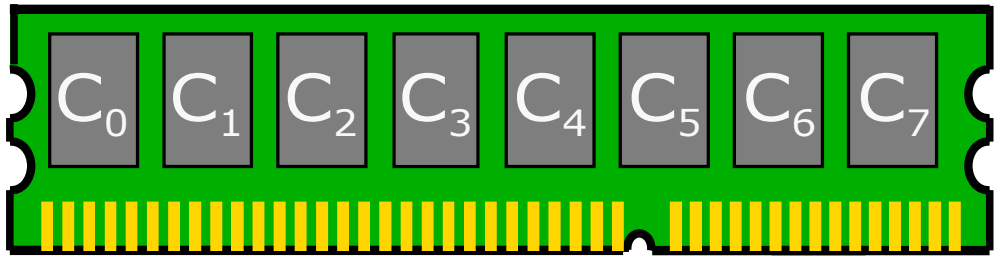
Data Cacheline

Problem: Metadata Accesses Consume Memory Bandwidth



Access Number

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2 Ctr Encryption Counter Cacheline — **Used to Encrypt Data**

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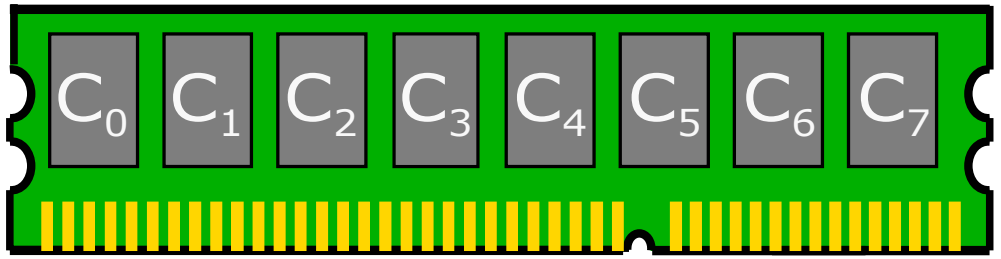

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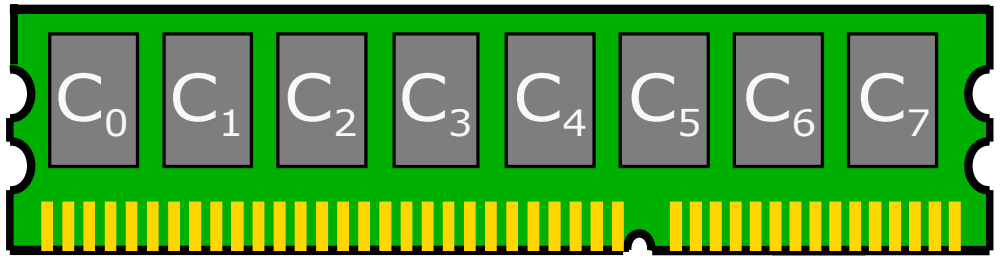

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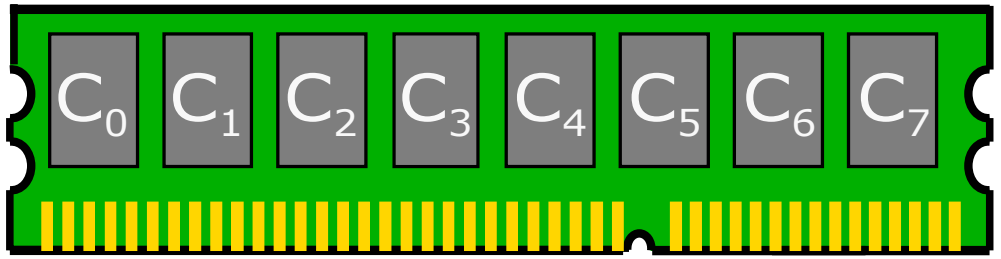

Secure Memory *can require*
4+ memory accesses *for each* ***Data access***

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Memory Access Bloat

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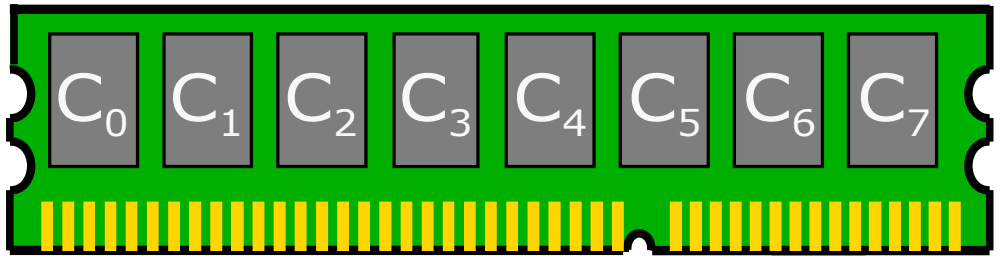

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Cacheable On-Chip

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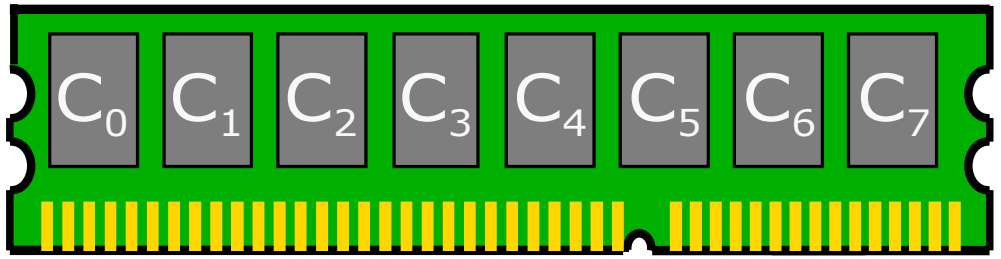

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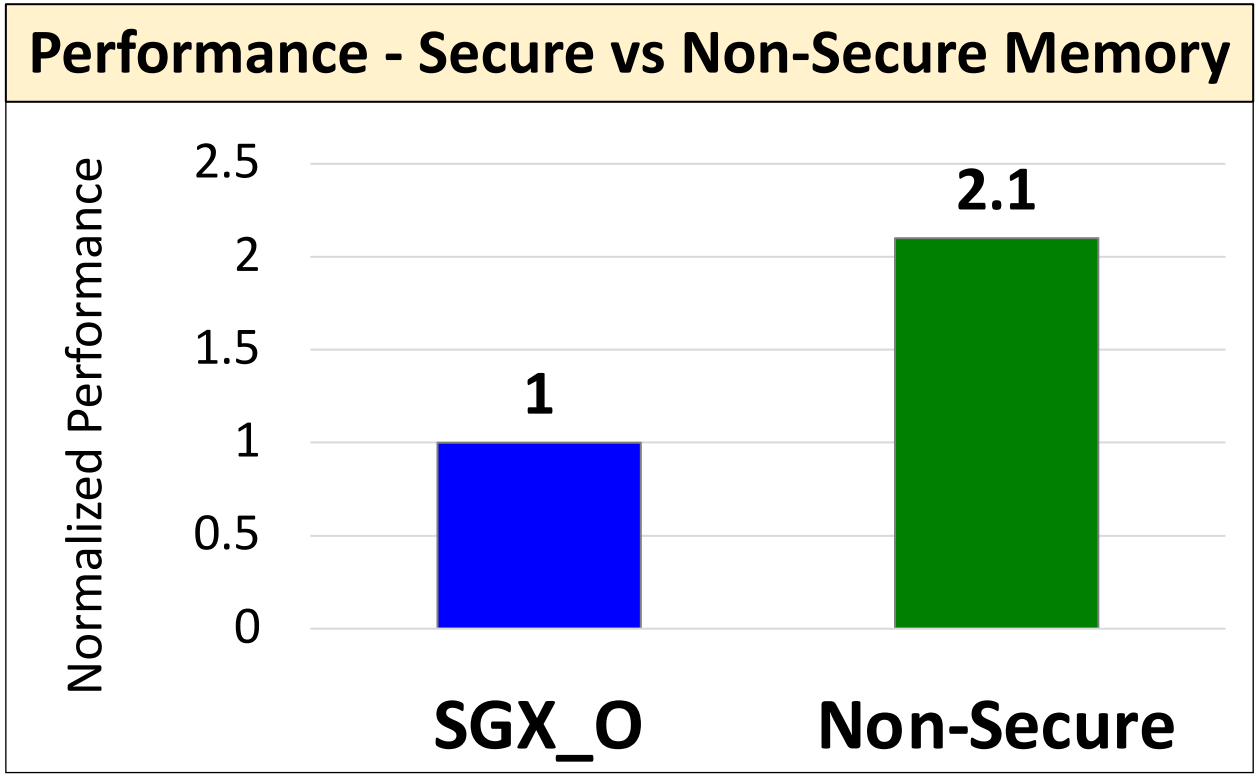
Memory Access Bloat

Memory Access Bloat due to Security Metadata can lead to Performance Overheads

Dissecting Overheads For Secure Memory



SGX_O – *Enhanced Baseline for Secure Memory*

(SGX with LLC shared by Counters & Data)

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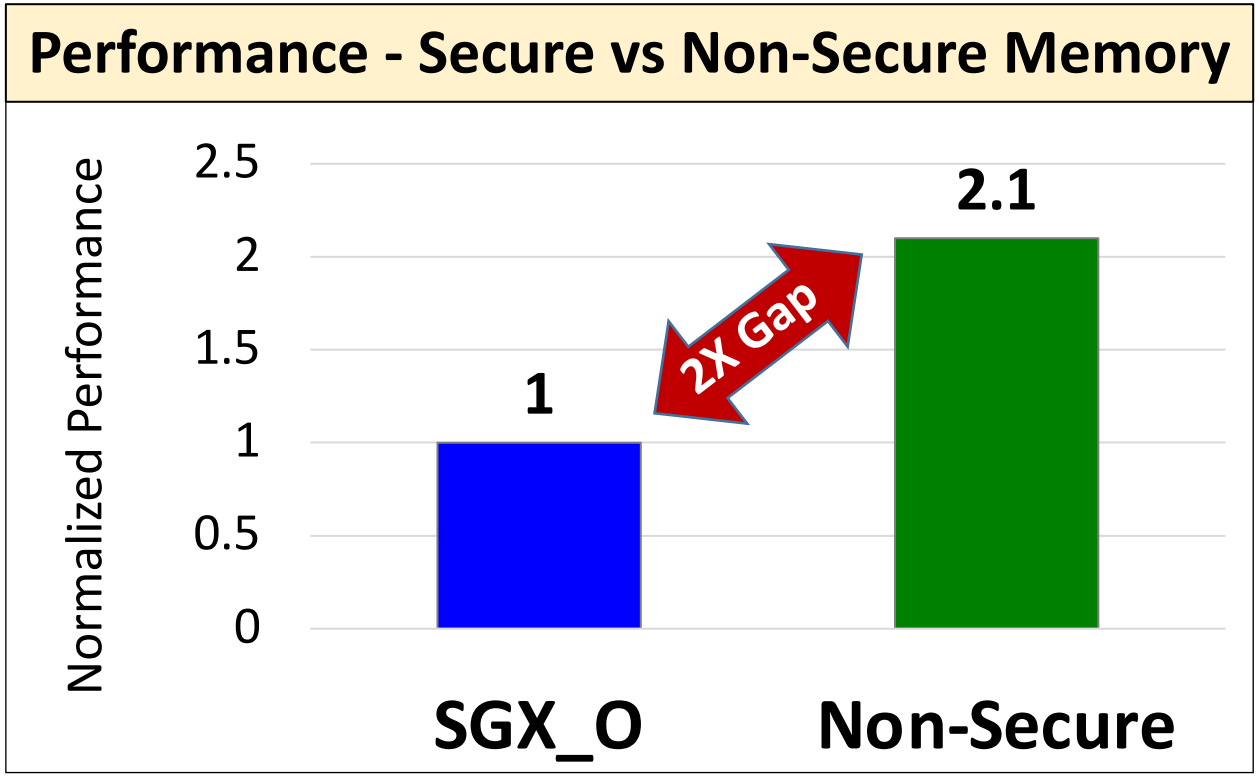

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Dissecting Overheads For Secure Memory

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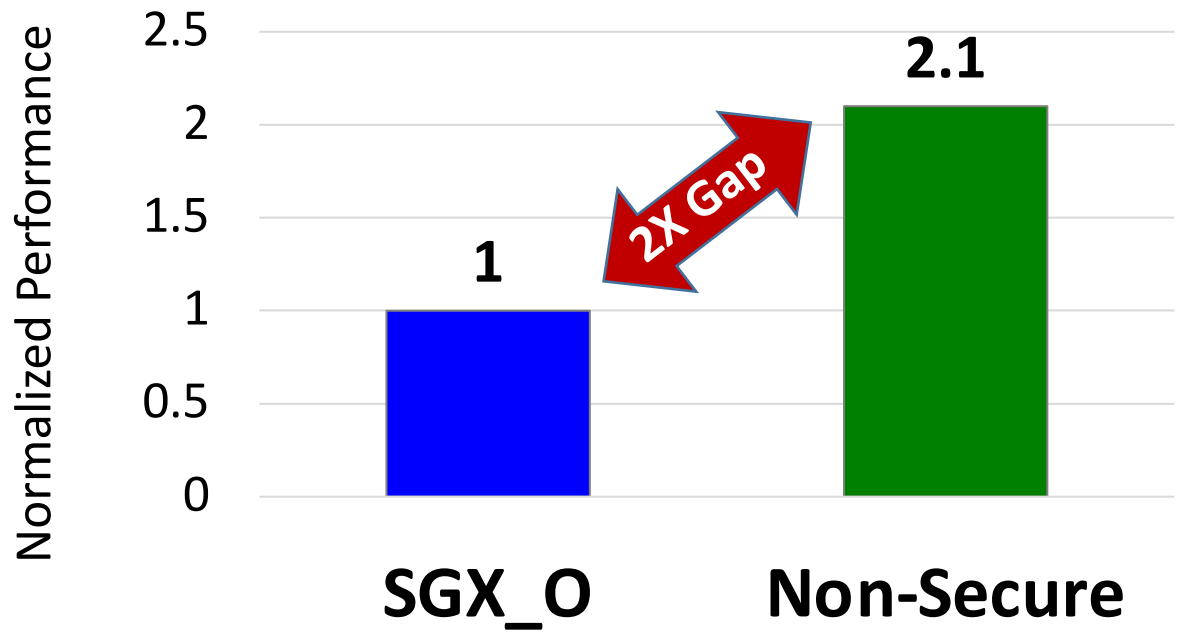

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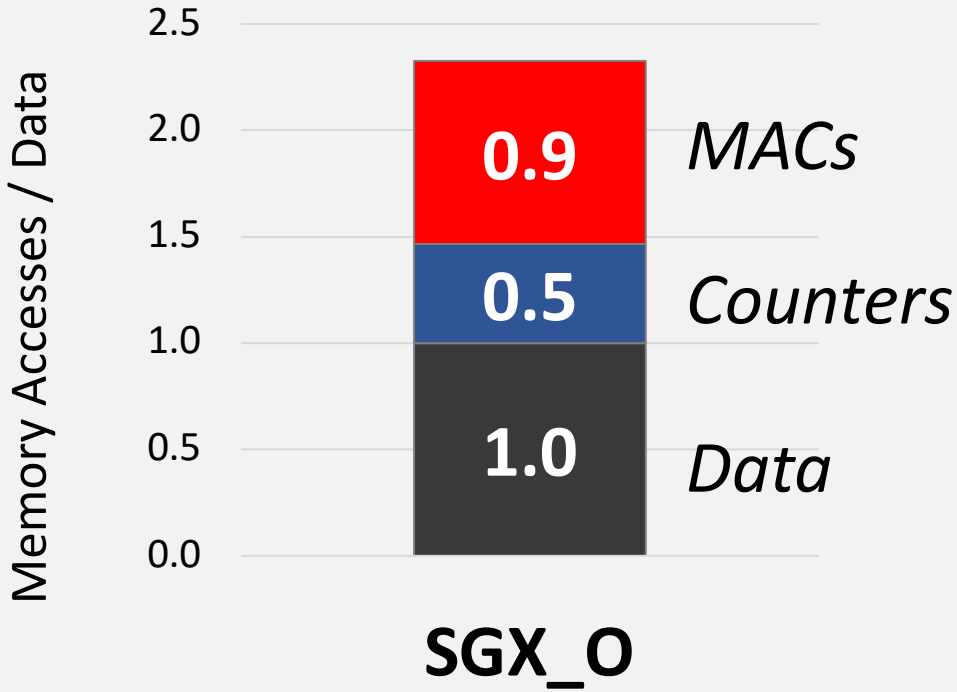
Cause: Memory access bloat due to metadata accesses



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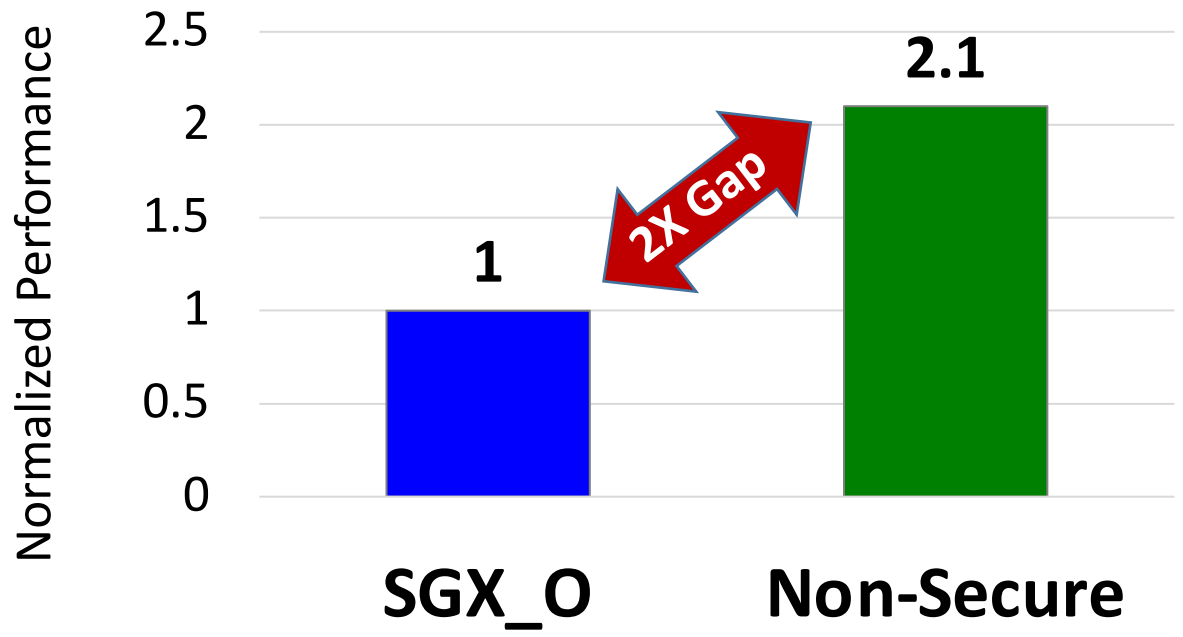

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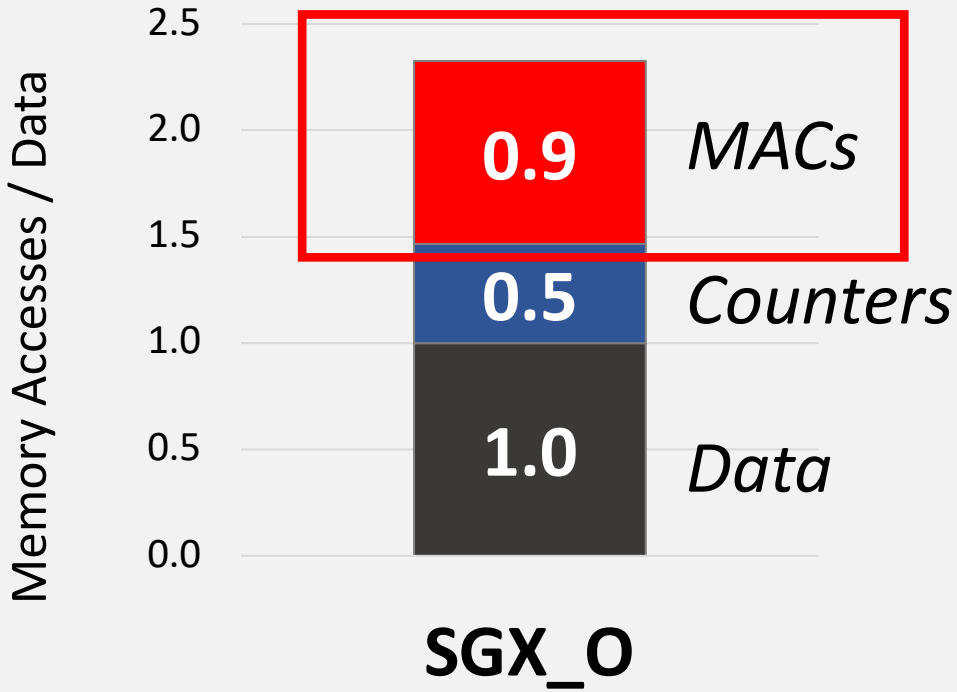

MACs cause 0.9x additional accesses – *focus of this paper !*

Dissecting Overheads For Secure Memory

Goal:

Reduce MAC access bloat to improve secure memory performance

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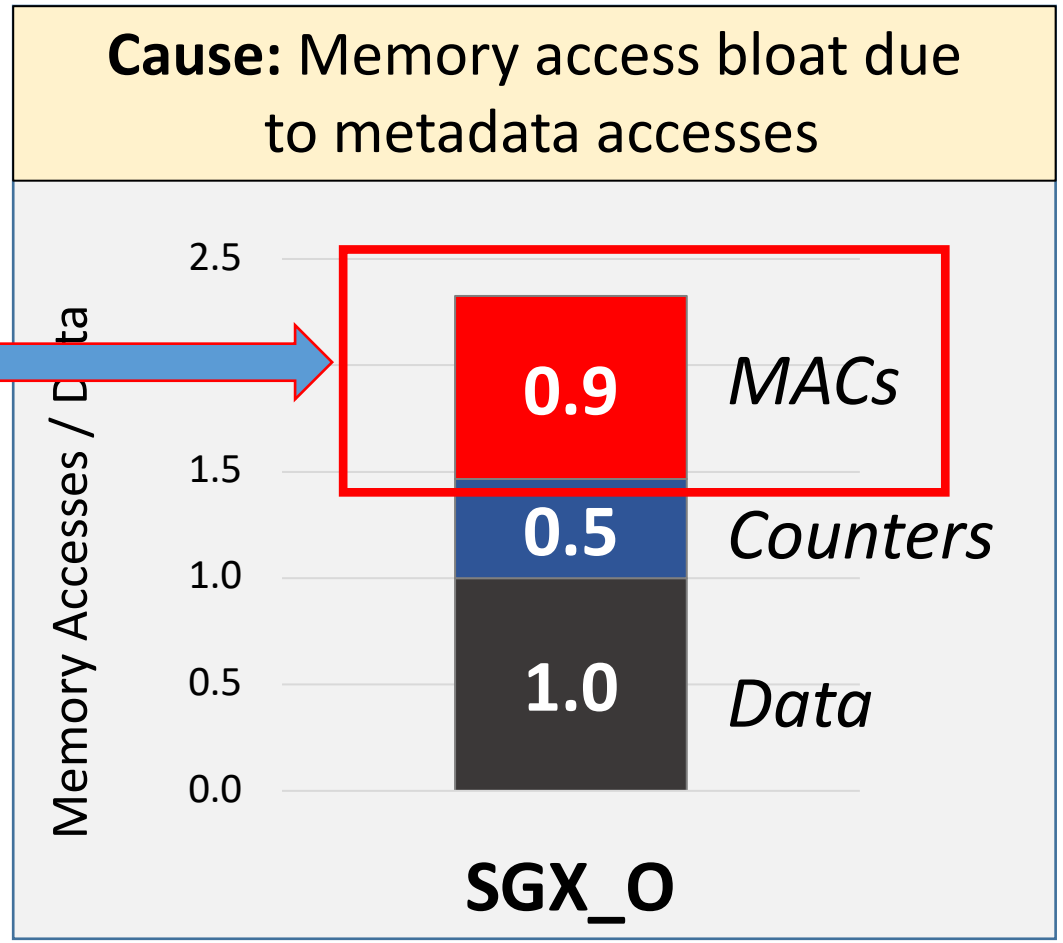

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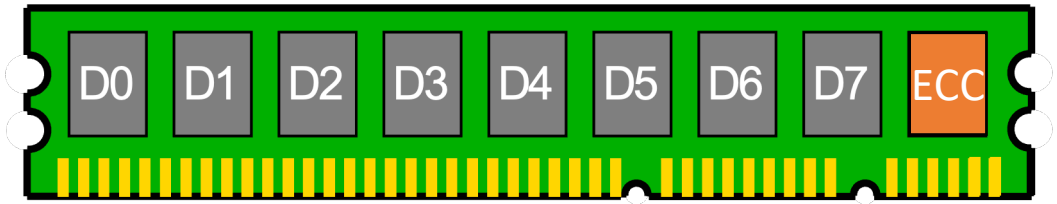
Insight: Leverage ECC-DIMM To Reduce MAC Overheads

ECC-DIMM for Reliability



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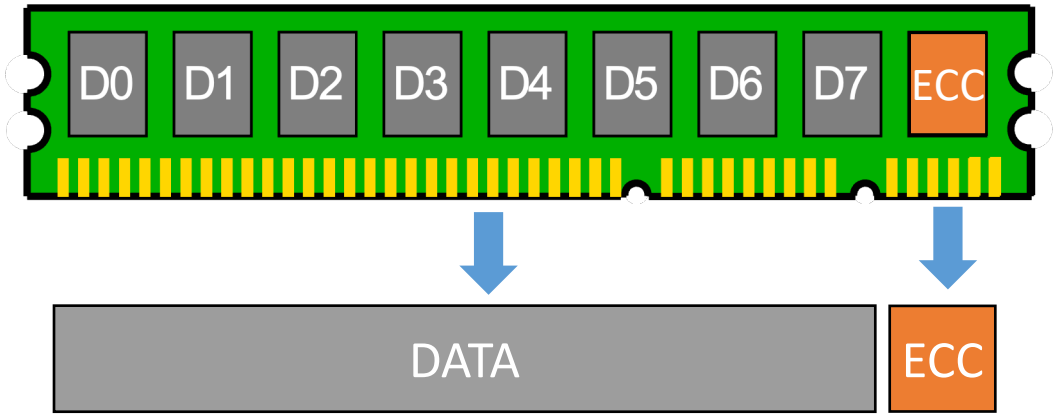


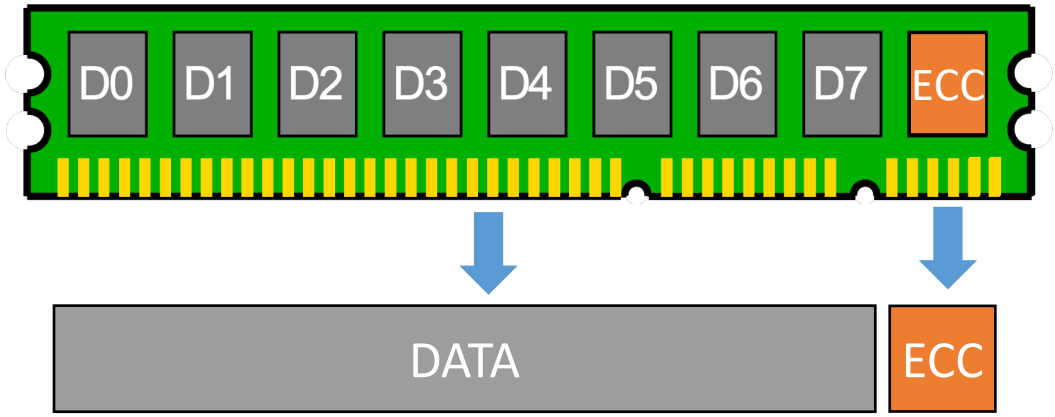
ECC

Fetched

Same Access as Data

Insight: Leverage ECC-DIMM To Reduce MAC Overheads

ECC-DIMM for Reliability



ECC

Fetched *Same Access as Data*

Detects *2-Bit Errors*

Corrects *1-Bit Error*

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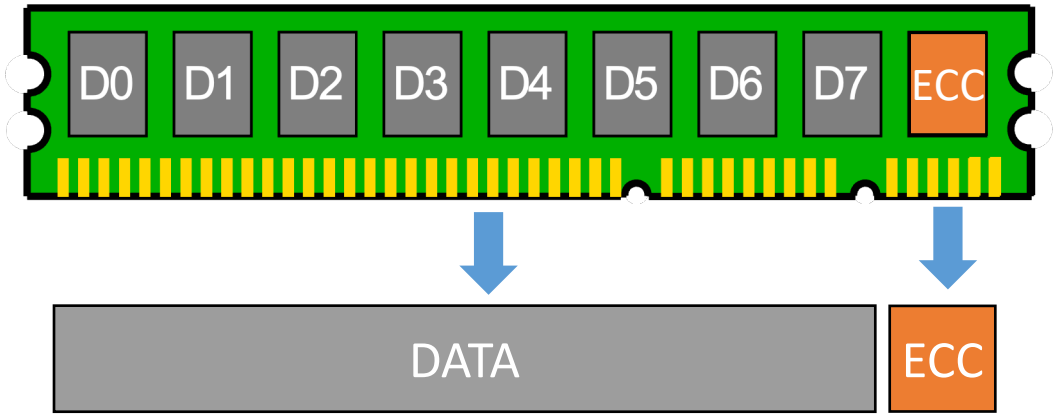

ECC

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Rare

Insight: Leverage ECC-DIMM To Reduce MAC Overheads

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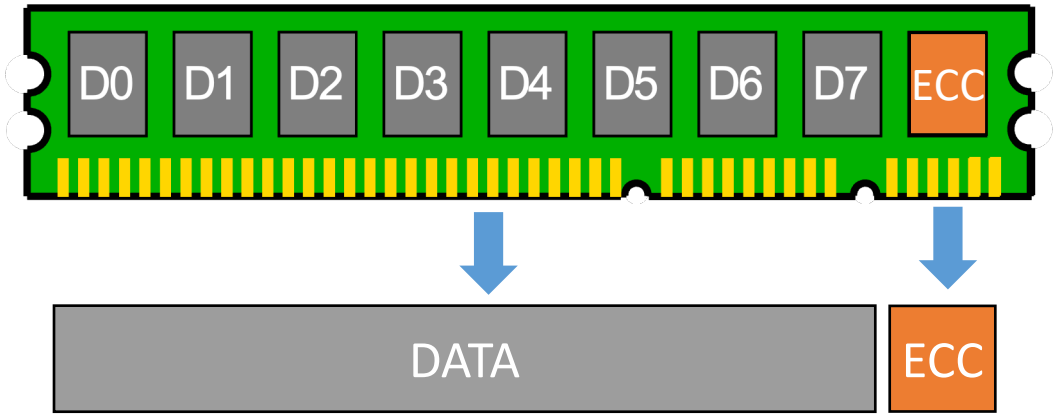

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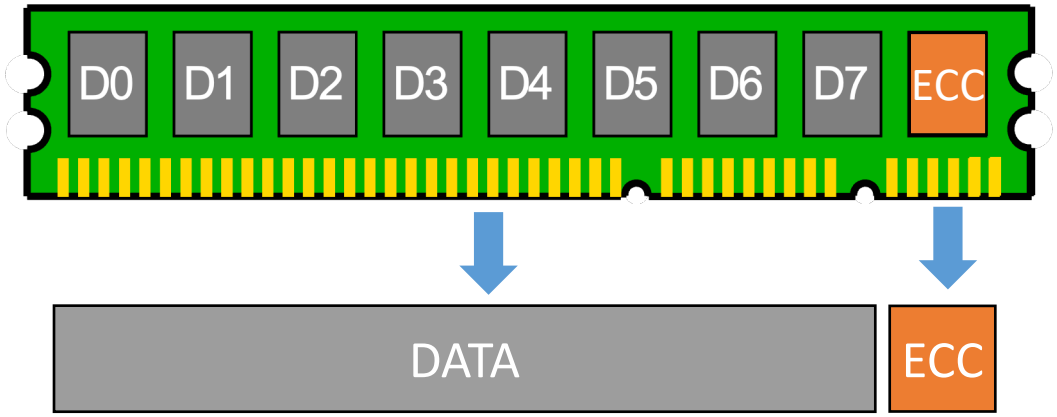
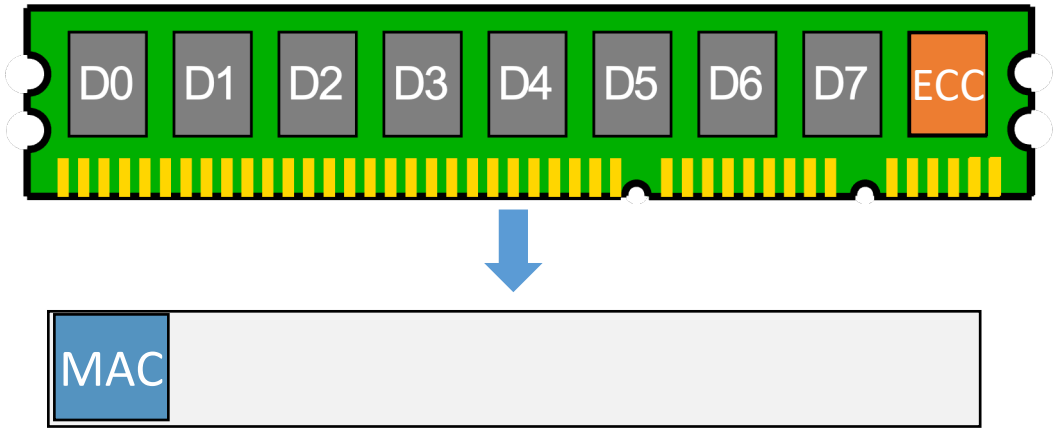


Security with MAC



	ECC	MAC
Fetched	*Same Access as Data*	*Separate Access*
Detects	*2-Bit Errors*	

Insight: Leverage ECC-DIMM To Reduce MAC Overheads

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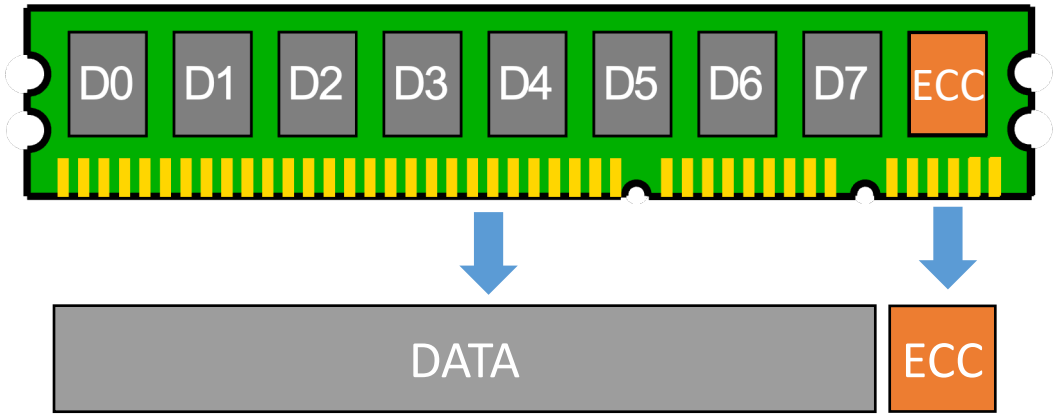

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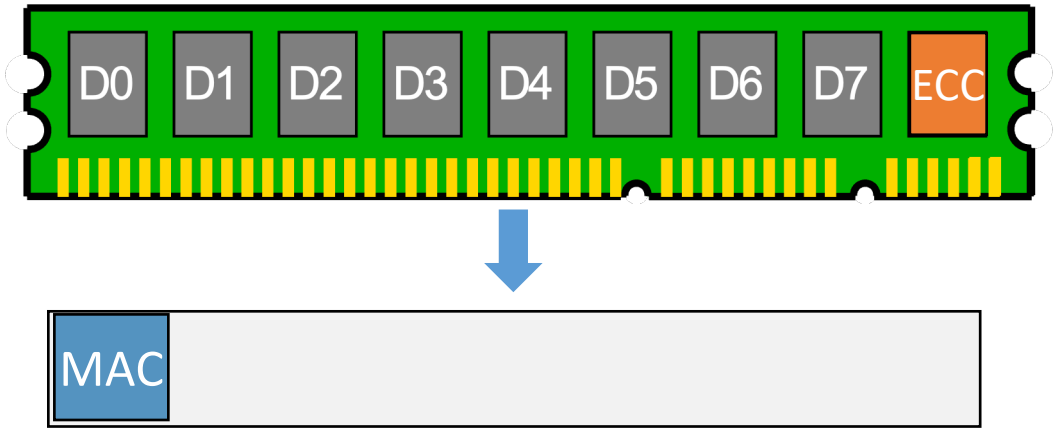

	ECC	MAC
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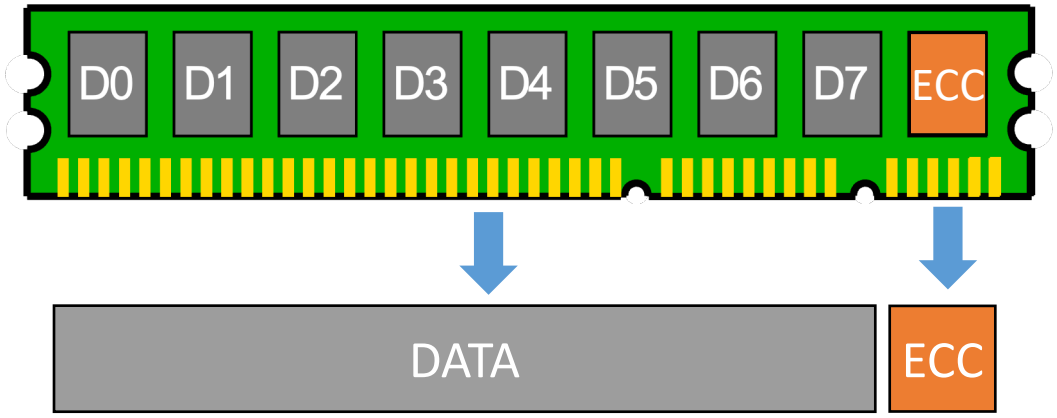
Insight: Leverage ECC-DIMM To Reduce MAC Overheads

ECC-DIMM for Reliability



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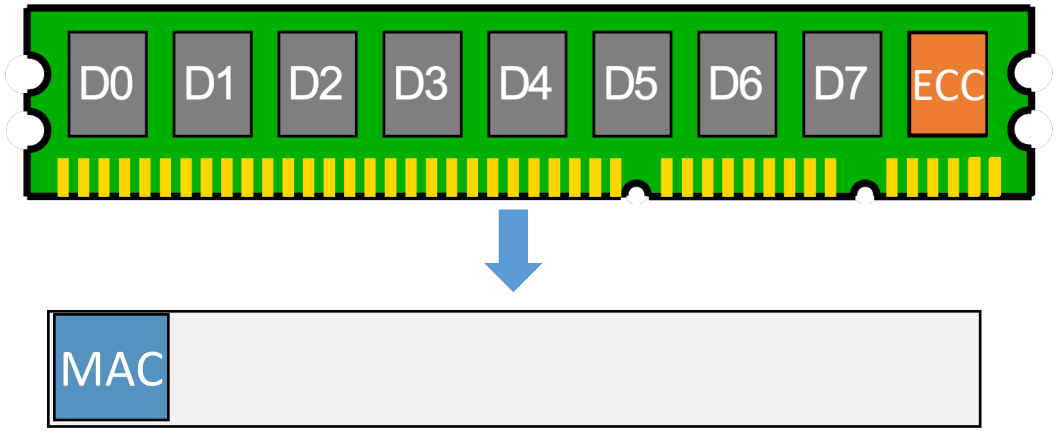

	ECC	MAC
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Replace

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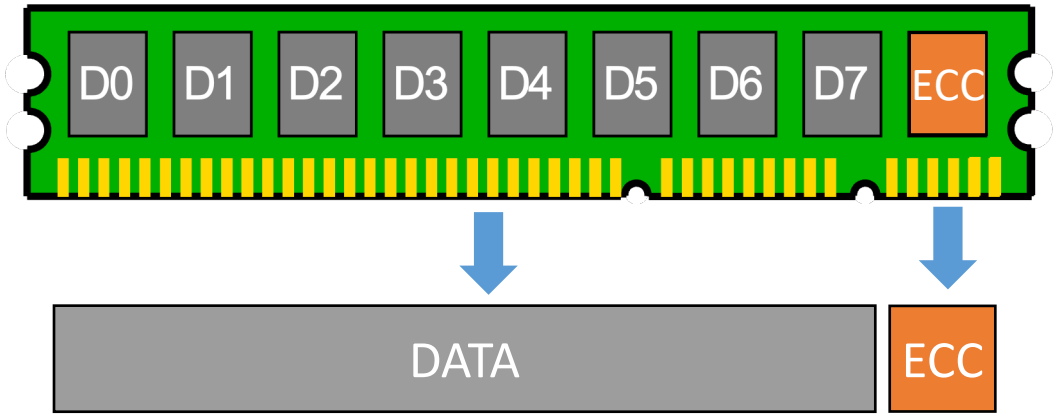
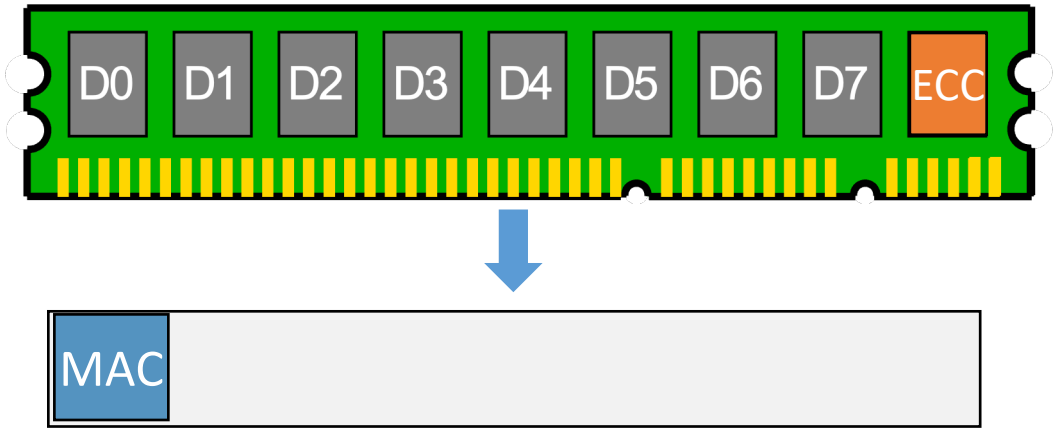


Security with MAC



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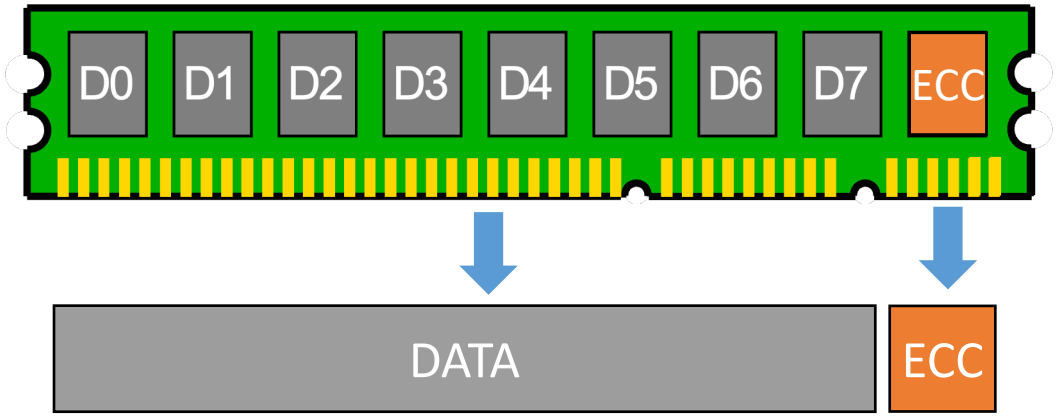
Replace

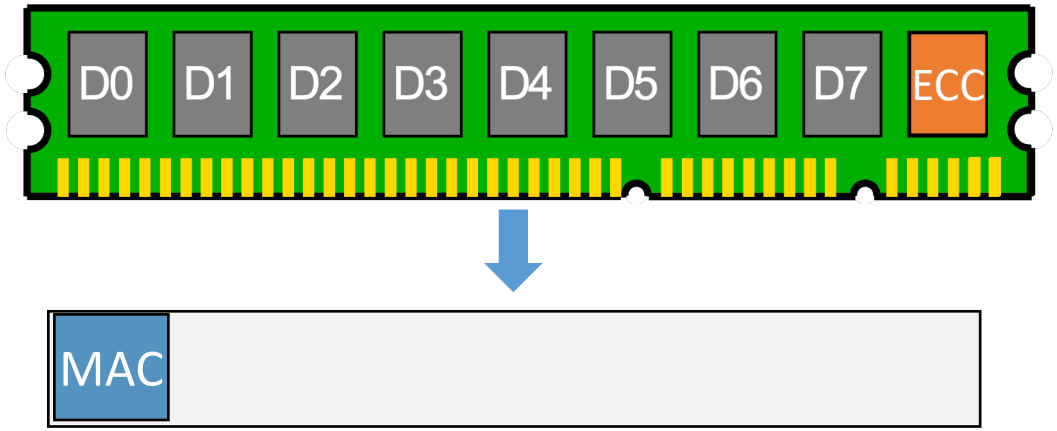
Still need ECC for Correction!

Insight: Leverage ECC-DIMM To Reduce MAC Overheads

ECC-DIMM for Reliability



Security with MAC



	ECC	MAC
Fetched	*Same Access as Data*	*Separate Access*
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Co-Design

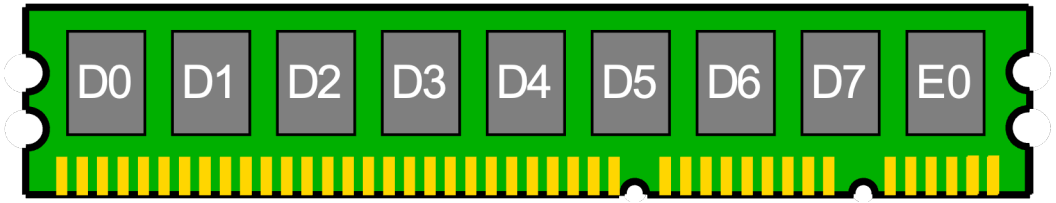
Still need ECC for Correction!

Agenda

- Introduction & Background
- **Synergy Design**
- Evaluation

SYNERGY Co-locates MAC & Data for Performance

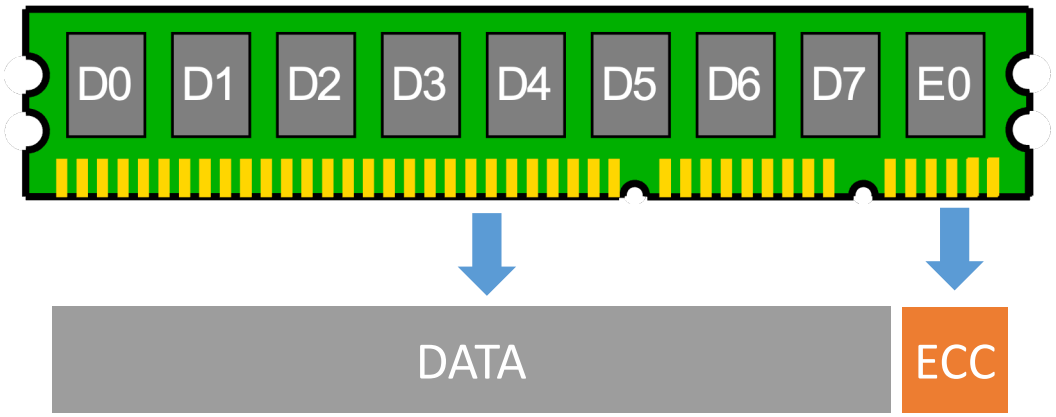
Data Cachelines



Non-Secure

SYNERGY Co-locates MAC & Data for Performance

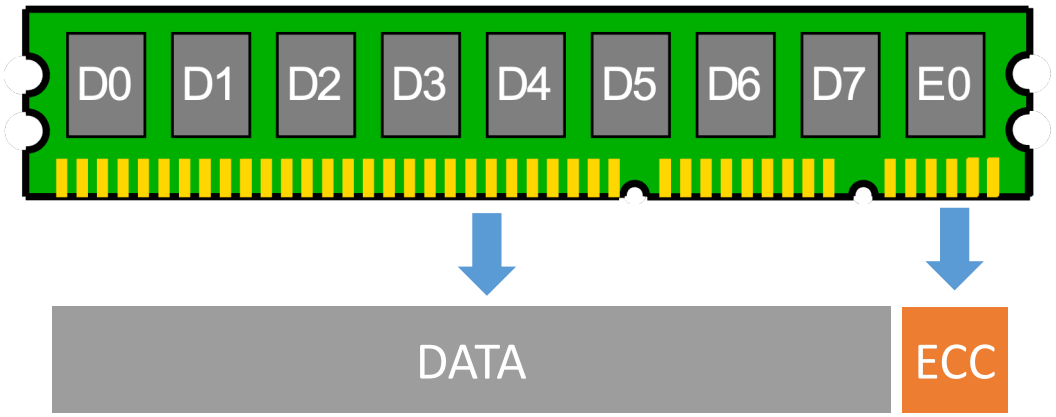
Data Cachelines



Non-Secure - 1 access

SYNERGY Co-locates MAC & Data for Performance

Data Cachelines



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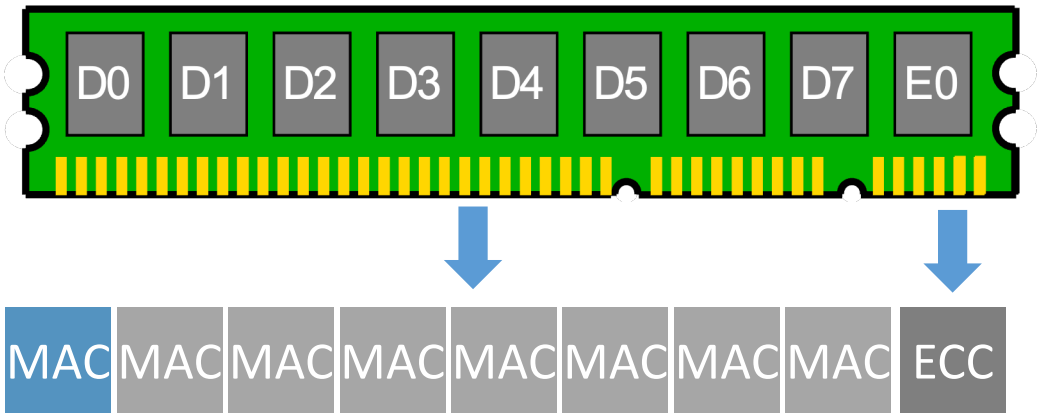
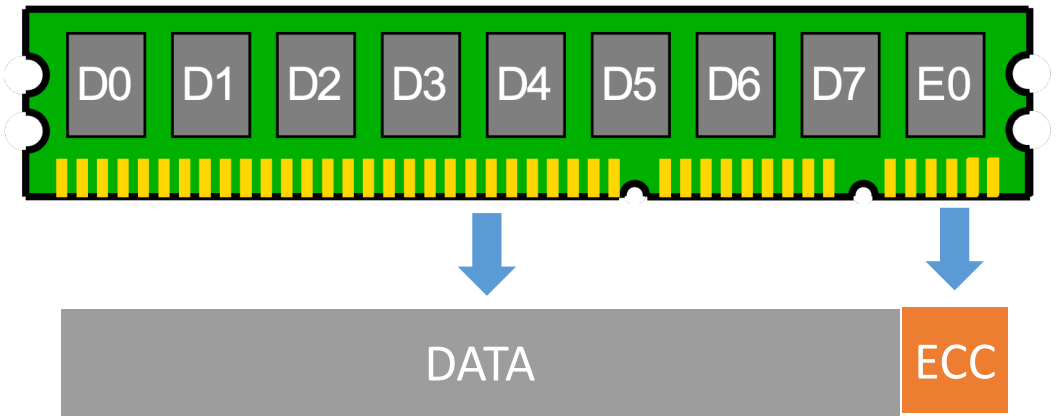
MAC Cachelines



Secure Memory

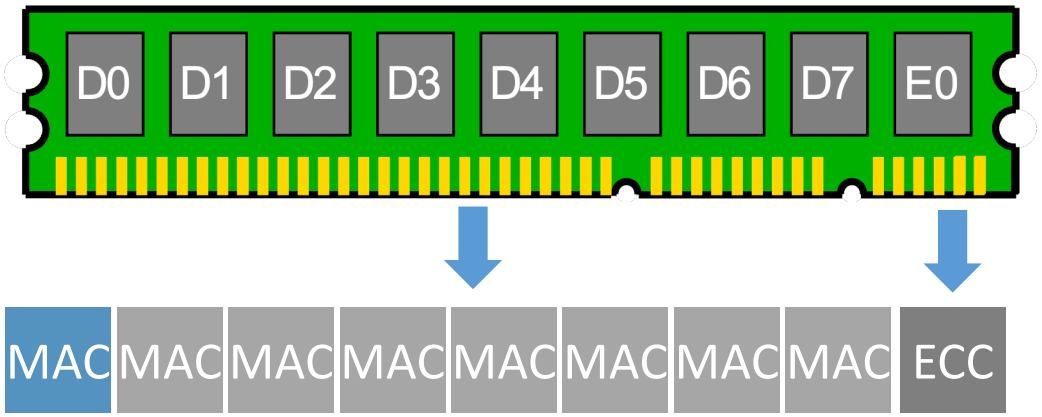
SYNERGY Co-locates MAC & Data for Performance

Data Cachelines



Non-Secure - 1 access

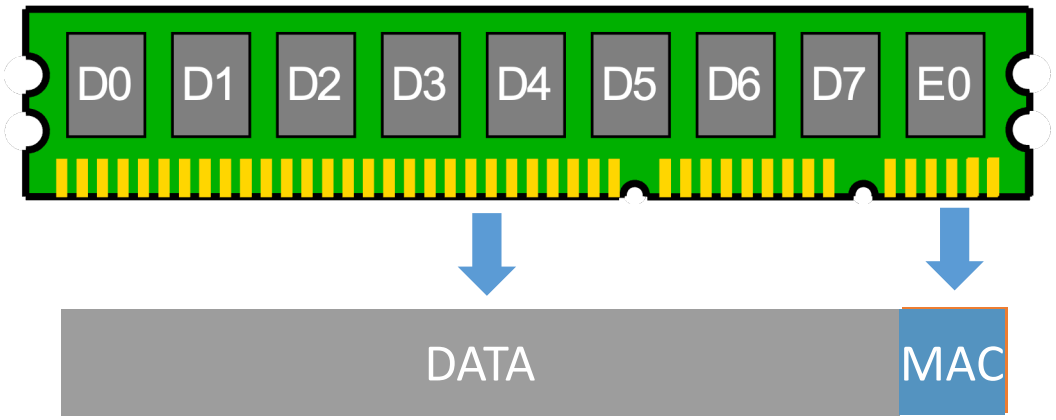
MAC Cachelines



Secure Memory - 2 accesses

SYNERGY Co-locates MAC & Data for Performance

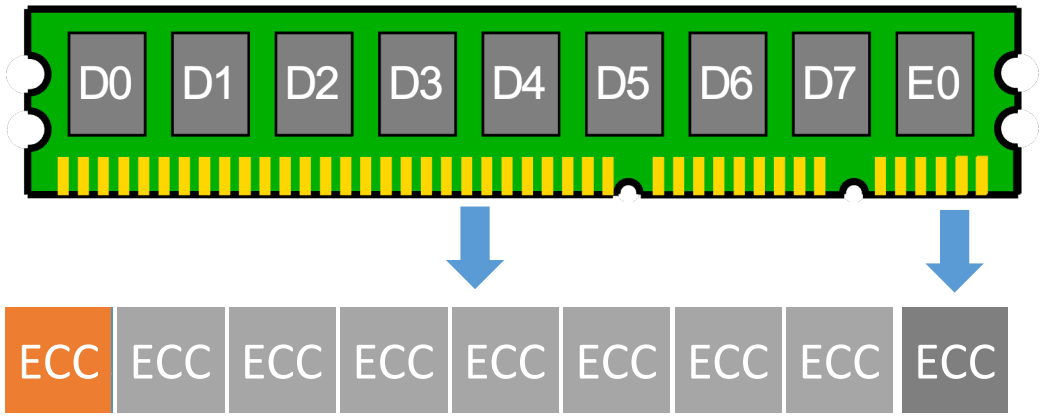
Data Cachelines



Non-Secure - 1 access

SYNERGY

ECC Cachelines



Secure Memory - 2 accesses

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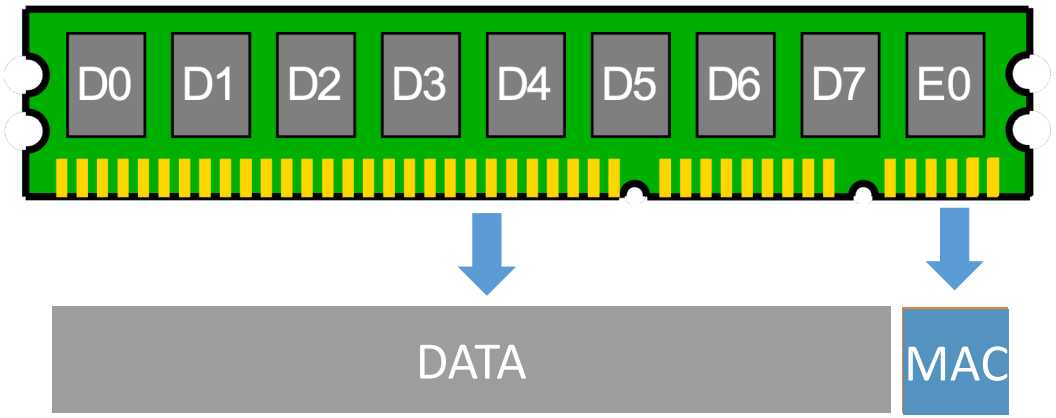
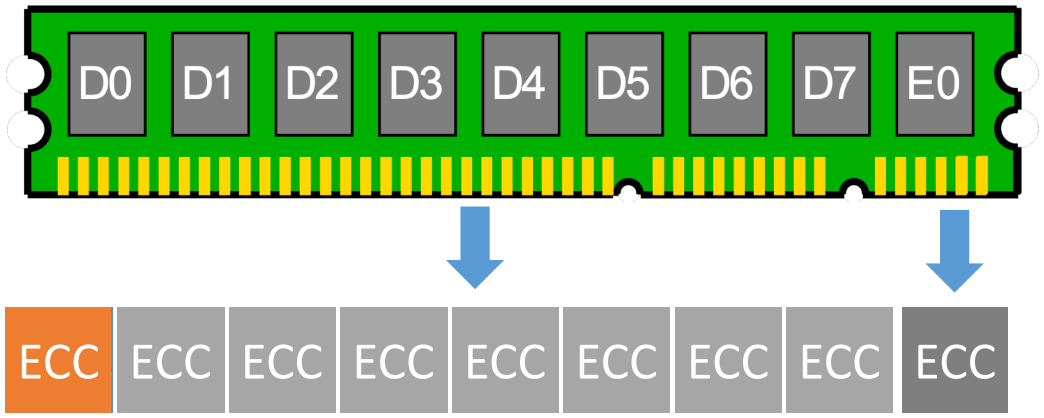


ECC Cachelines



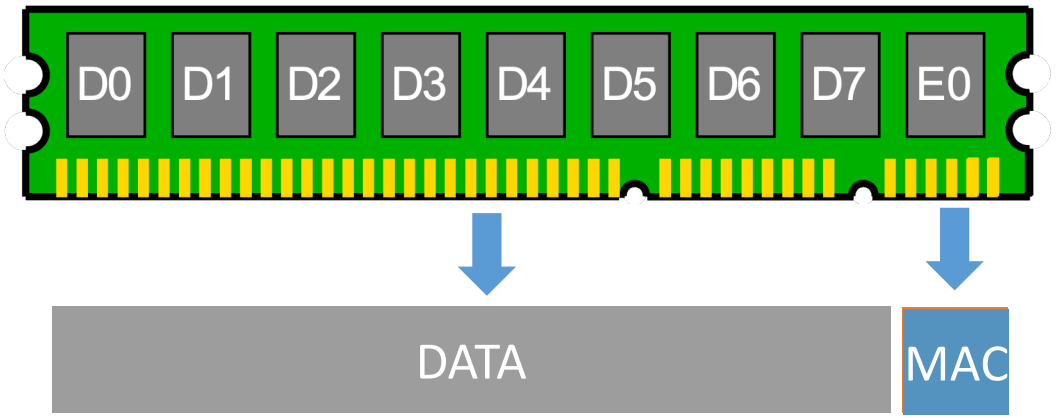
Non-Secure - 1 access

Secure Memory - 2 accesses

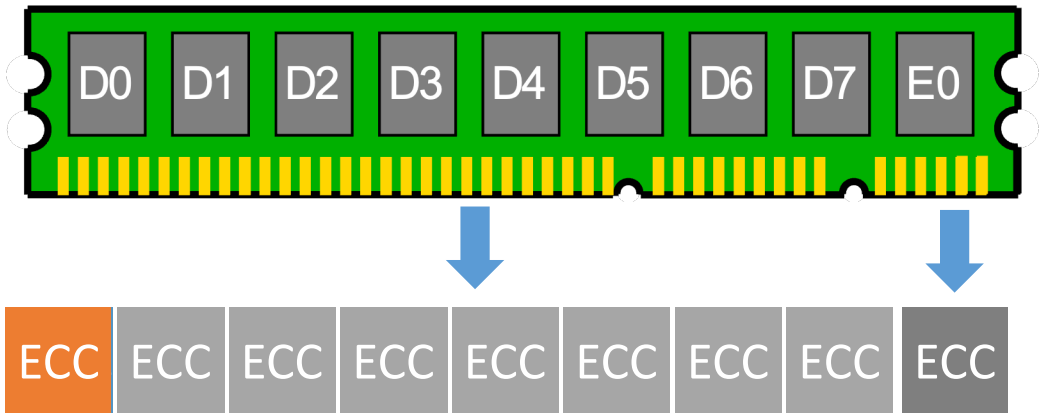
SYNERGY - 1 access for reads, unless error *(rare)*

SYNERGY Co-locates MAC & Data for Performance

Data Cachelines



ECC Cachelines



Non-Secure - 1 access

Secure Memory - 2 accesses

SYNERGY

- 1 access for reads, unless error *(rare)*
- 2 accesses for writes

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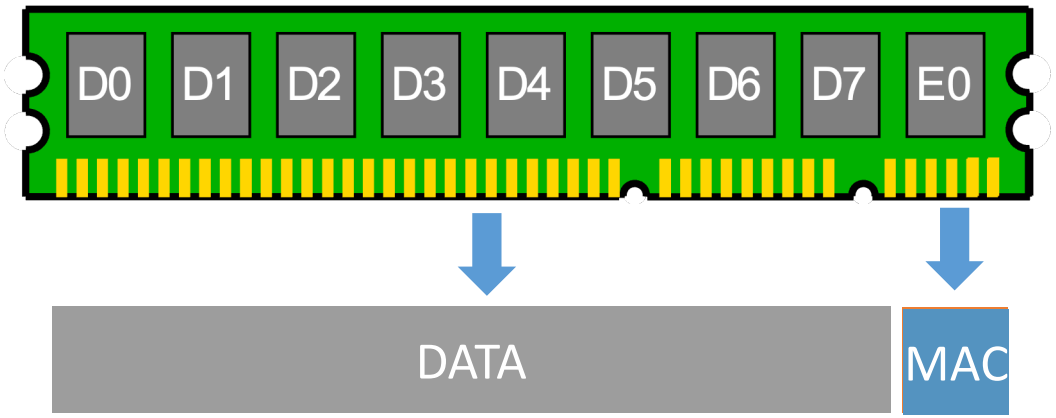

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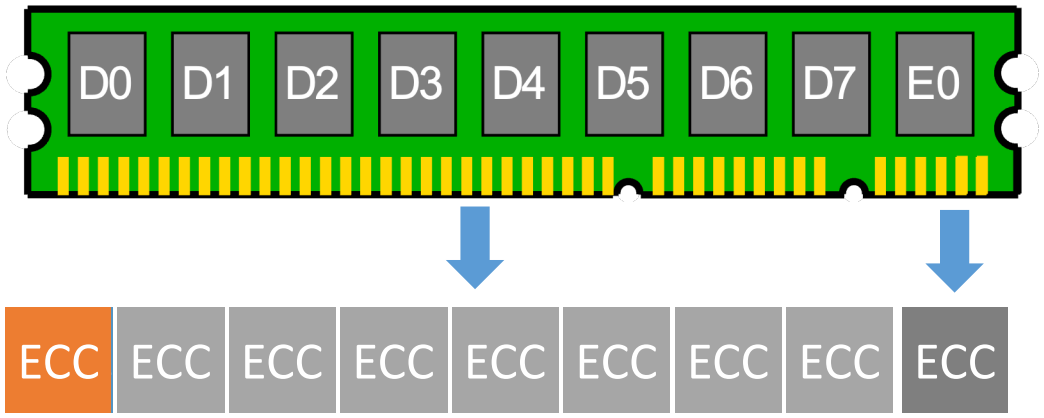

Non-Secure - 1 access

Secure Memory - 2 accesses

SYNERGY
- 1 access for reads, unless error *(rare)*
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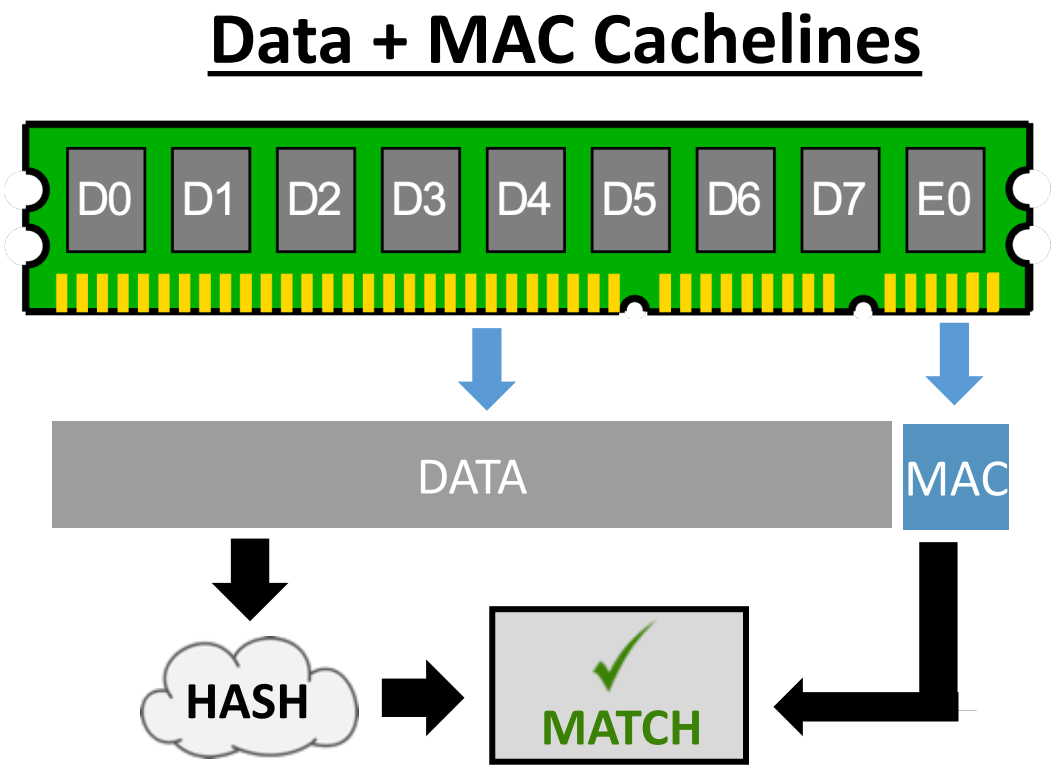
Synergy avoids extra MAC lookups and improves performance, without any additional storage

SYNERGY uses MAC for Error Detection



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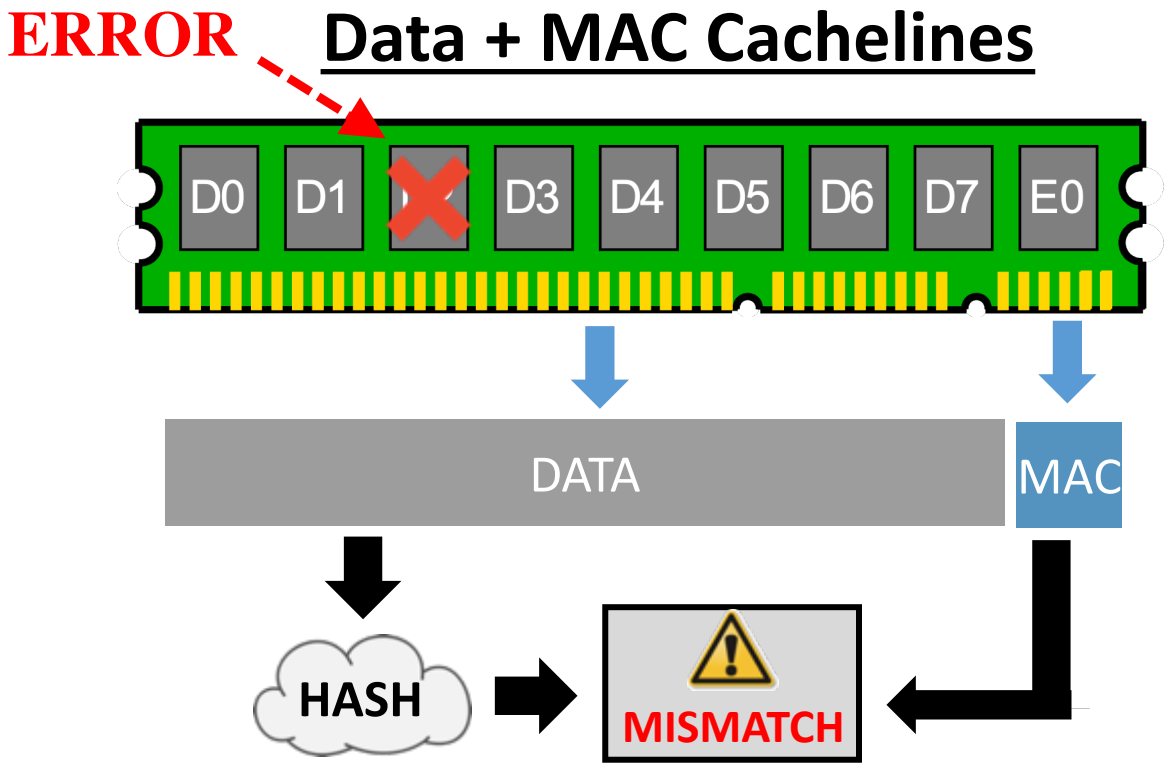

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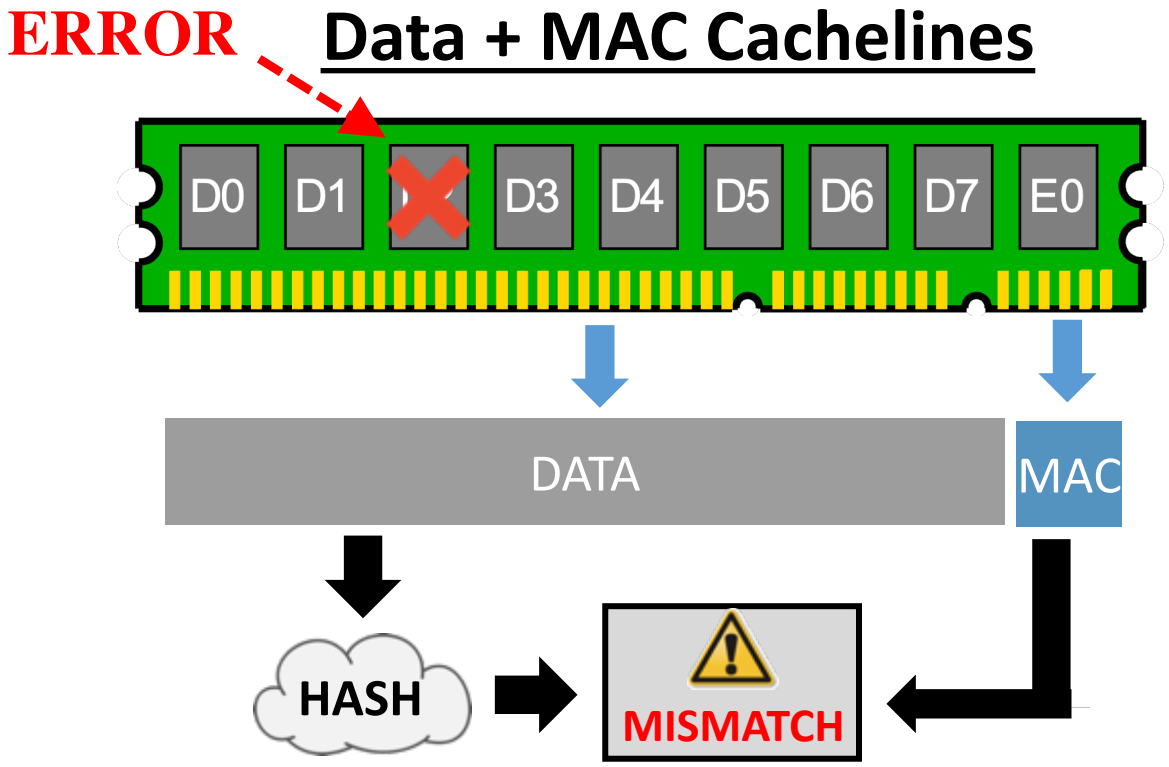
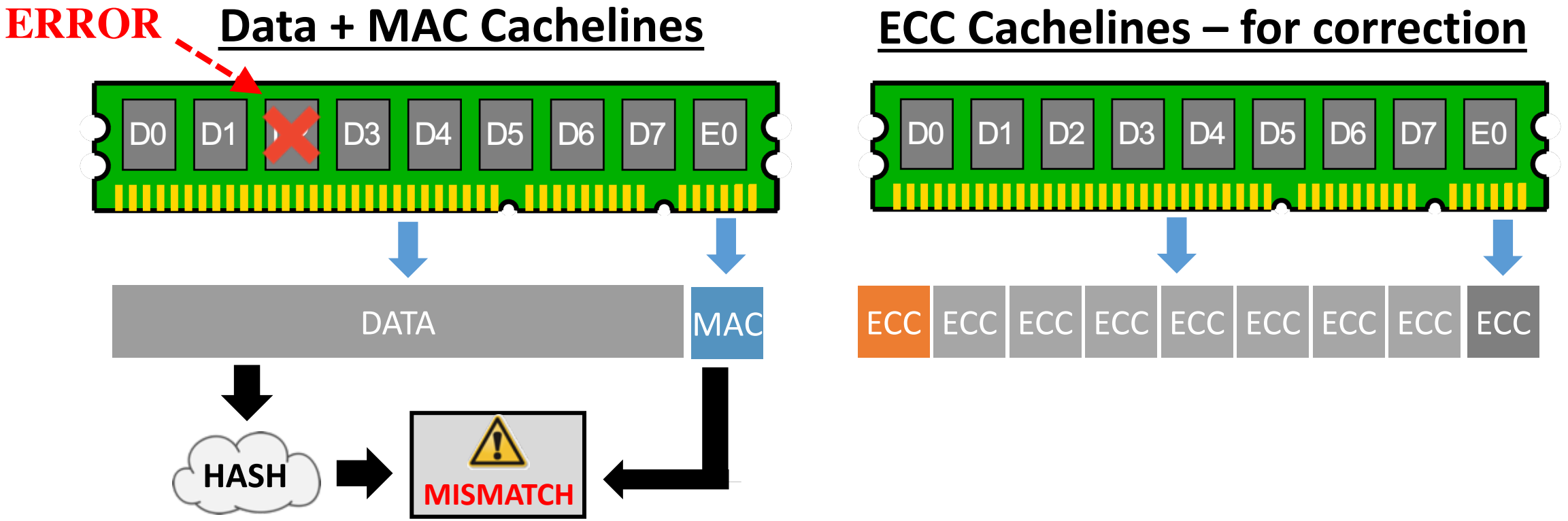


MACs have strong error detection ability

SYNERGY uses MAC for Error Detection



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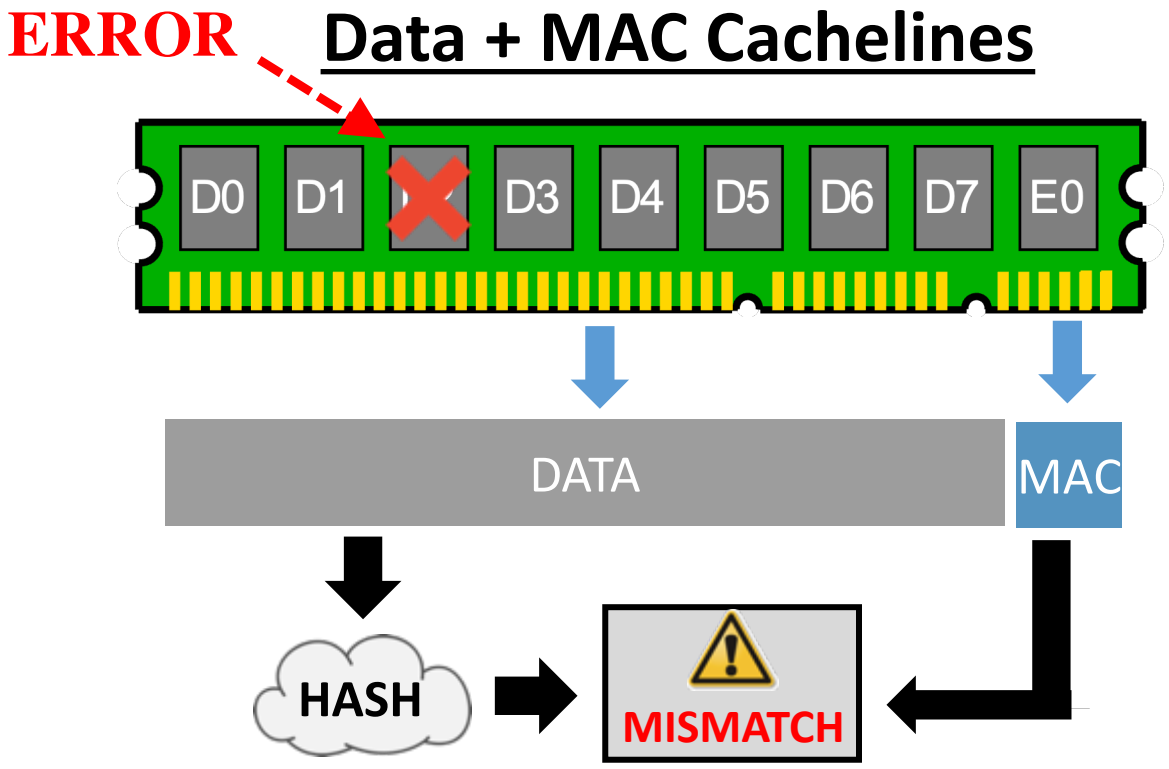

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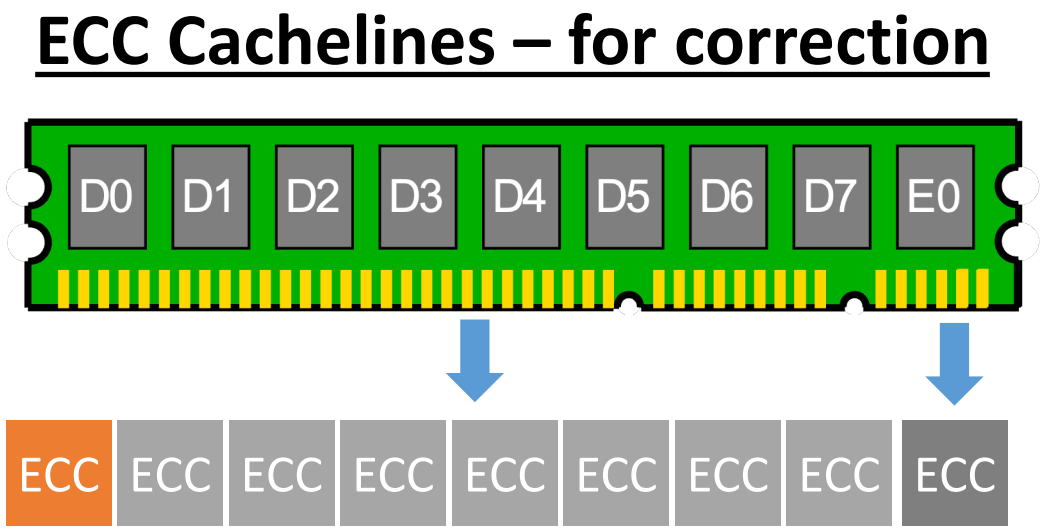

Baseline ECC (SECDED) provides single-bit error correction

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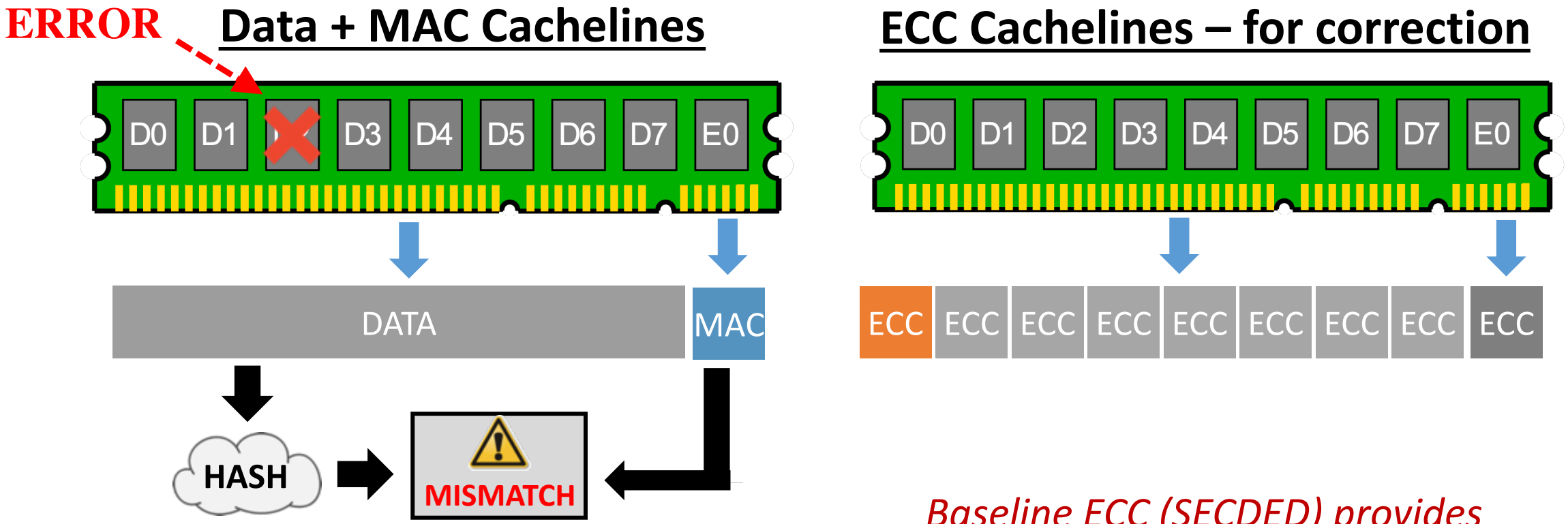

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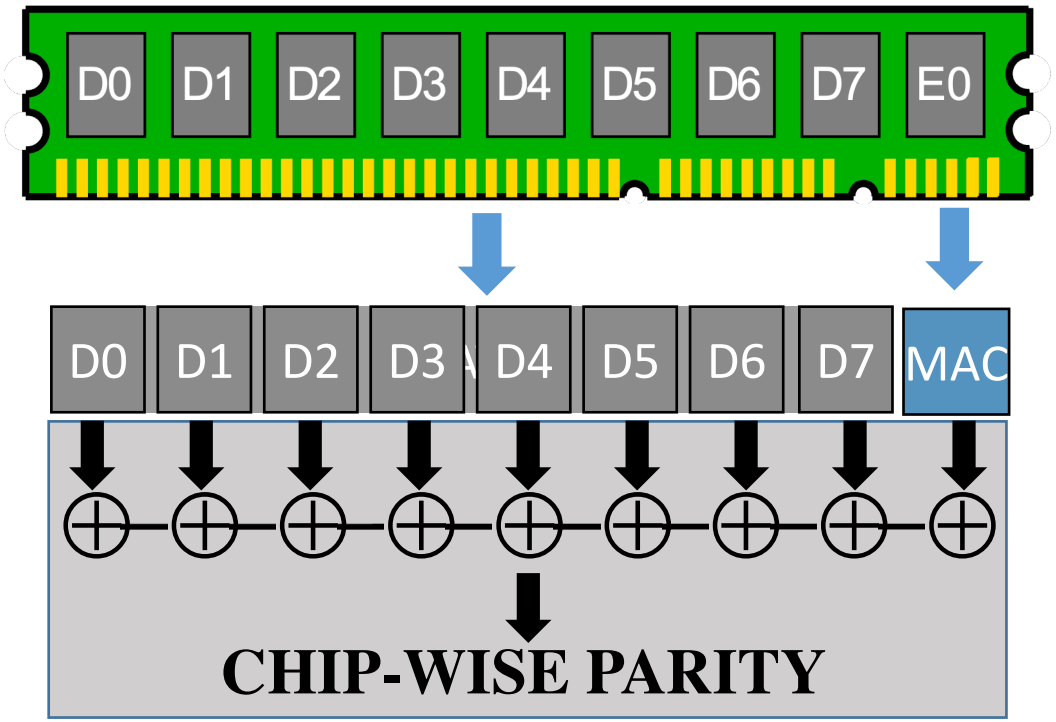
Baseline ECC (SECDED) provides single-bit error correction

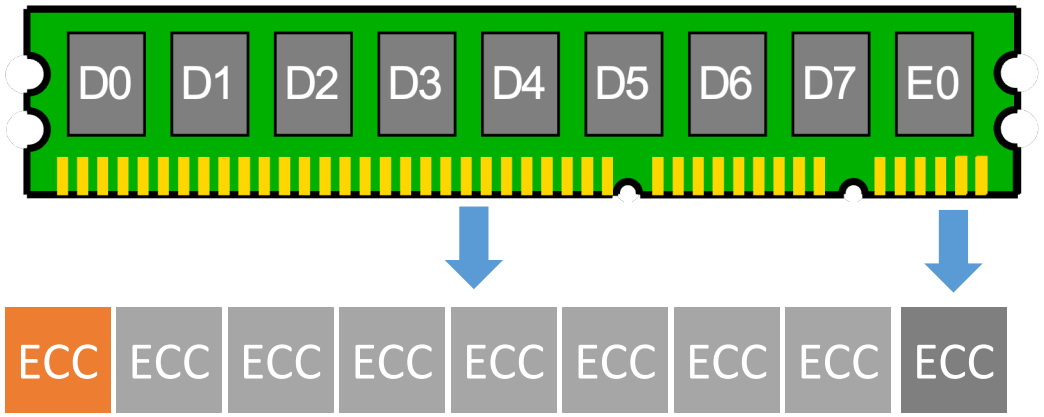
Can We Achieve Stronger Error-Correction with Co-Design?

Parity Can Reconstruct Chip With Failure

Data + MAC Cachelines



ECC Cachelines – for correction



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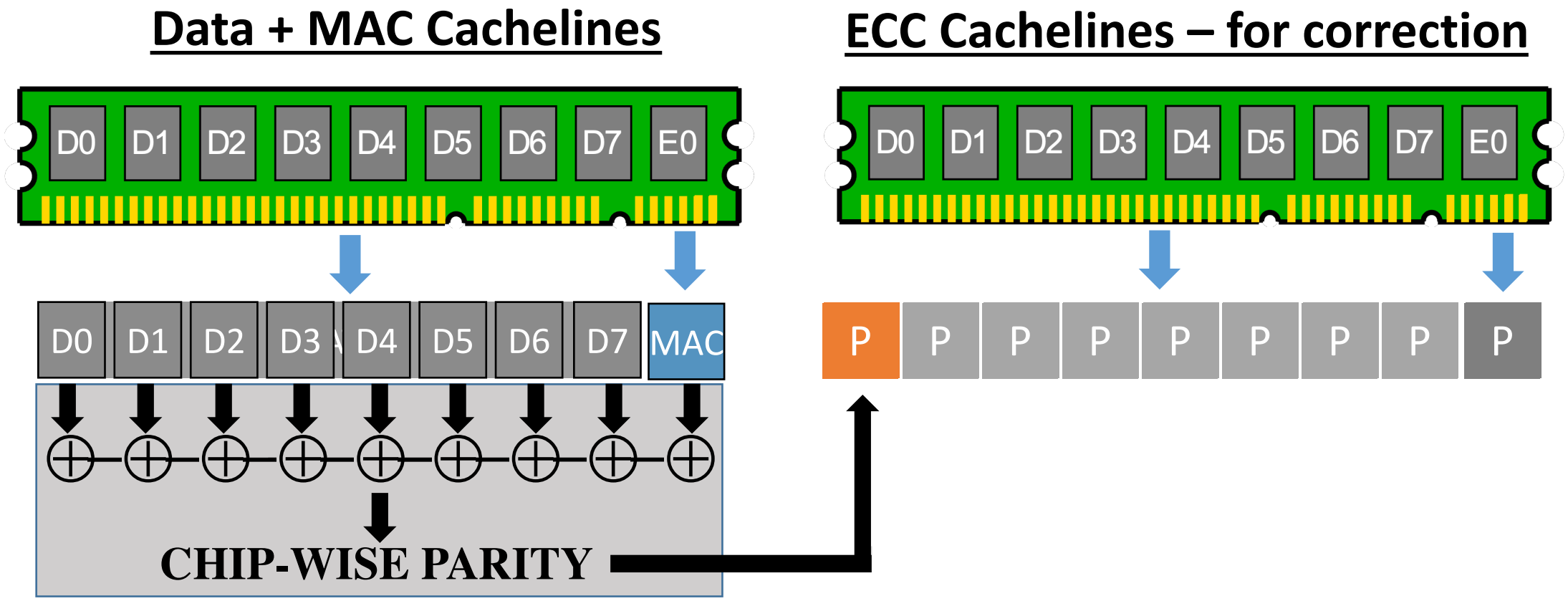

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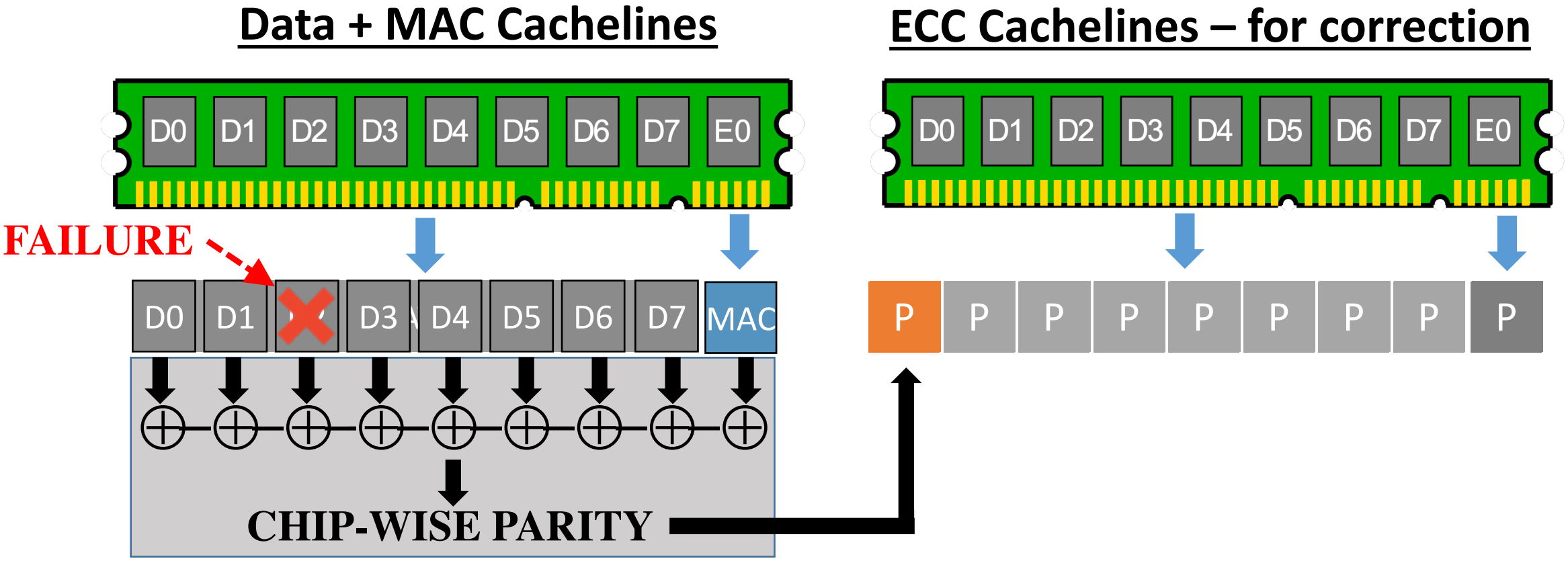

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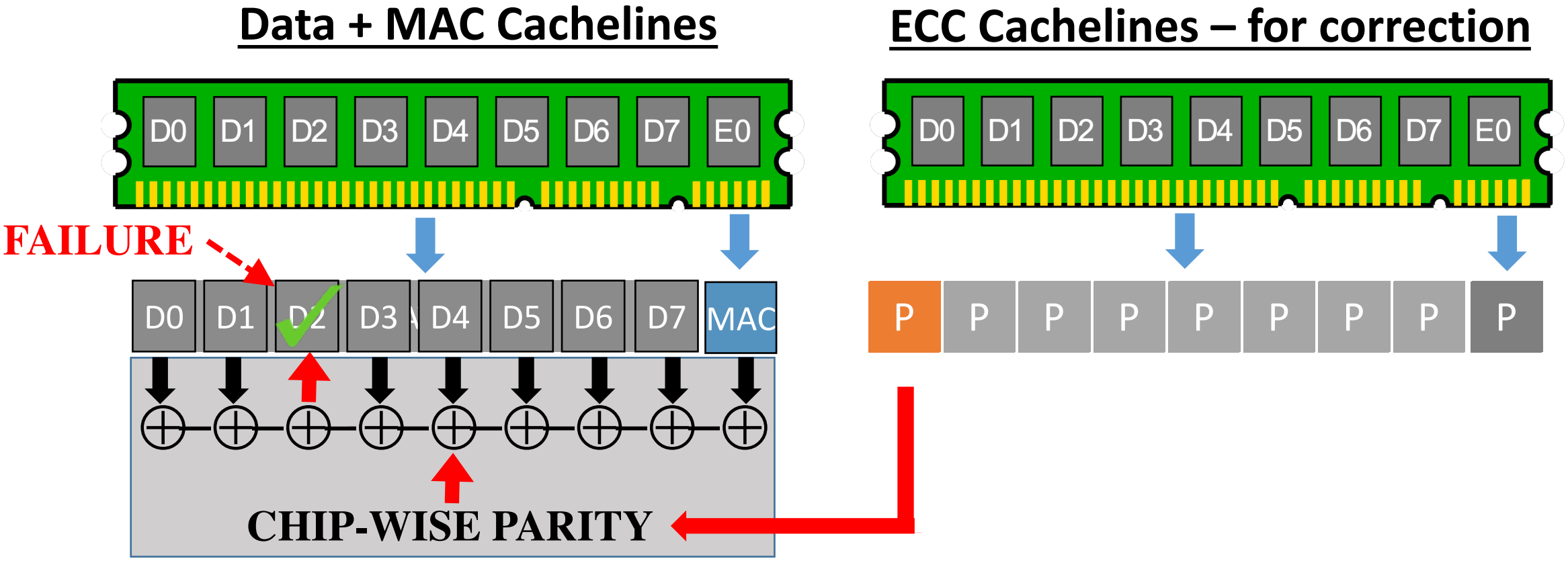

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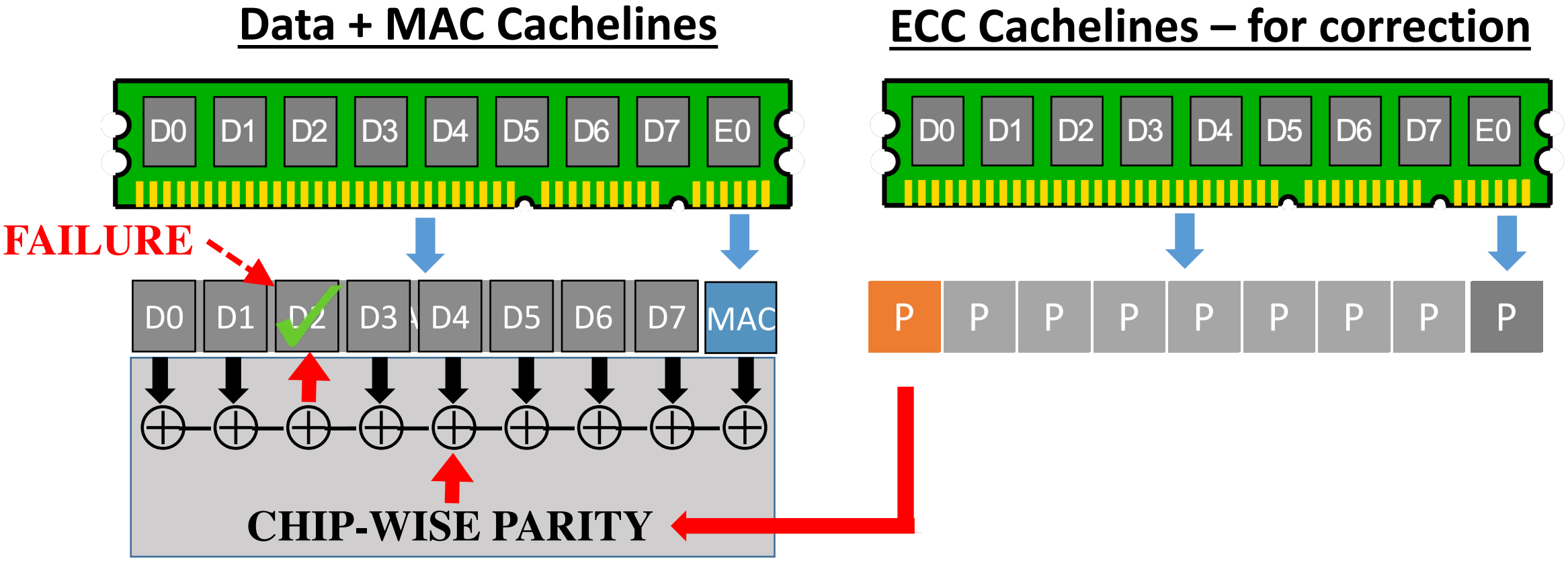
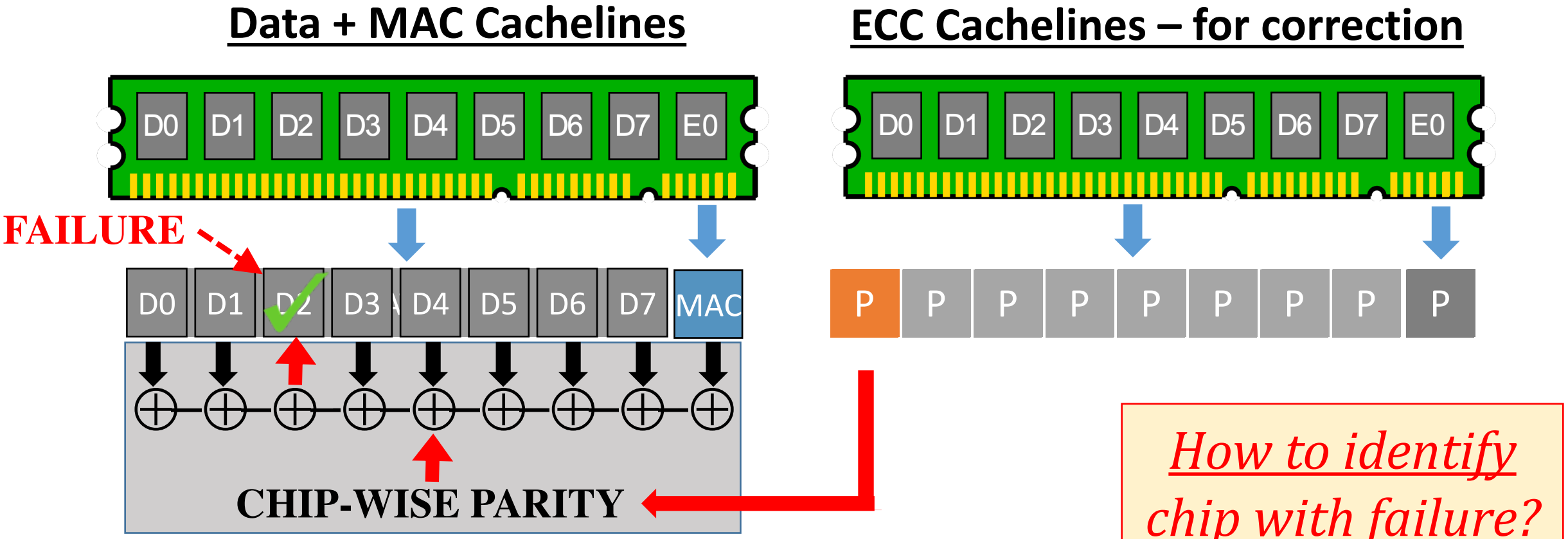


Parity Can Correct Large-Granularity Failures, If Chip With Failure Known

Parity Can Reconstruct Chip With Failure



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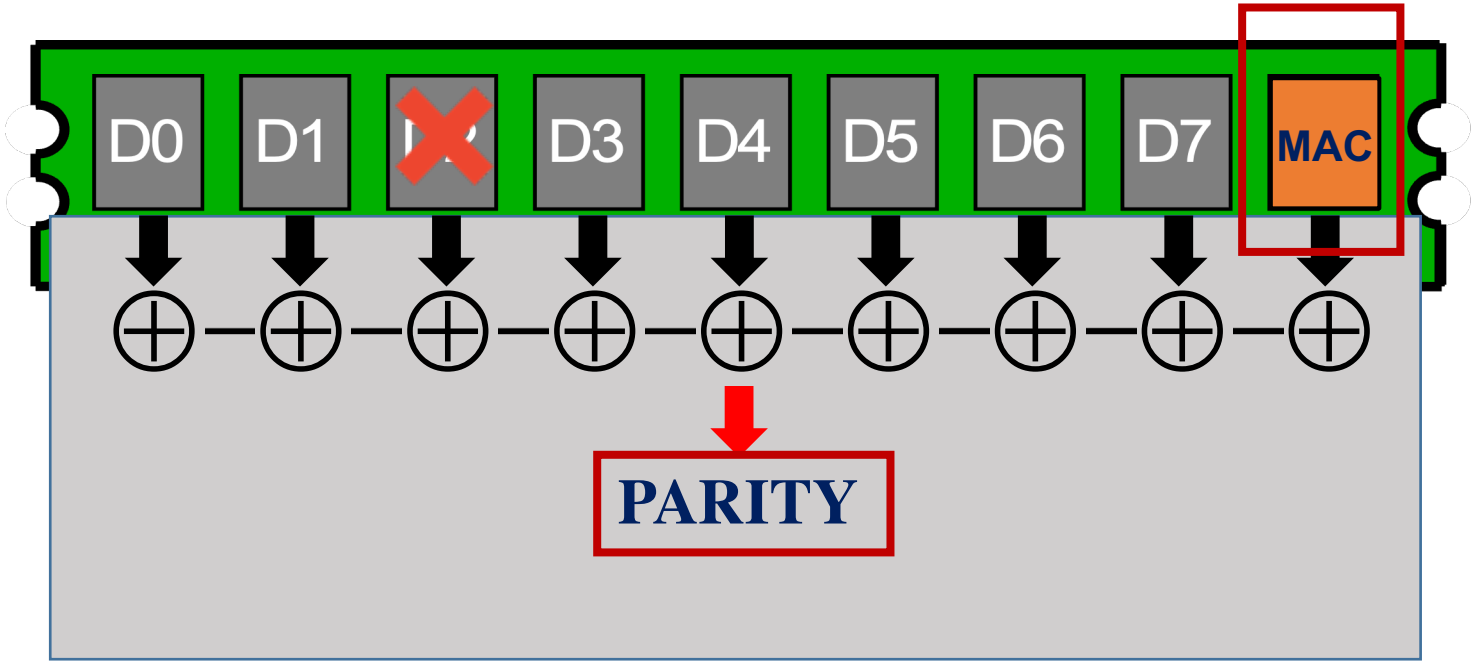
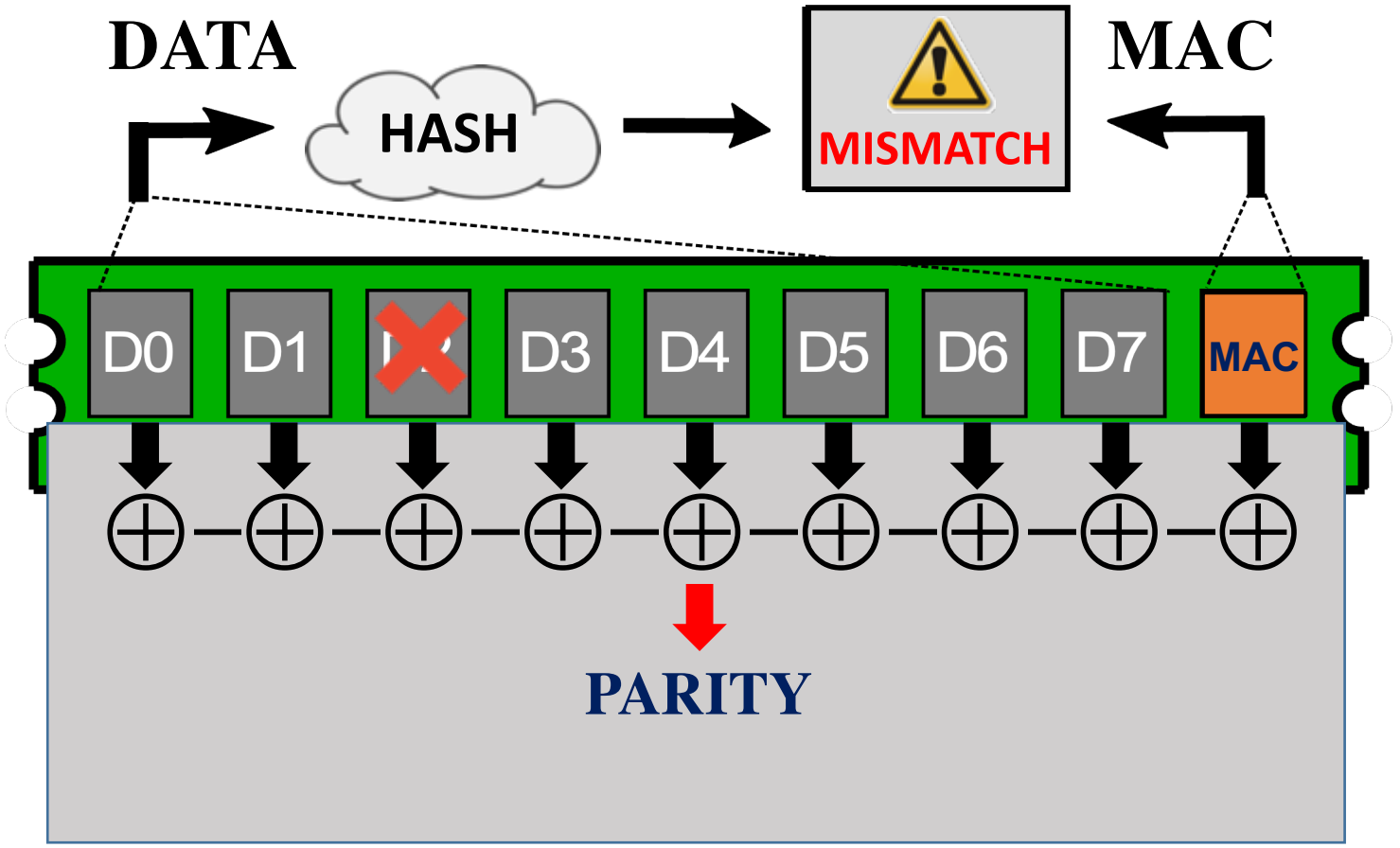


SYNERGY uses MAC + Parity for Error Correction

MAC can detect when data cacheline is free from error



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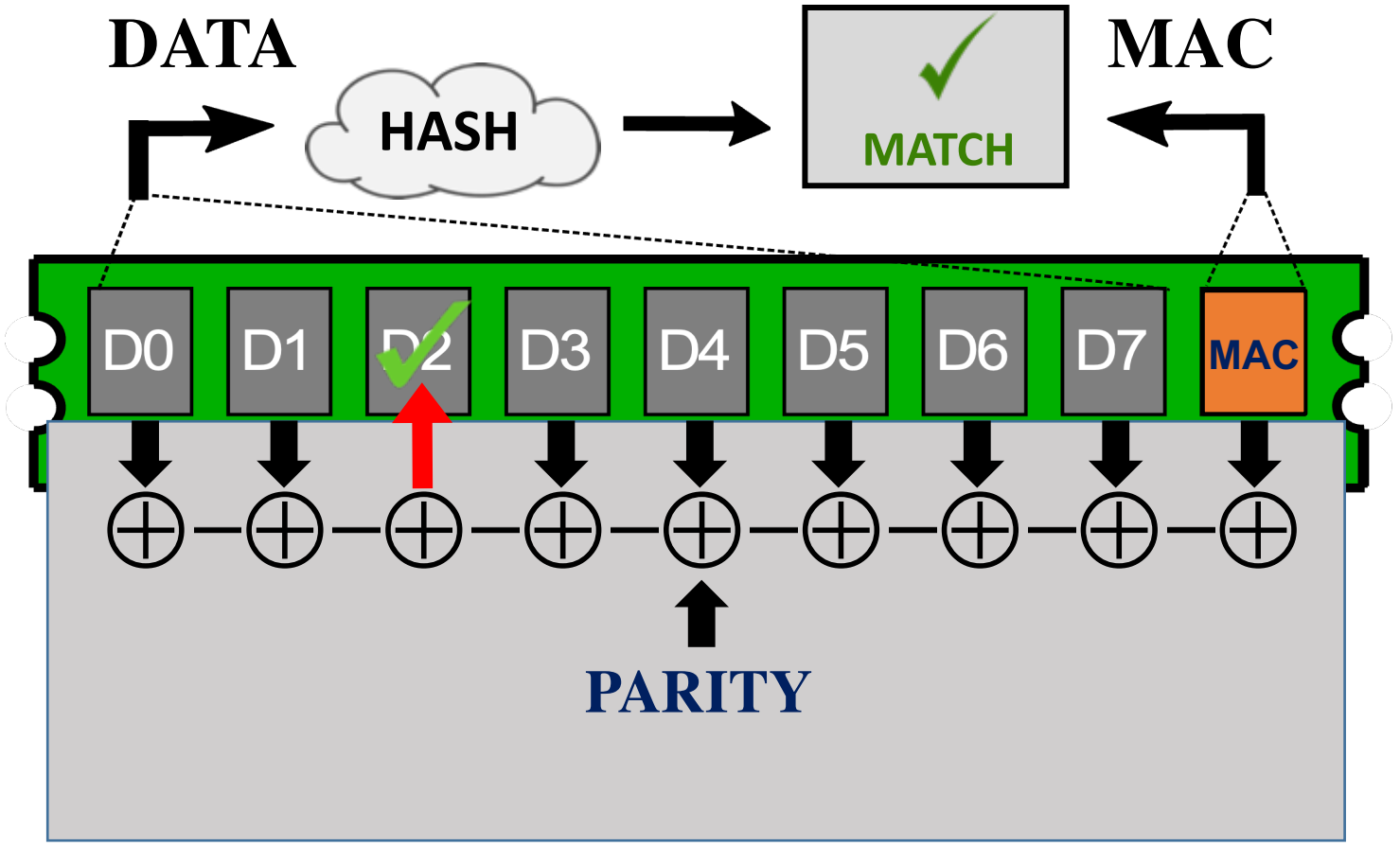

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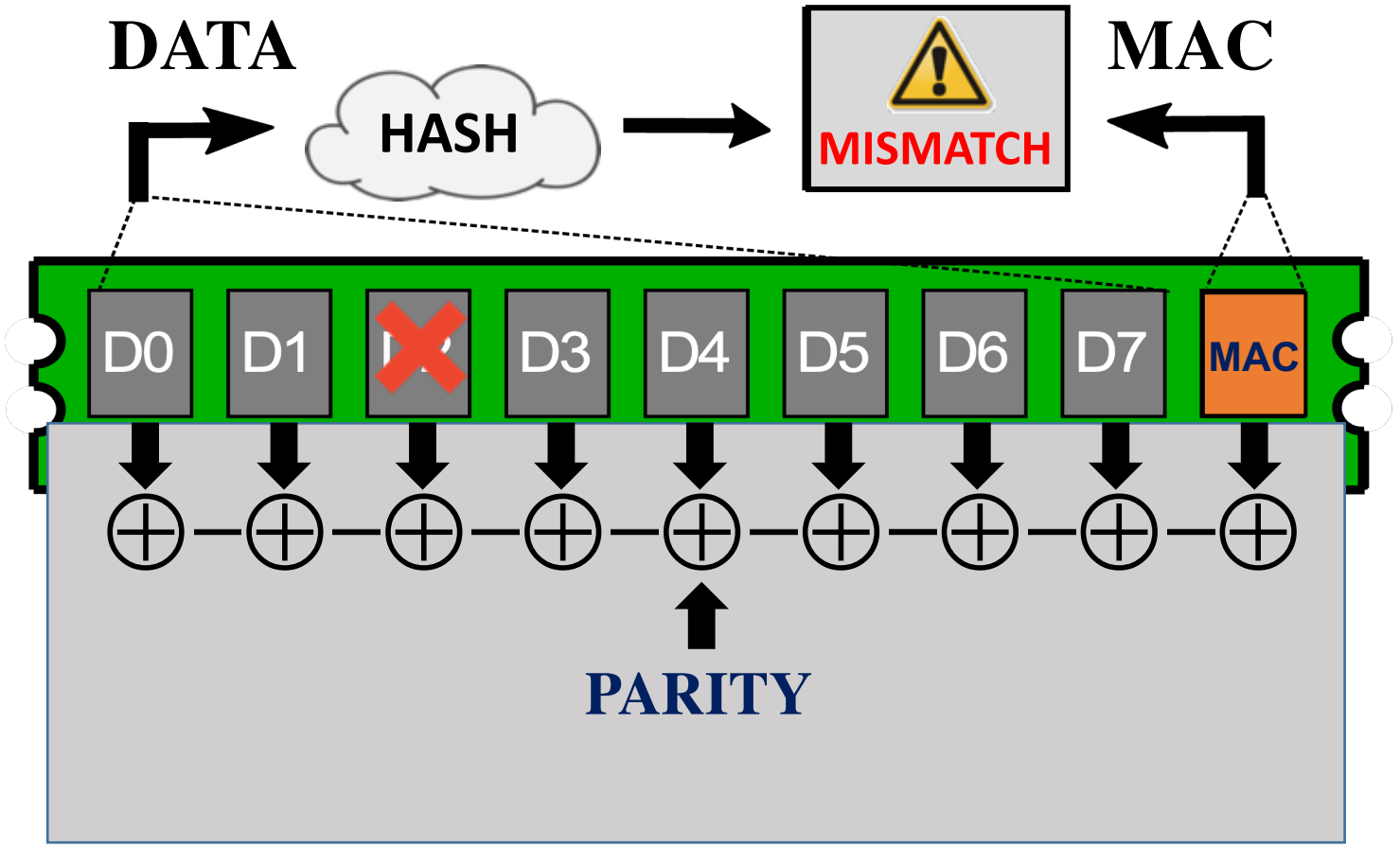

How to identify chip with failure?

SYNERGY uses MAC + Parity for Error Correction

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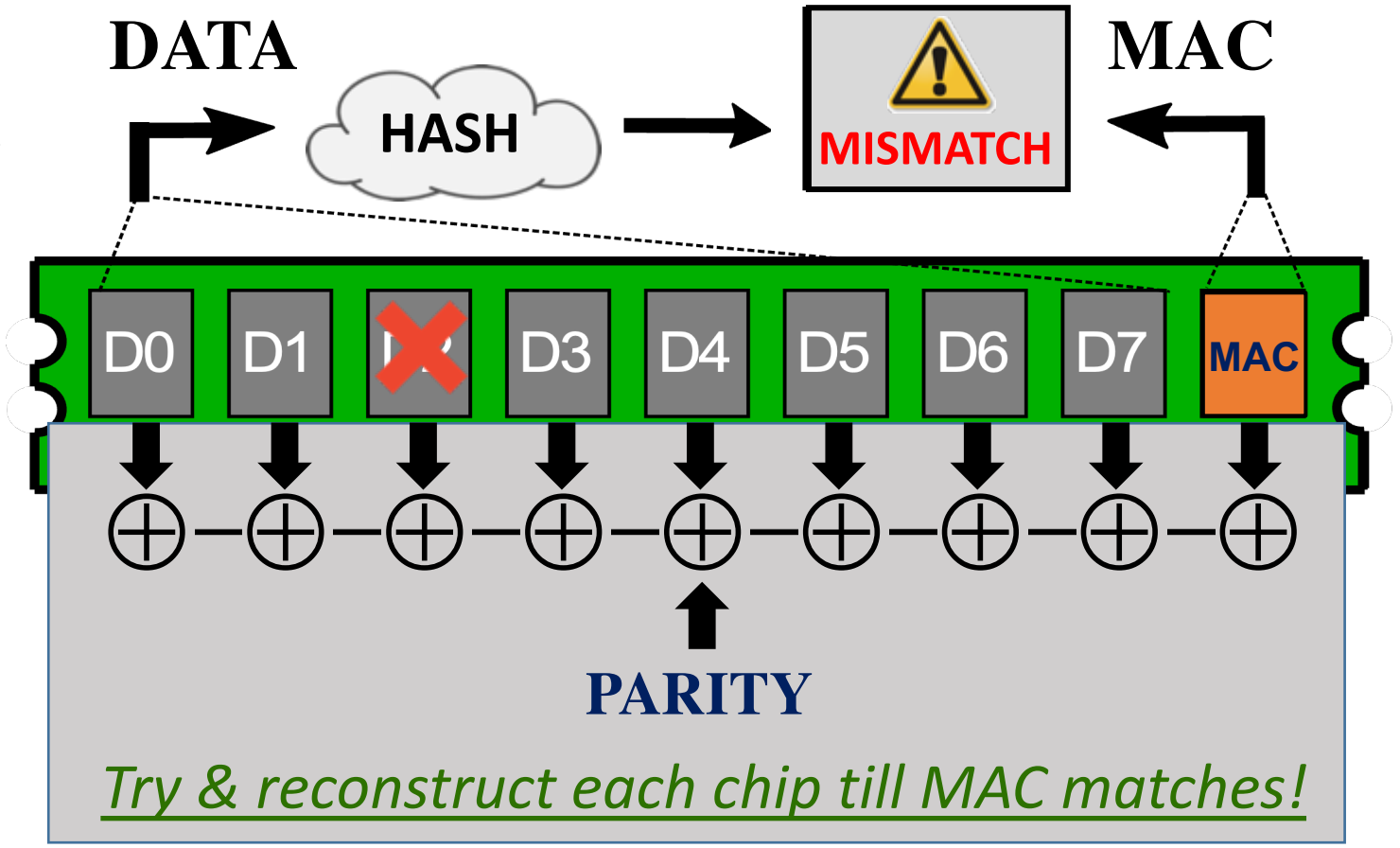

How to identify chip with failure?

Try & reconstruct each chip till MAC matches!

SYNERGY uses MAC + Parity for Error Correction

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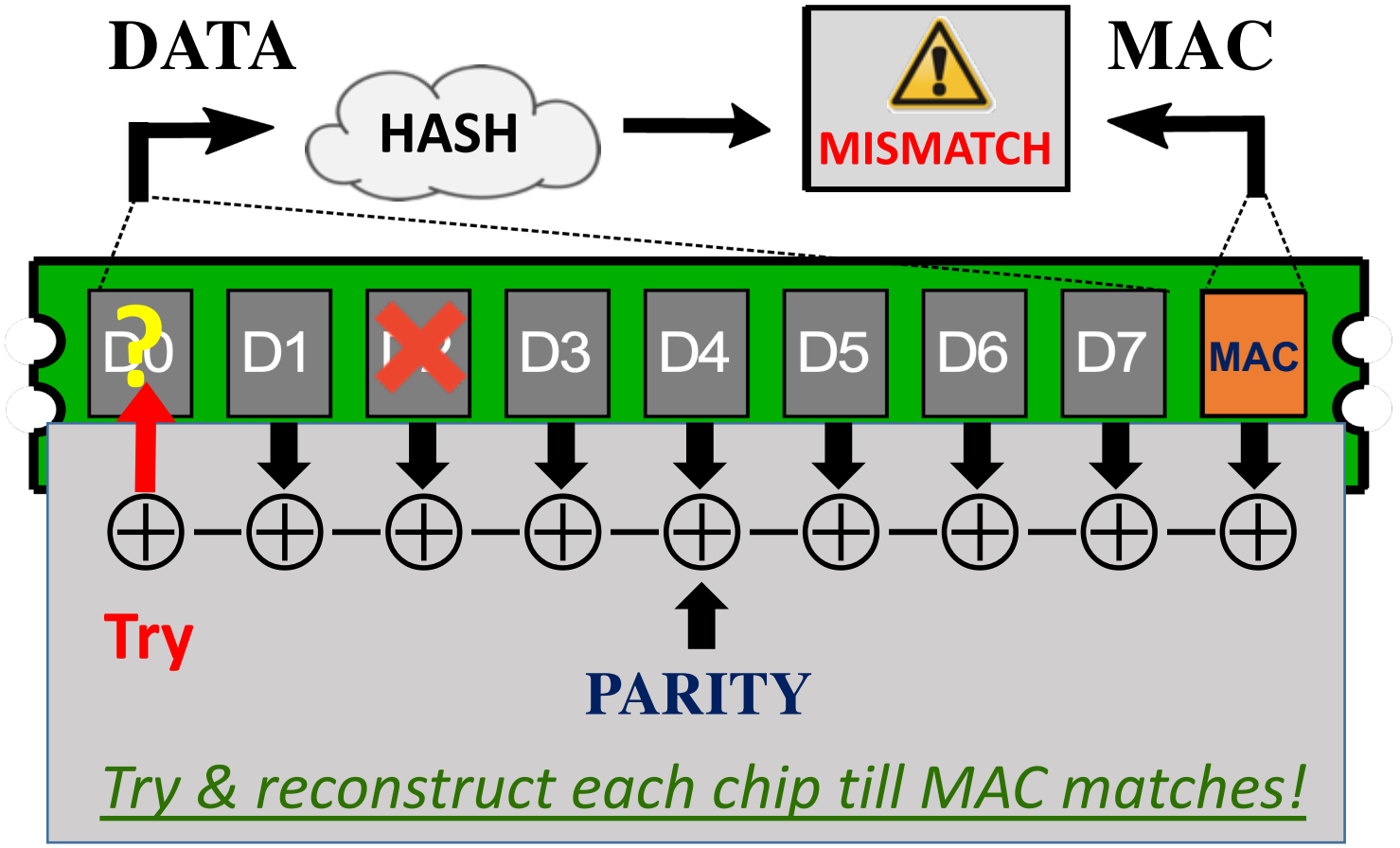

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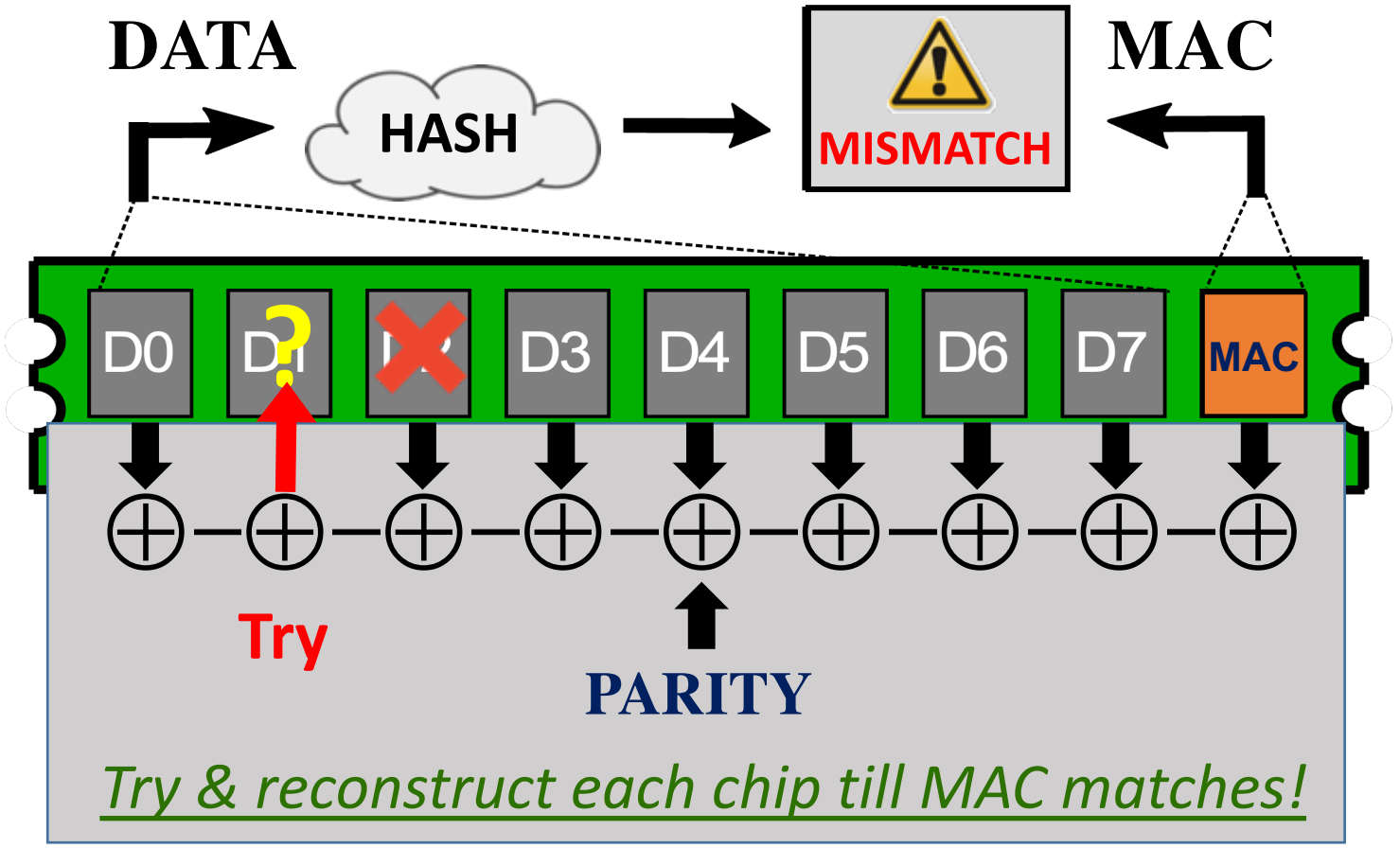

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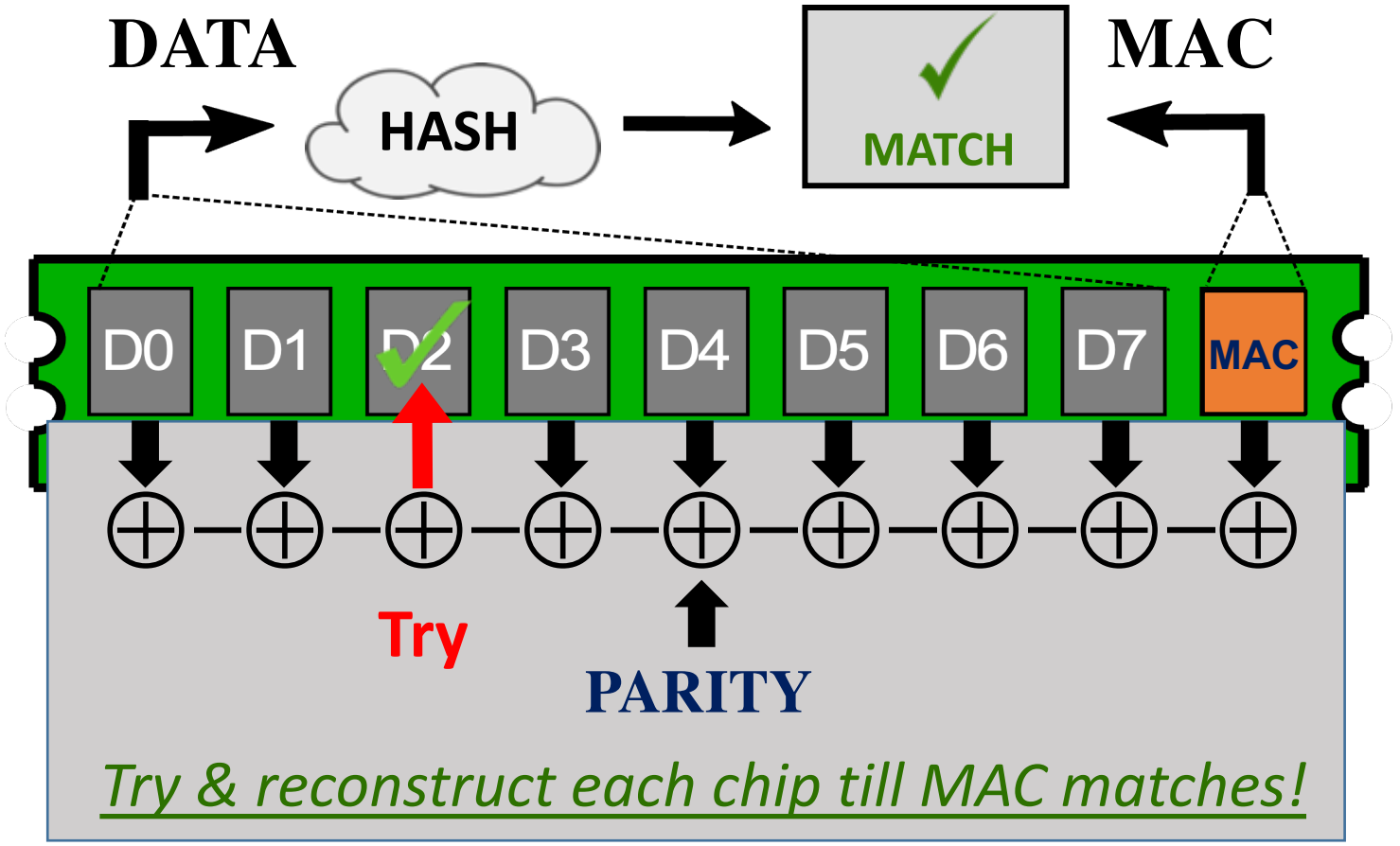

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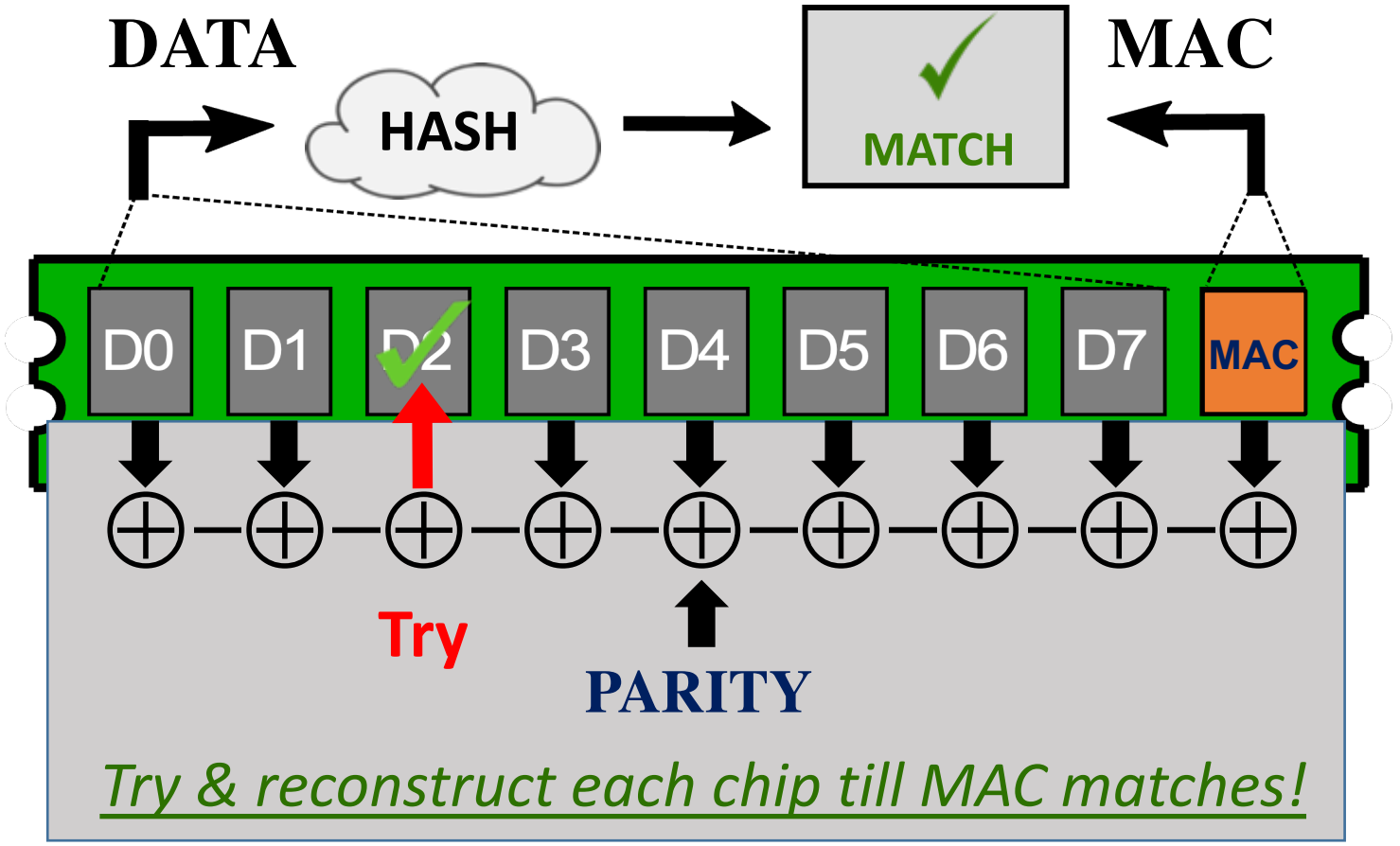
SYNERGY uses MAC + Parity for Error Correction

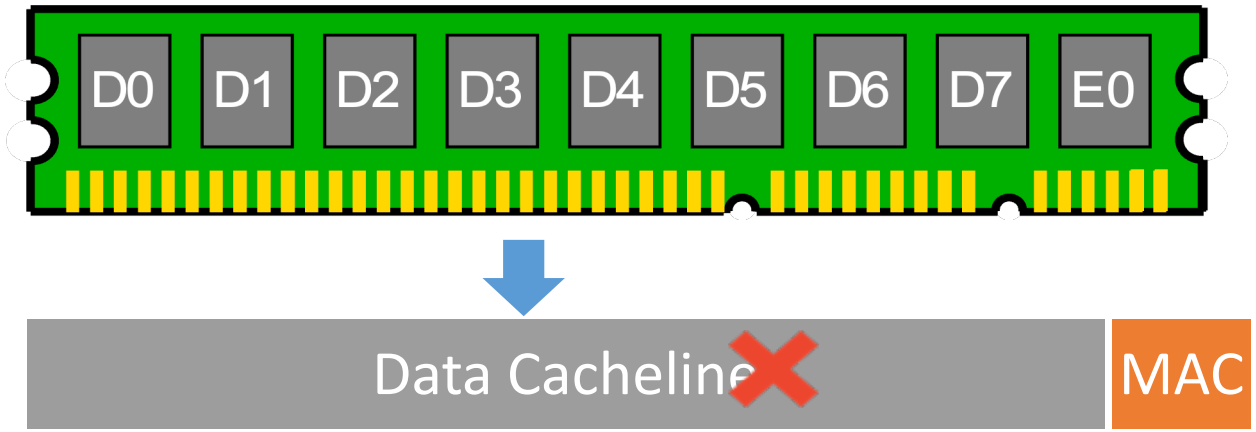
MAC can detect when data cacheline is free from error



How to identify chip with failure?

Synergy can tolerate 1 chip with failure out of 9 chips, much stronger reliability than SECDED (Baseline)

Tolerating Errors in Other Metadata



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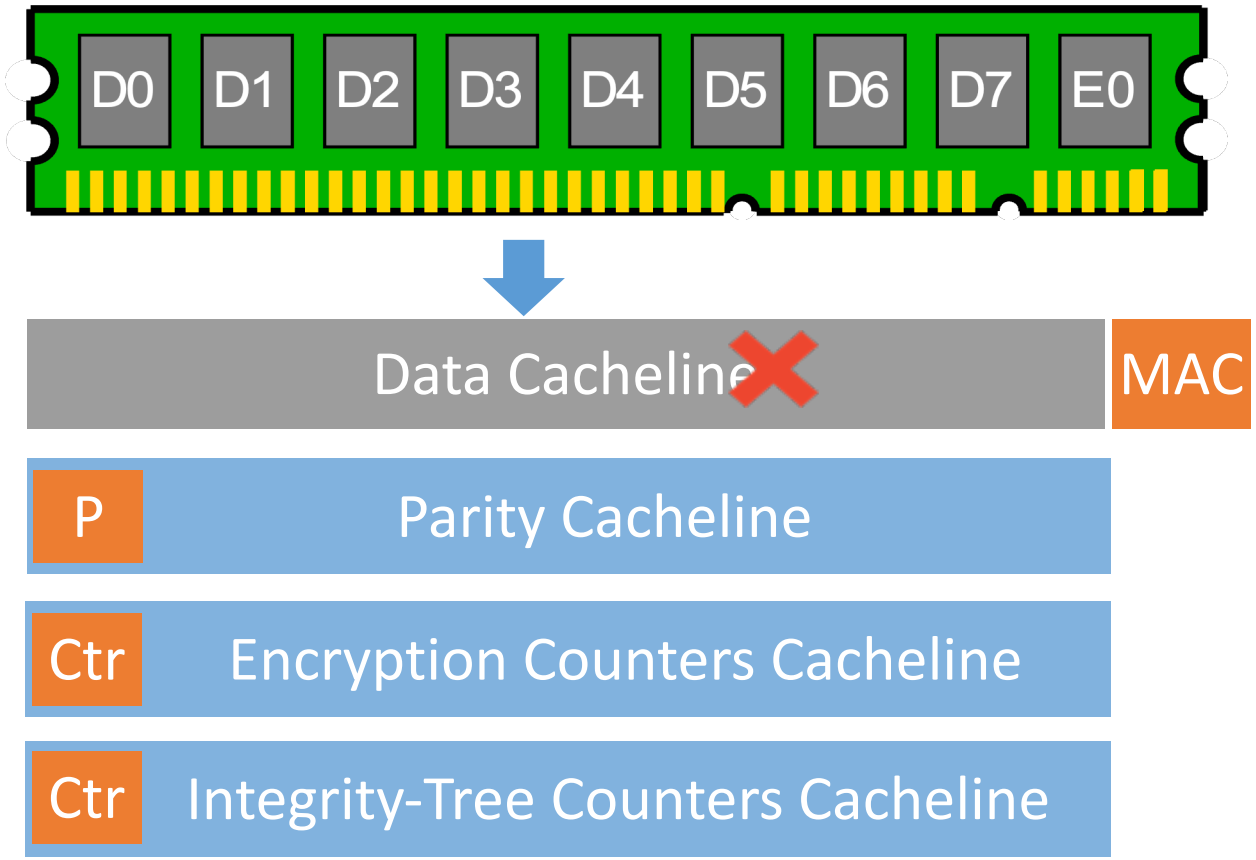

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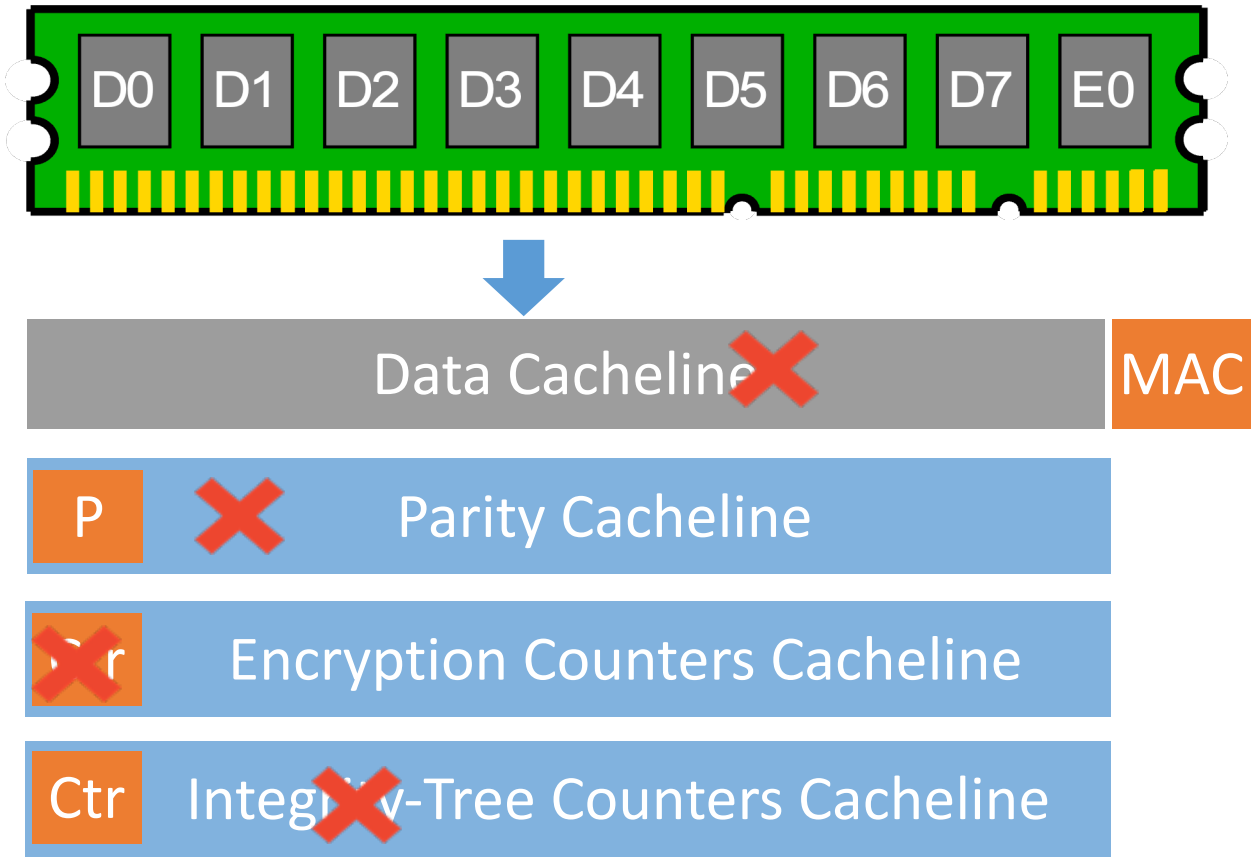
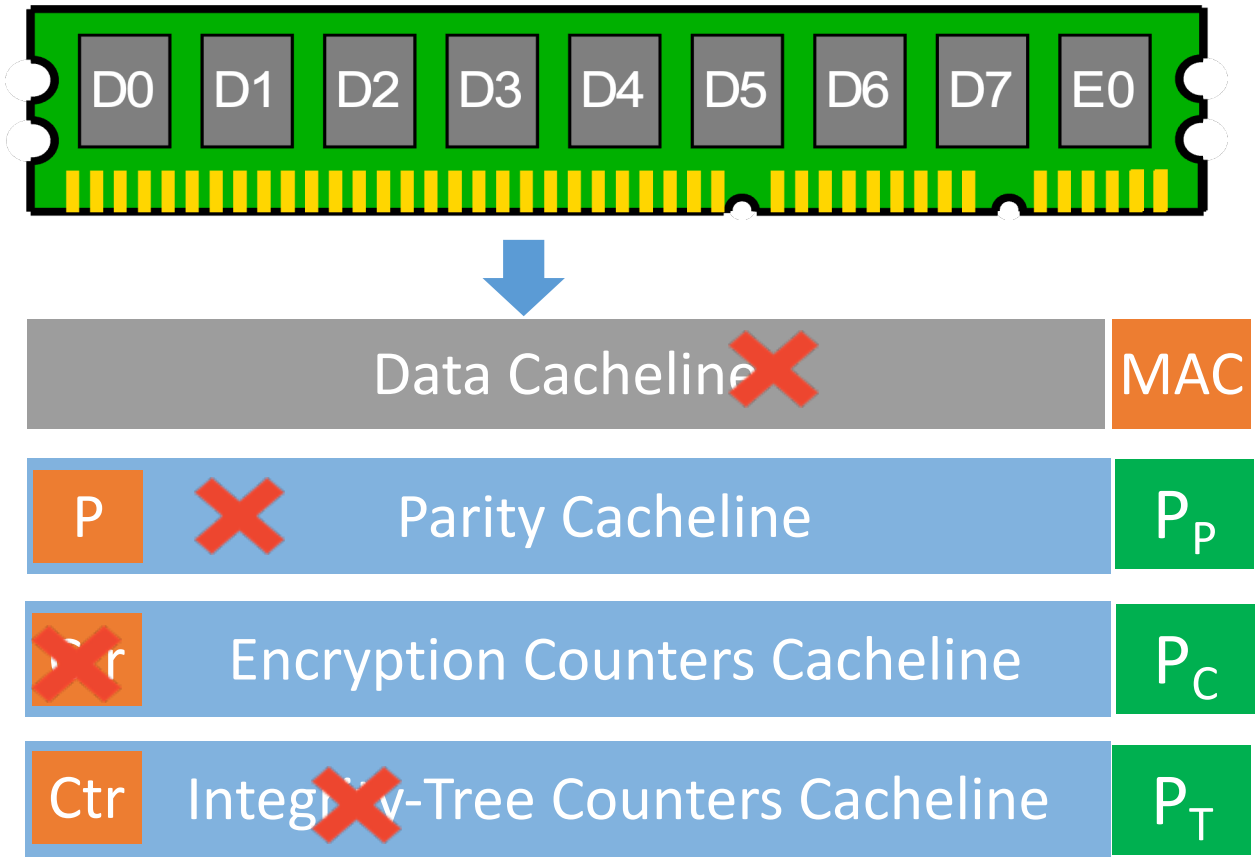


Errors can occur in any metadata stored in memory

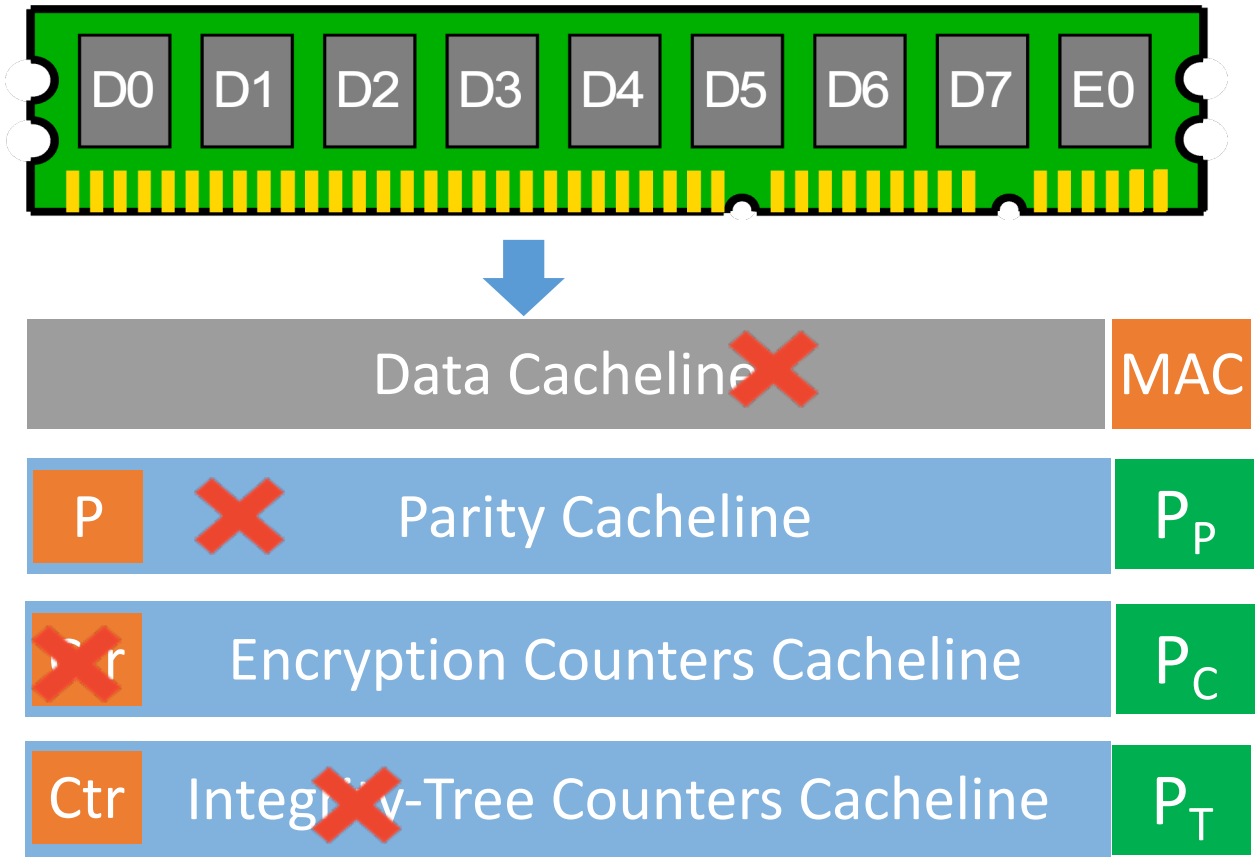
Tolerating Errors in Other Metadata



Errors can occur in any metadata stored in memory

SYNERGY stores Parity with each metadata to correct errors

Tolerating Errors in Other Metadata



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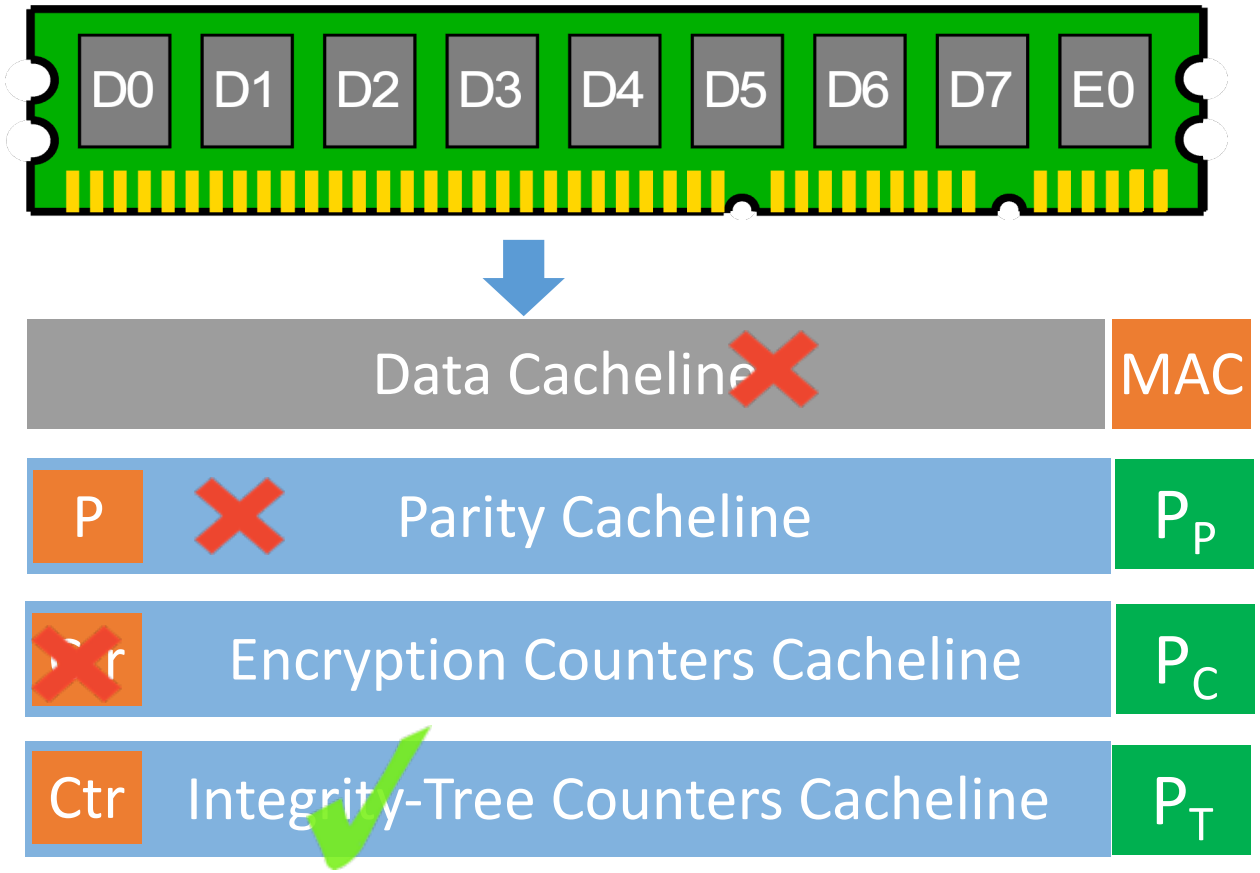
Level-wise Error Correction Algorithm

Tolerating Errors in Other Metadata



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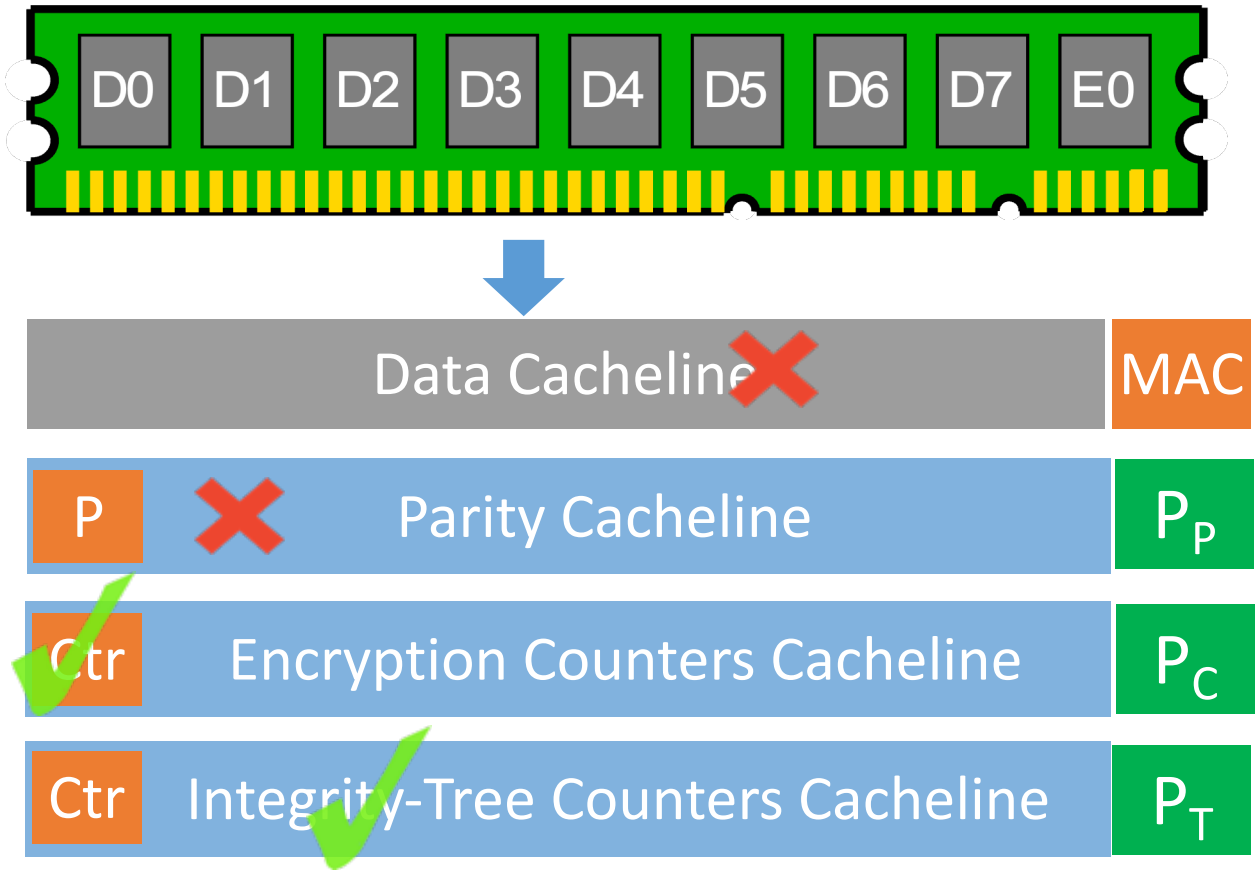

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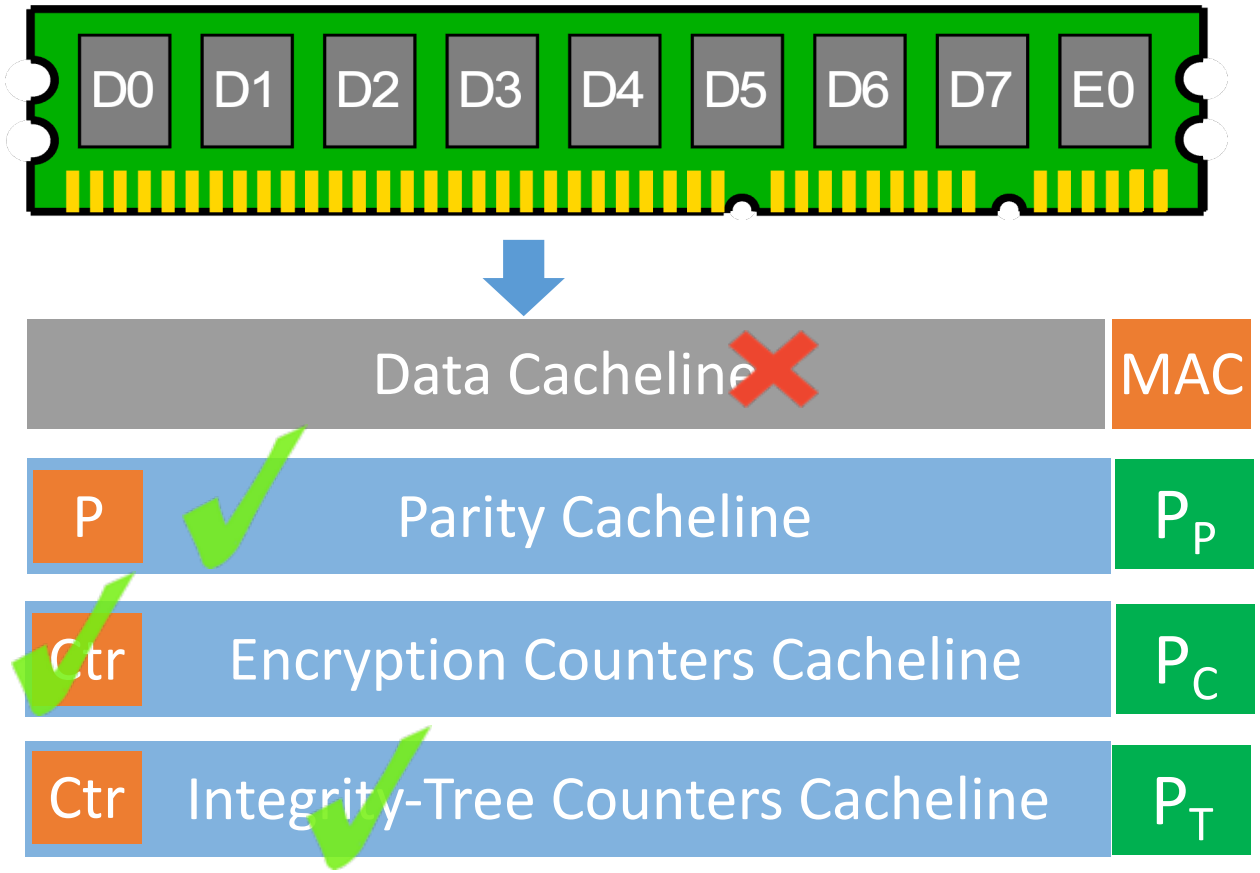

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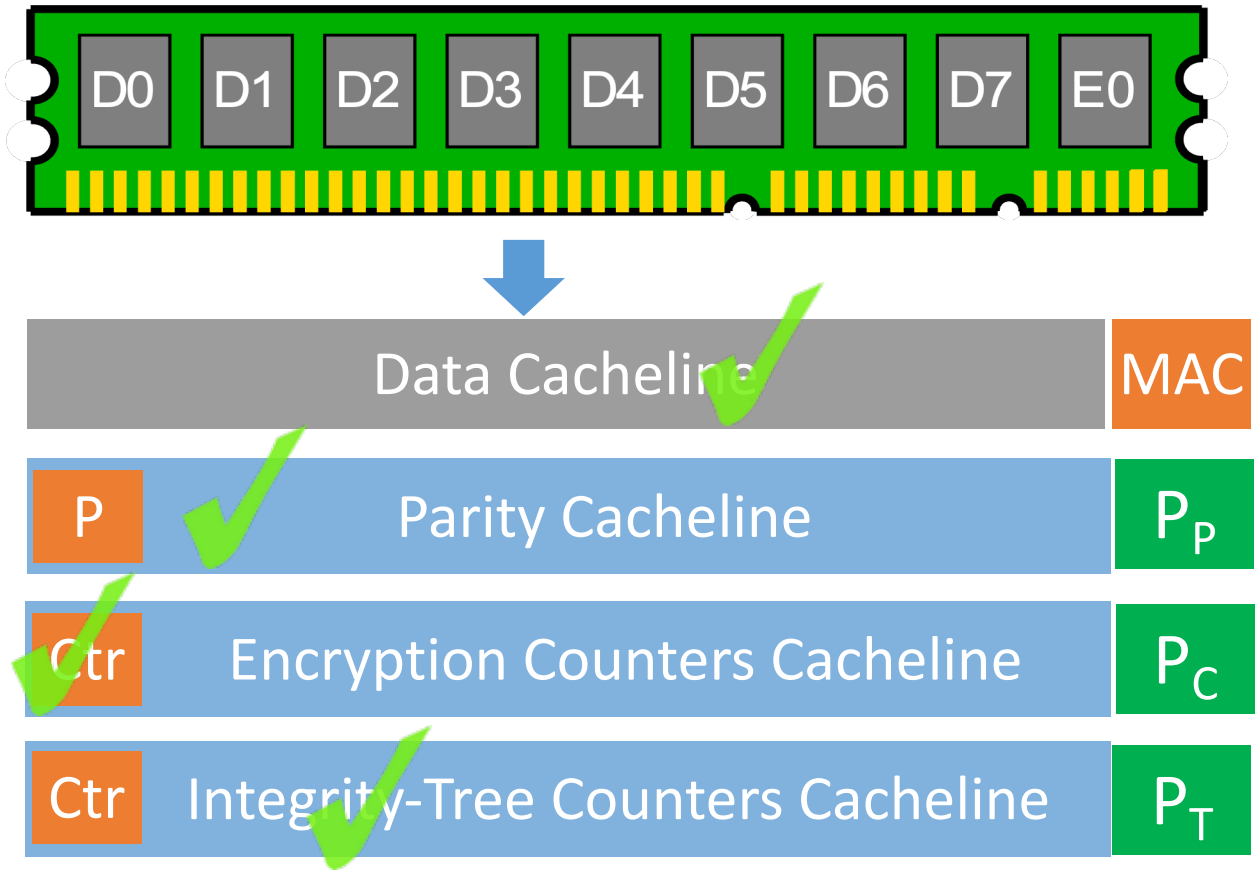


Errors can occur in any metadata stored in memory

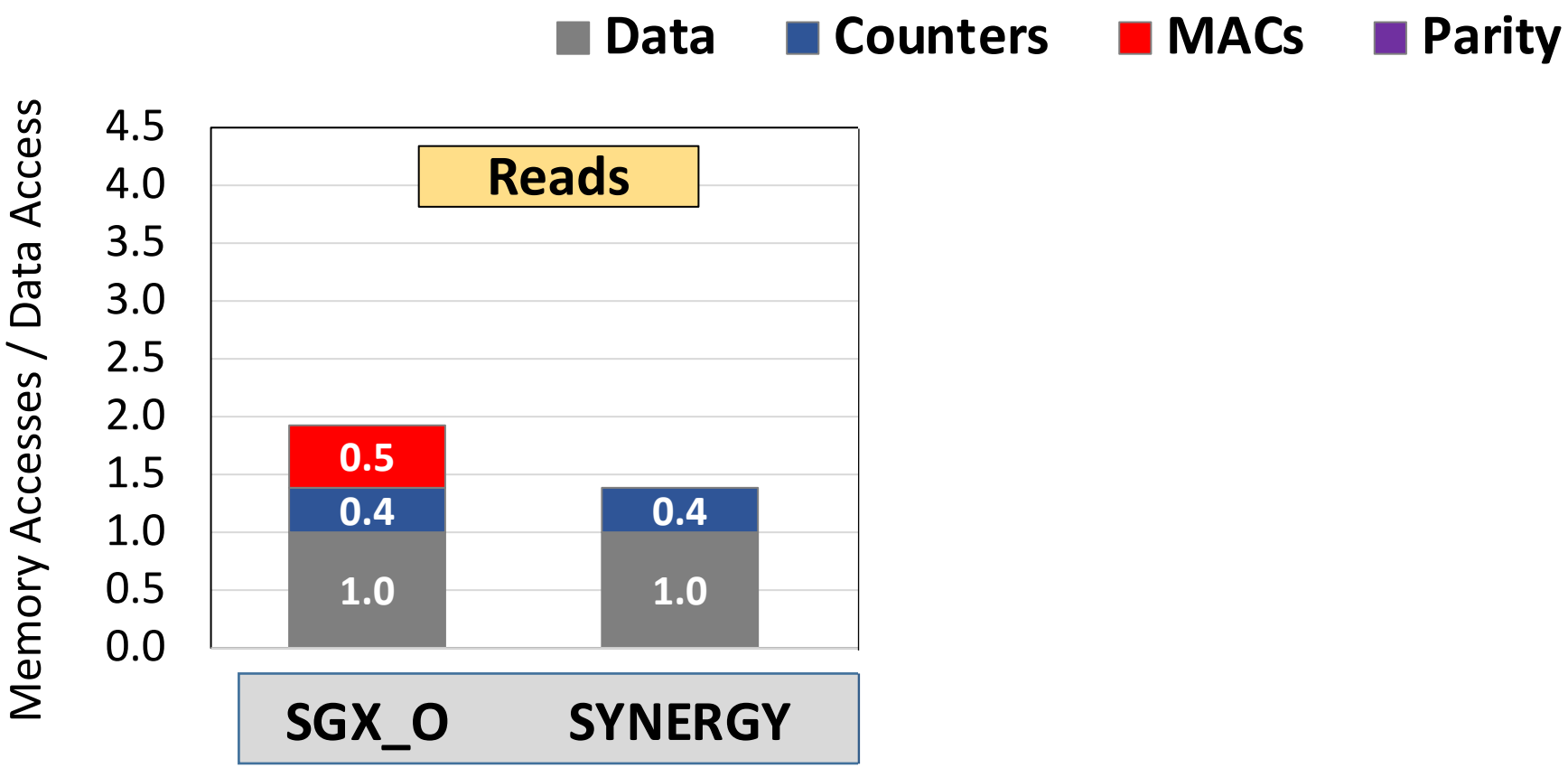
SYNERGY stores Parity with each metadata to correct errors

Level-wise Error Correction Algorithm

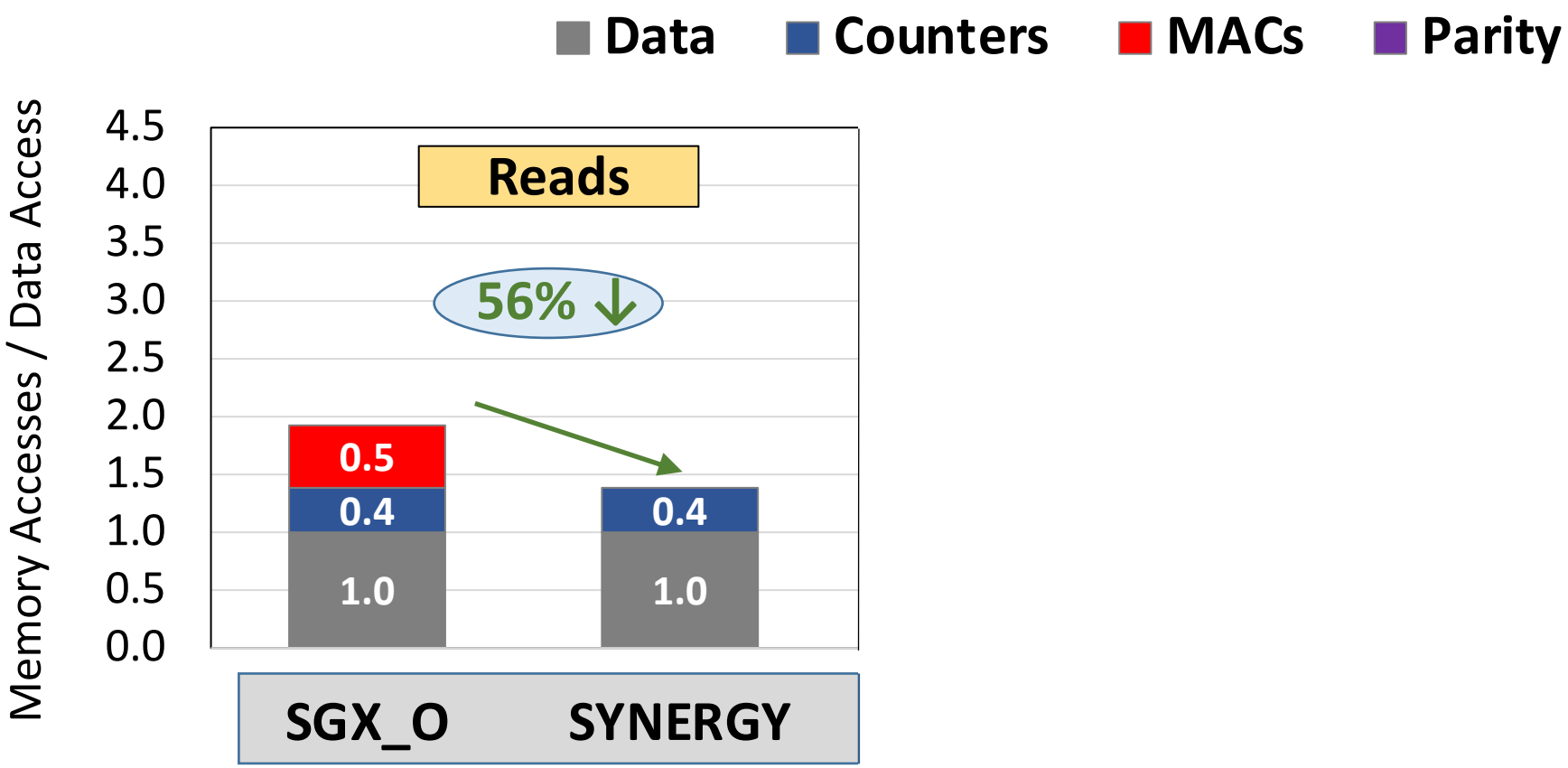
Agenda

- Introduction & Background
- Synergy Design
- **Evaluation**

Benefit-1: Reduced Memory Traffic



Benefit-1: Reduced Memory Traffic



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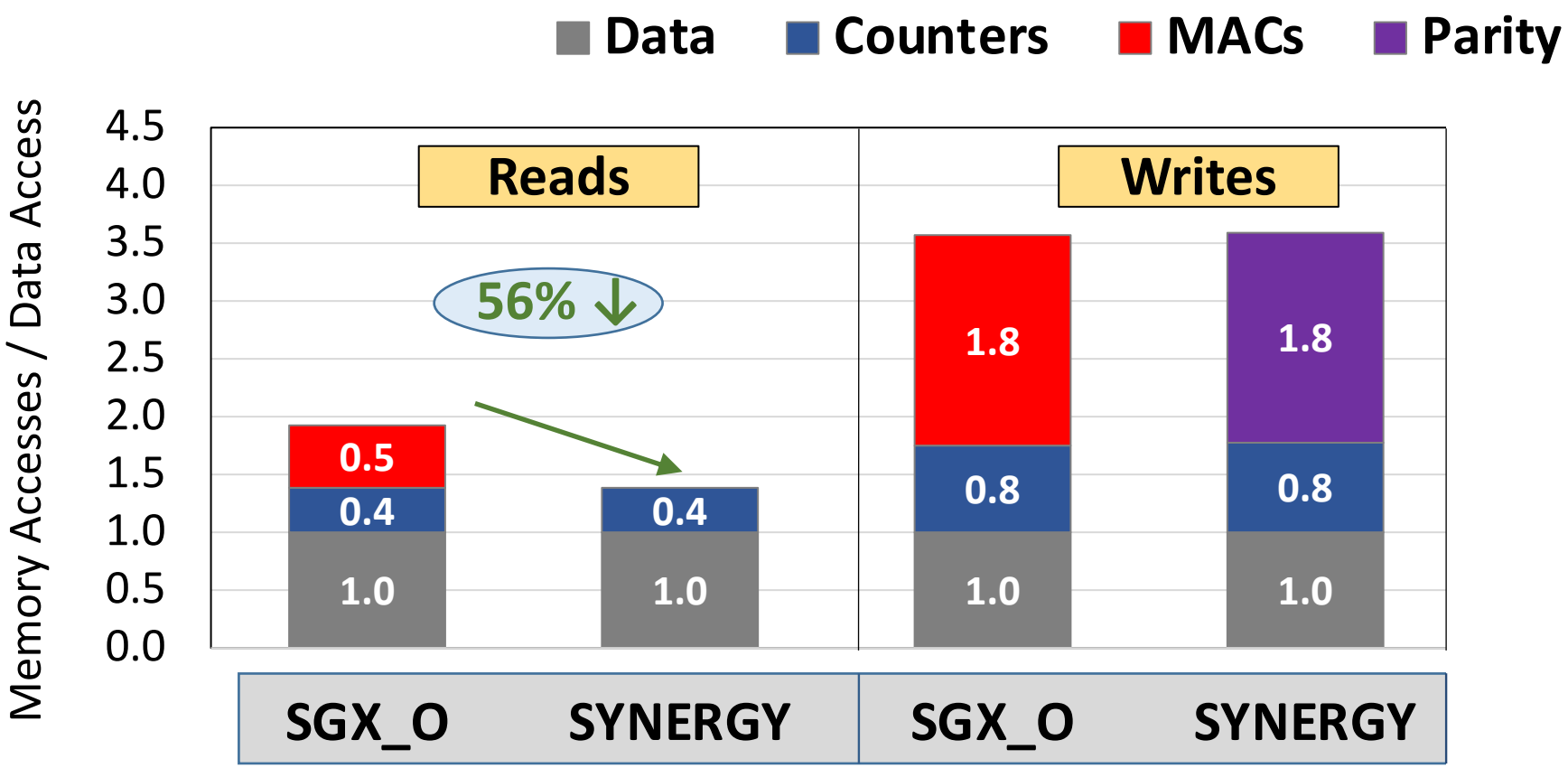

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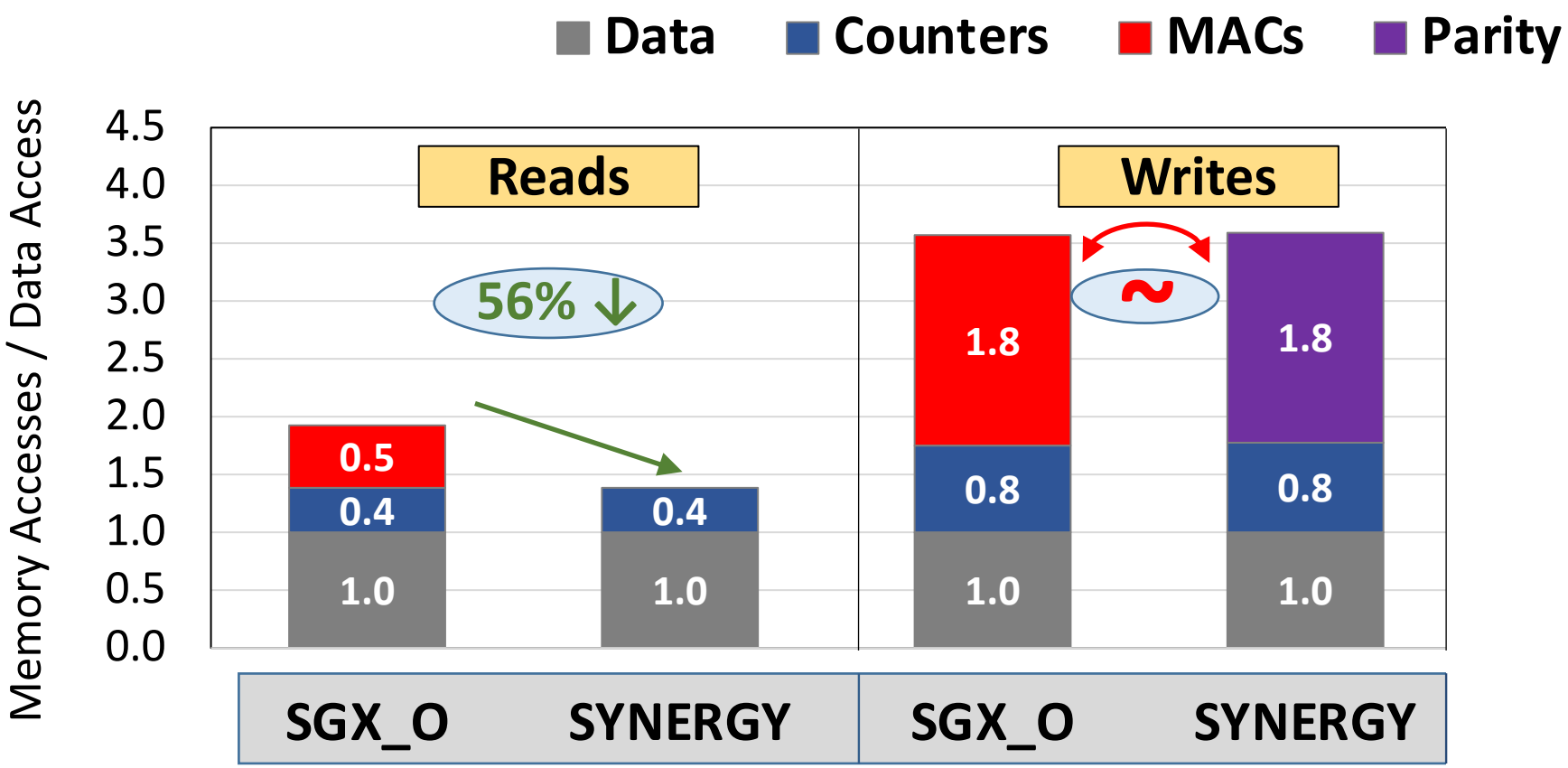

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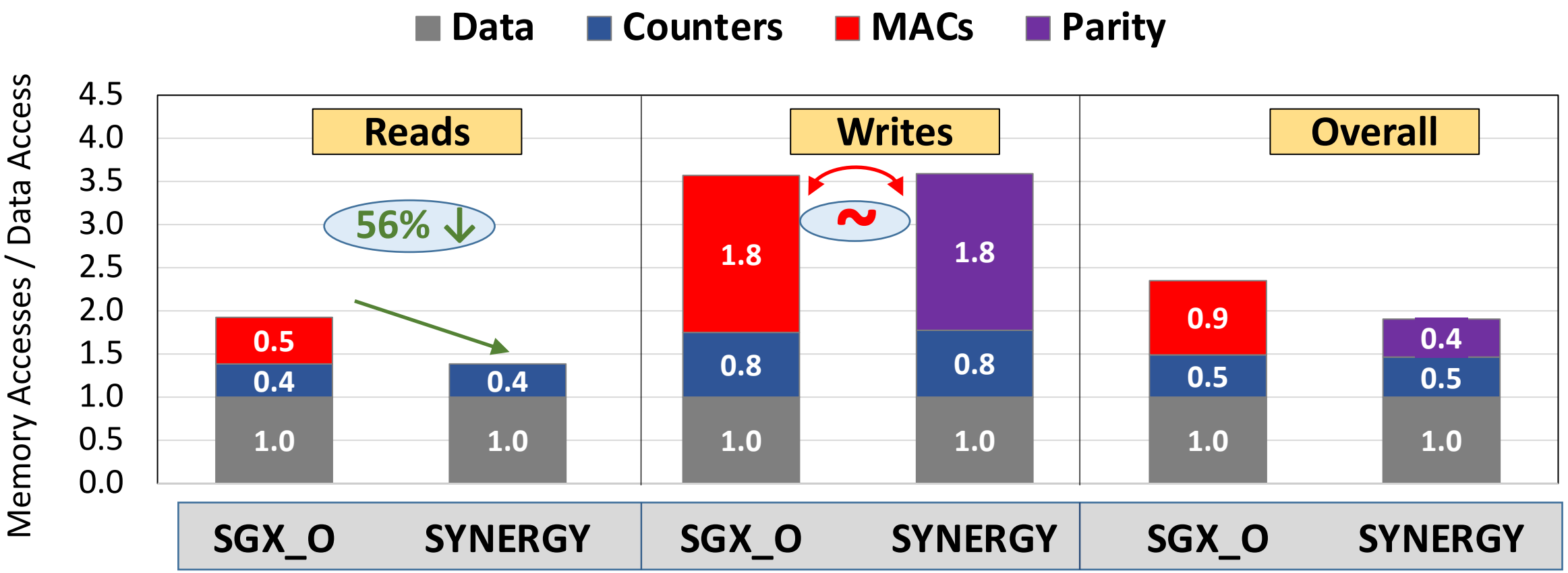

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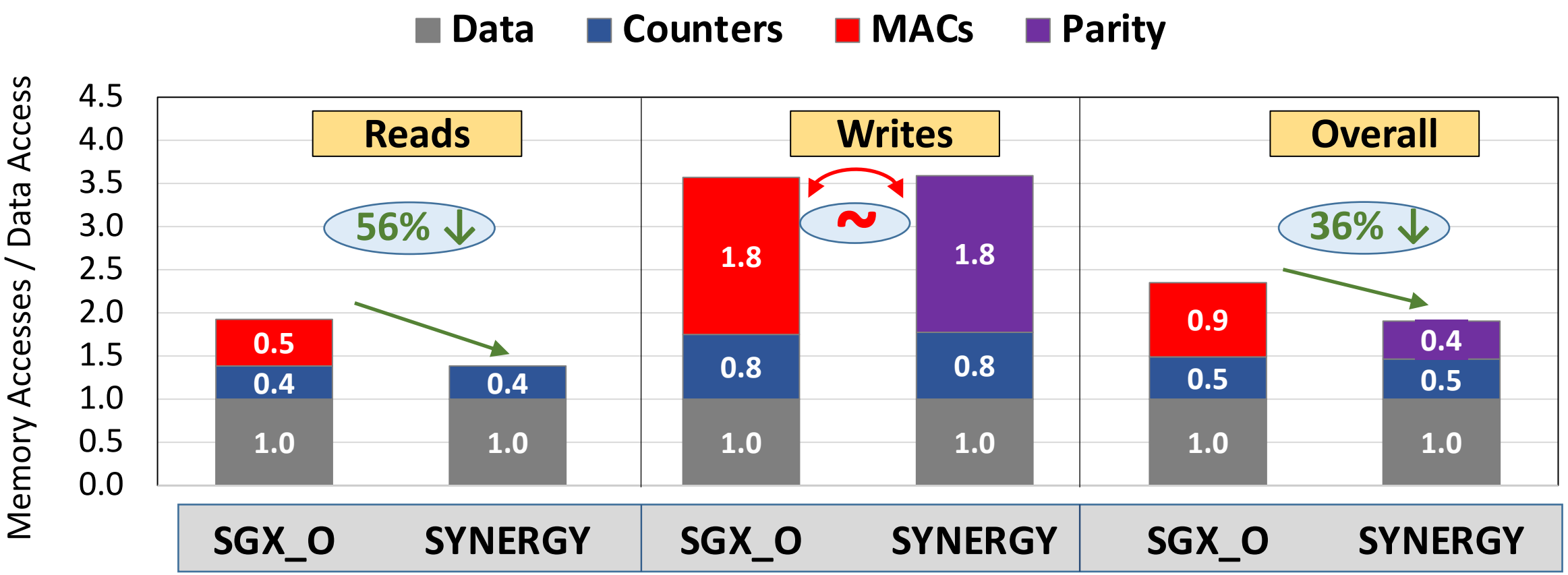

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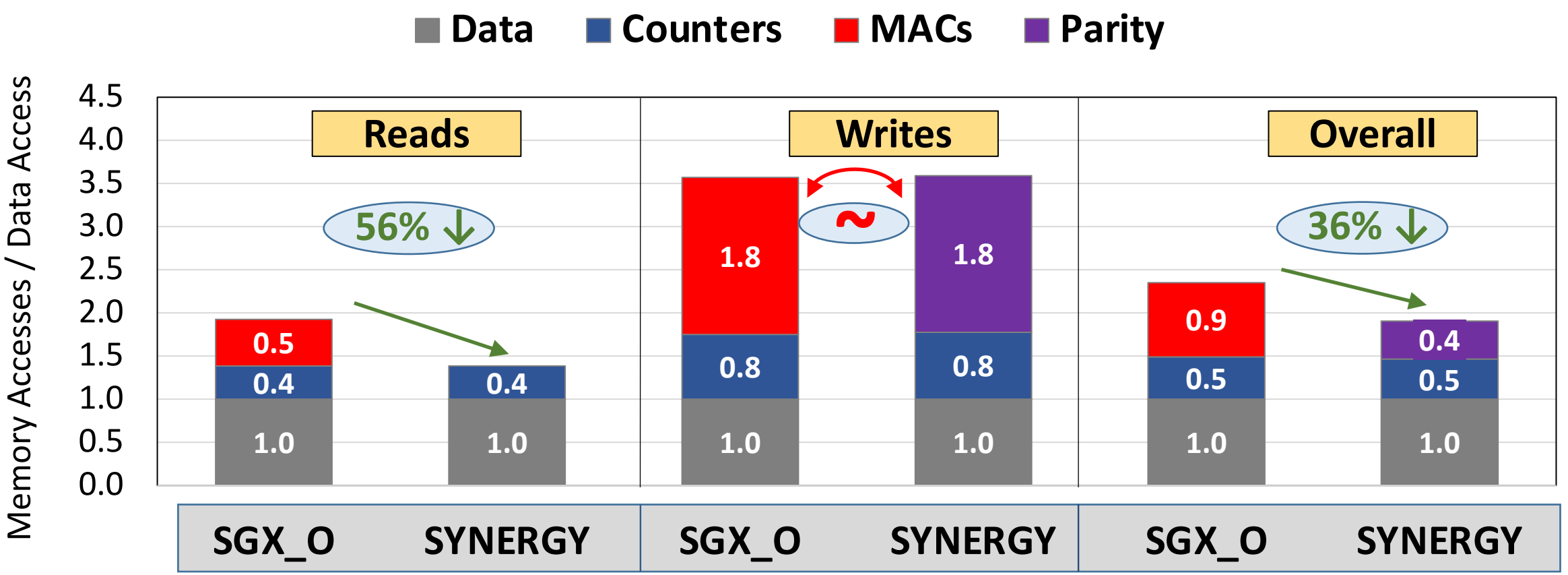
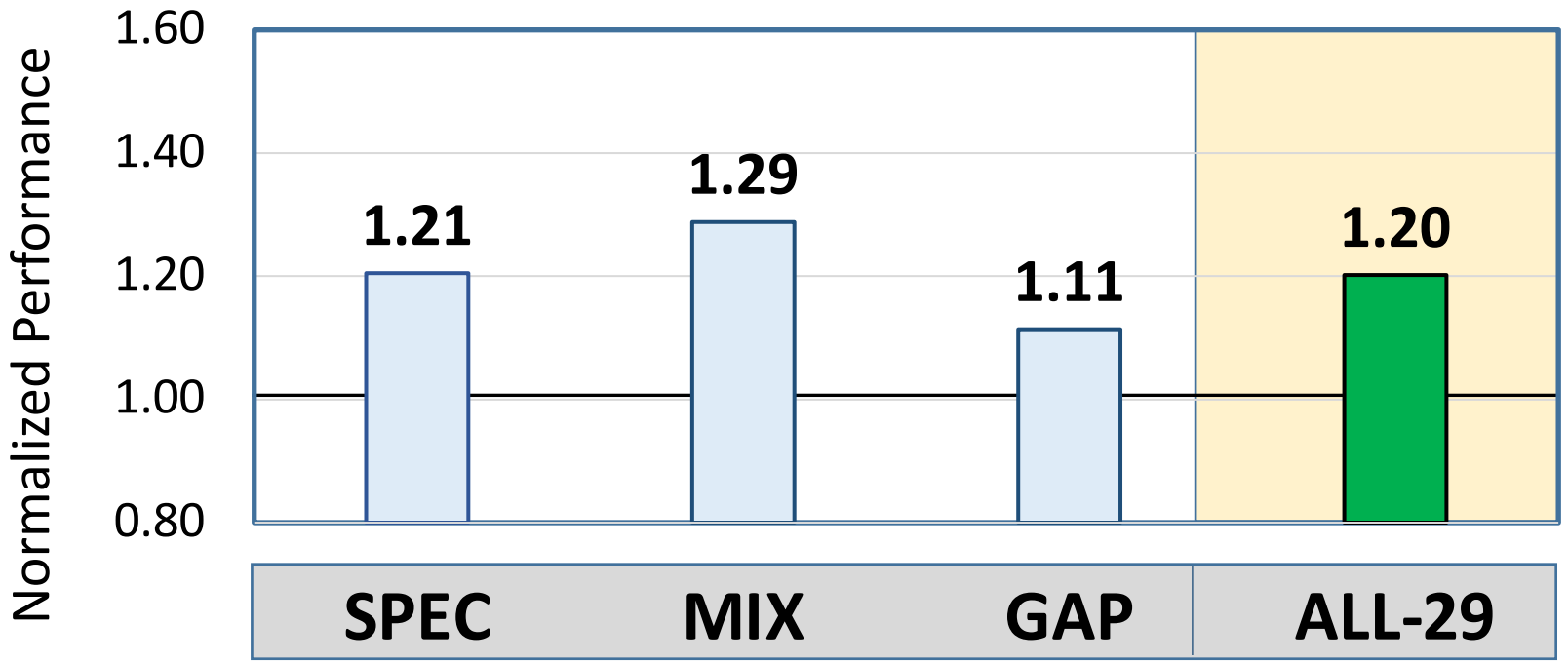


SYNERGY Reduces Metadata Accesses by 36%

Benefit-2: Better Performance

Performance of SYNERGY normalized to SGX_O



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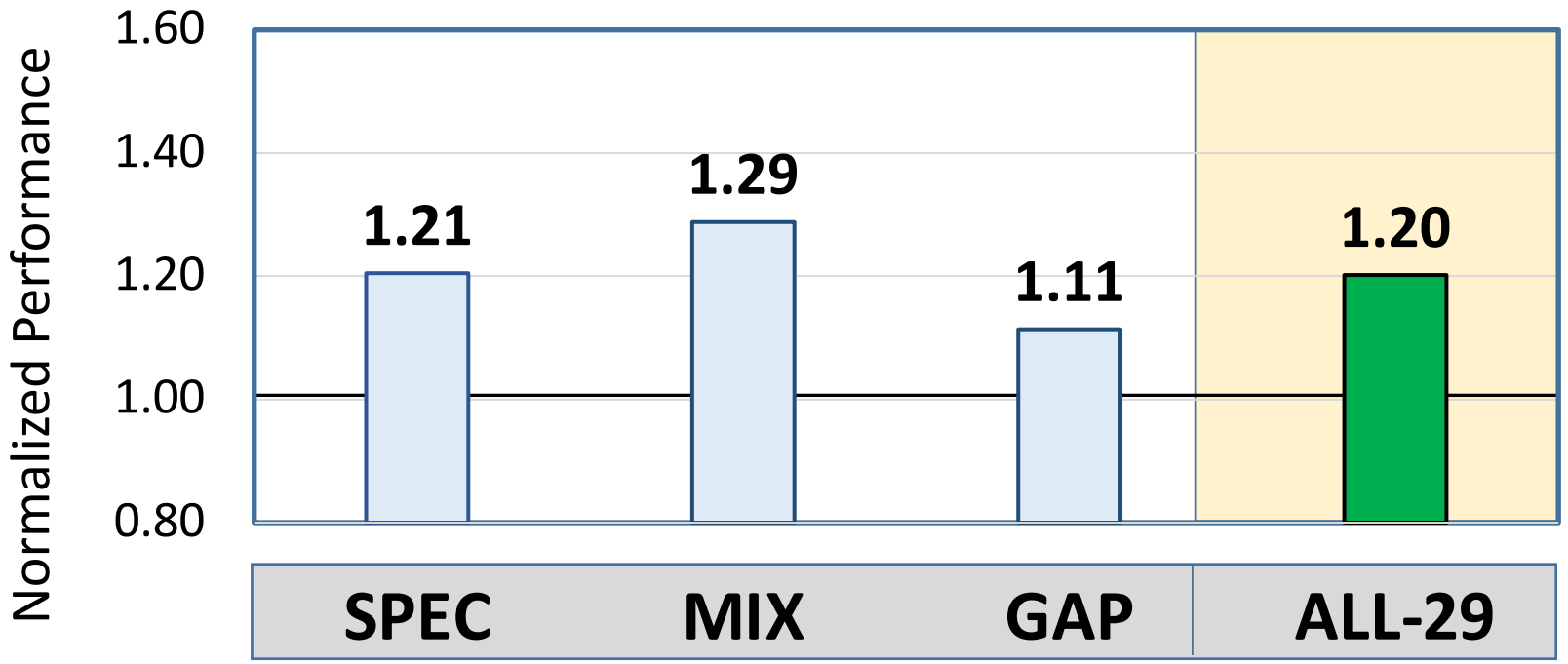
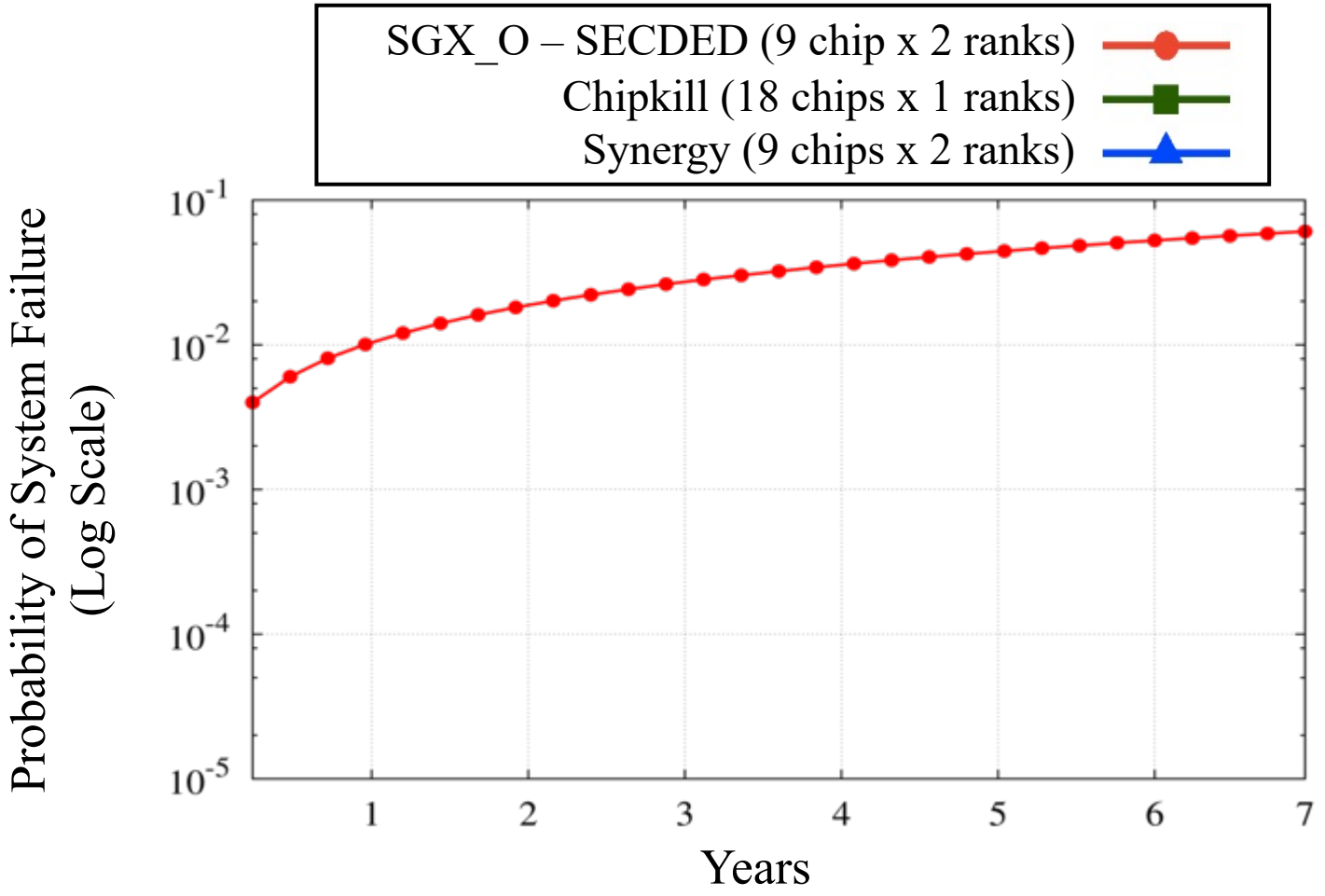
Performance of SYNERGY normalized to SGX_O



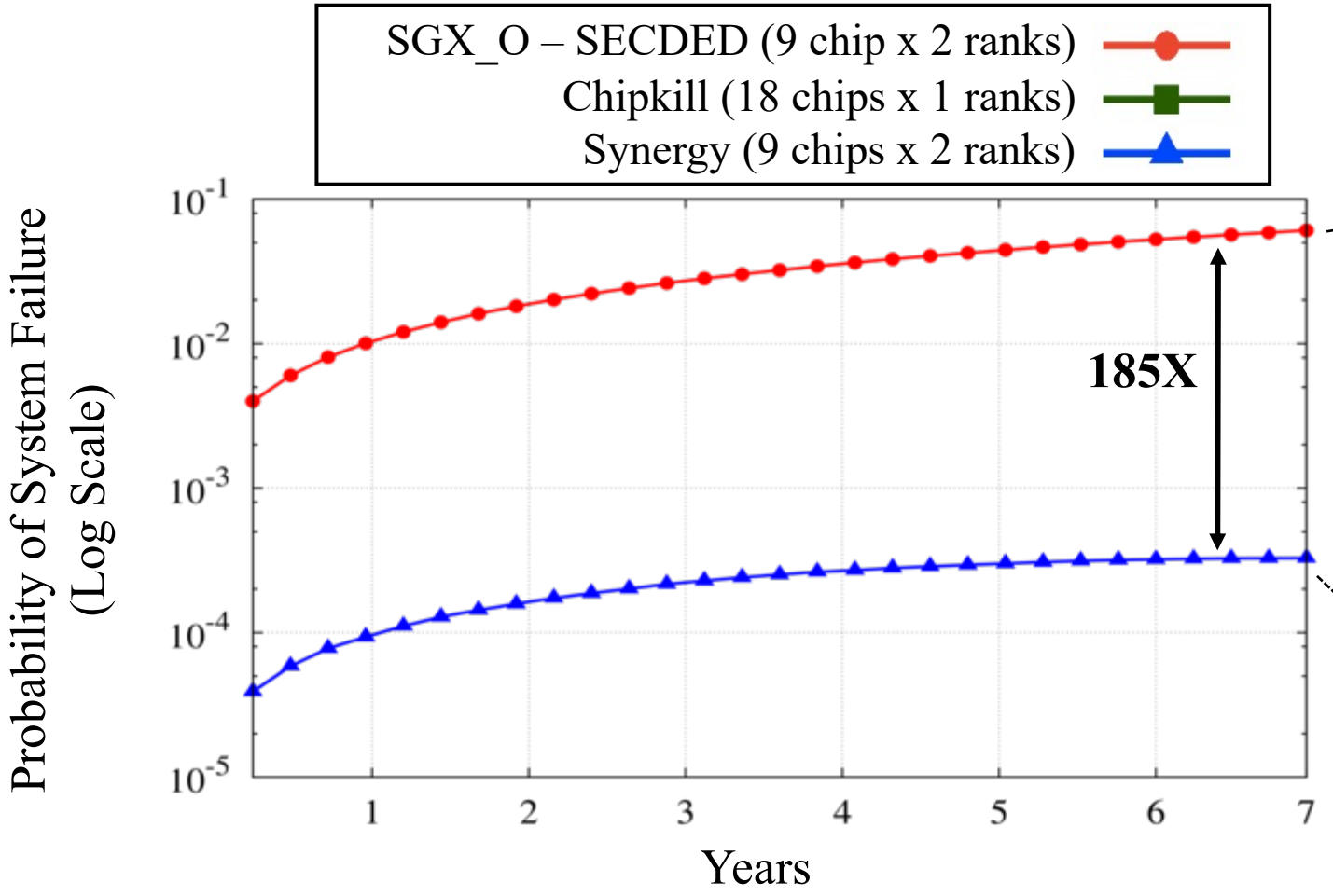
SYNERGY improves performance of secure memory by 20%, without any additional storage

Benefit-3: Stronger Reliability



SECDED only tolerates single-bit errors

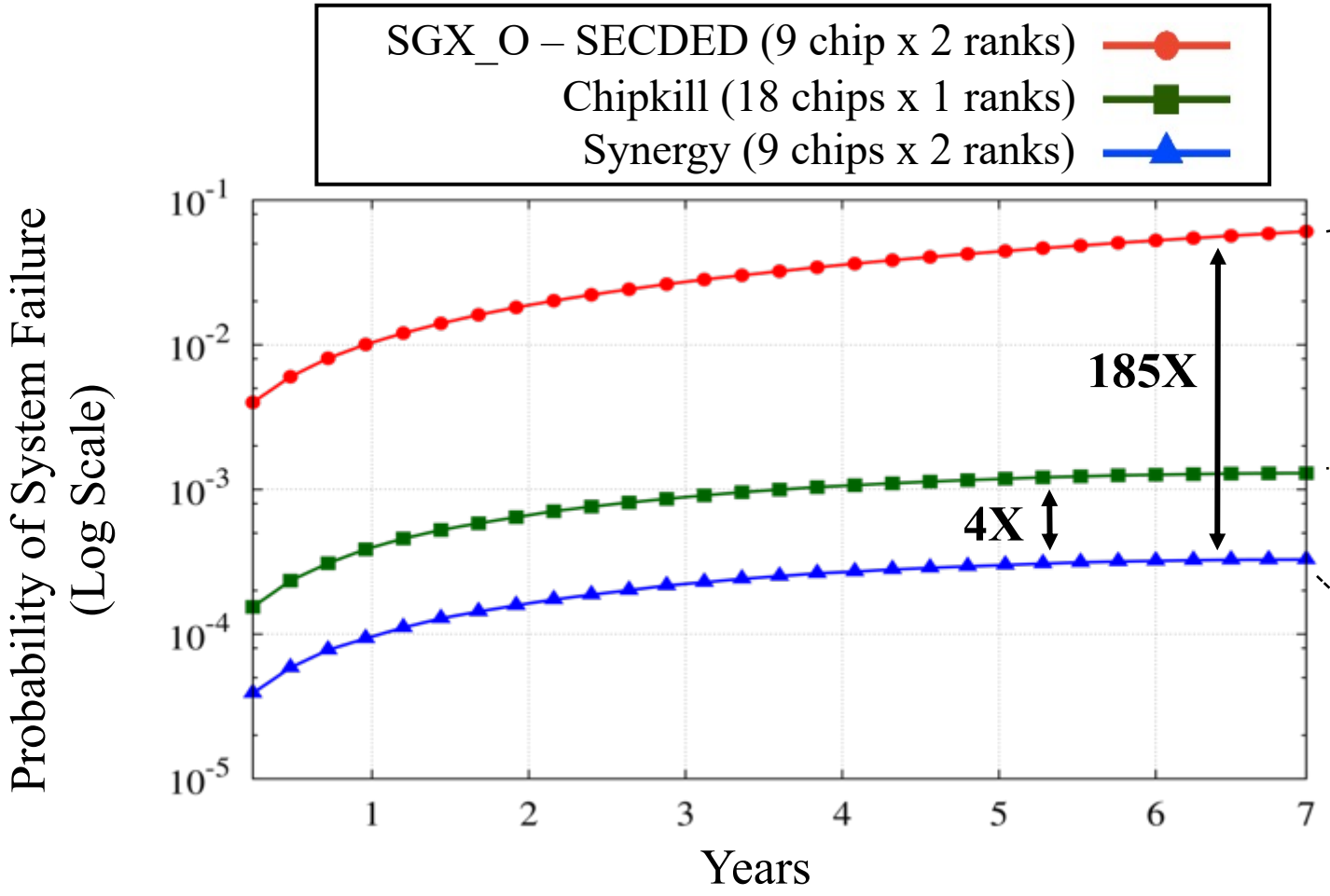
Benefit-3: Stronger Reliability



SECDED only tolerates single-bit errors

SYNERGY tolerates 1 chip failure out of 9 chips

Benefit-3: Stronger Reliability

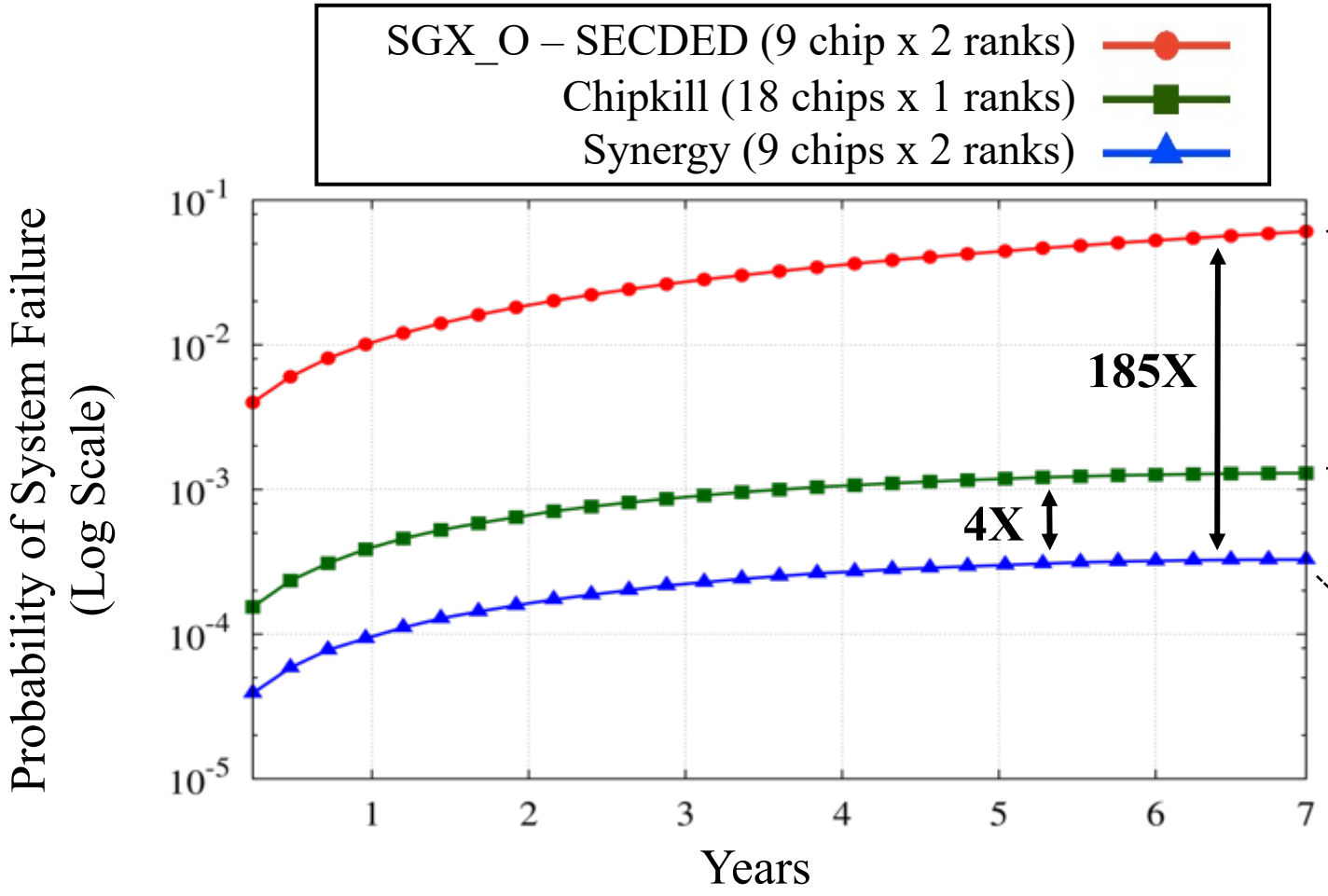


SECDED only tolerates single-bit errors

Chipkill tolerates 1 chip failure out of 18 chips

SYNERGY tolerates 1 chip failure out of 9 chips

Benefit-3: Stronger Reliability



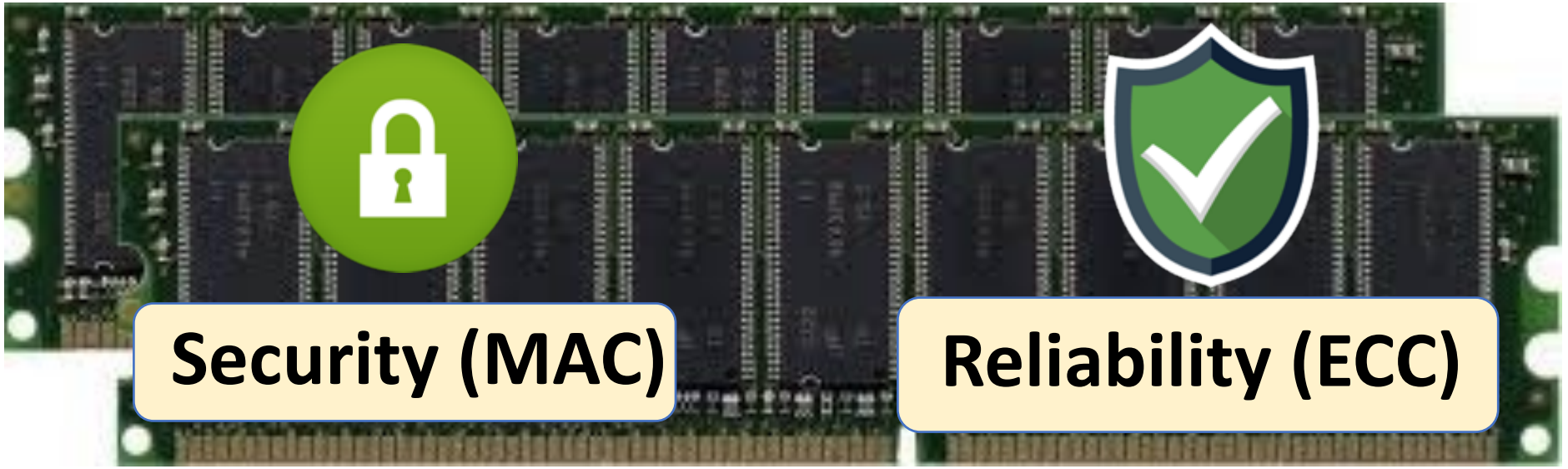
SECDED only tolerates single-bit errors

Chipkill tolerates 1 chip failure out of 18 chips

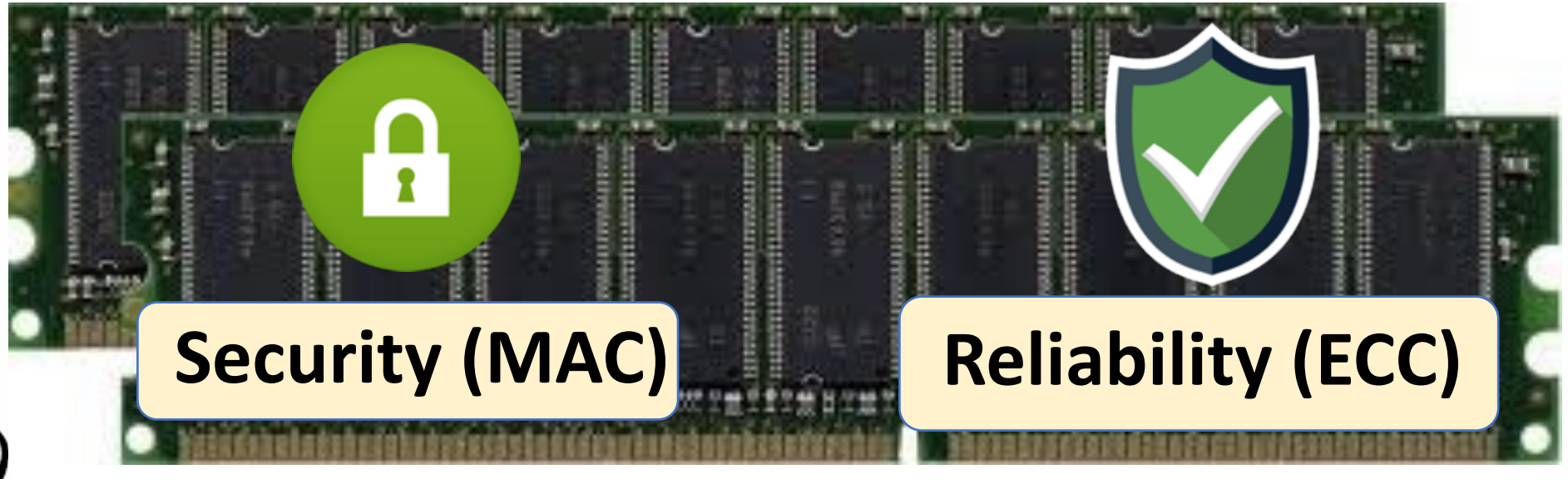
SYNERGY tolerates 1 chip failure out of 9 chips

SYNERGY has 185x higher reliability than Baseline ECC-DIMM

Conclusion



Conclusion



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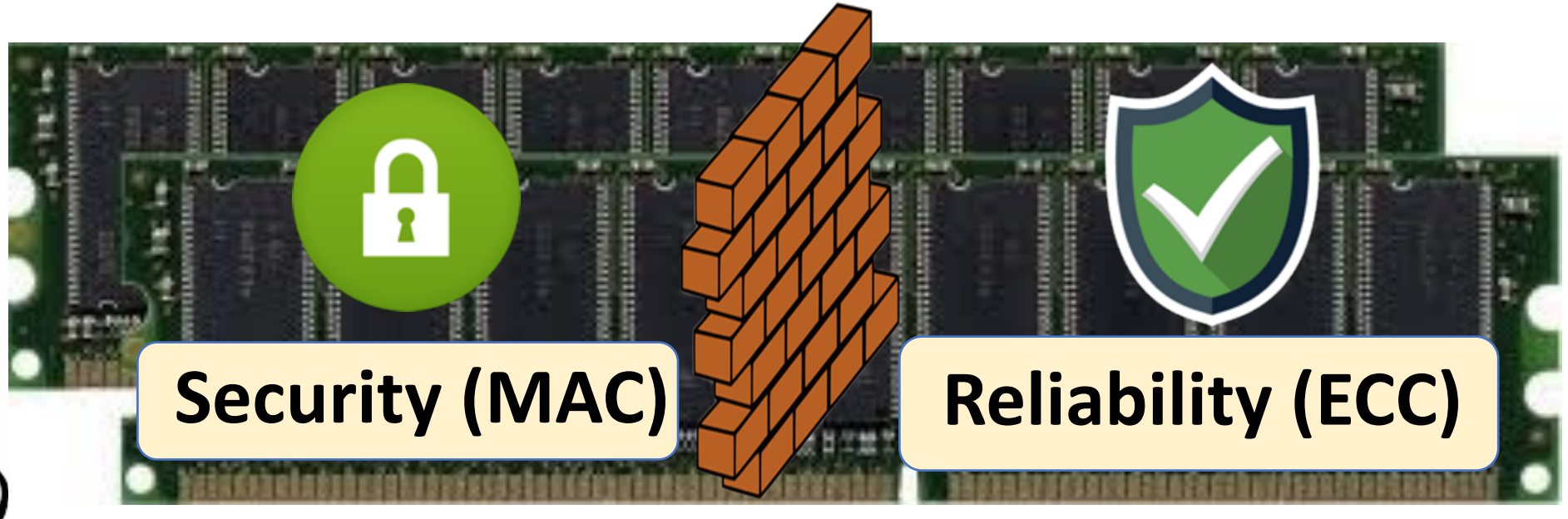
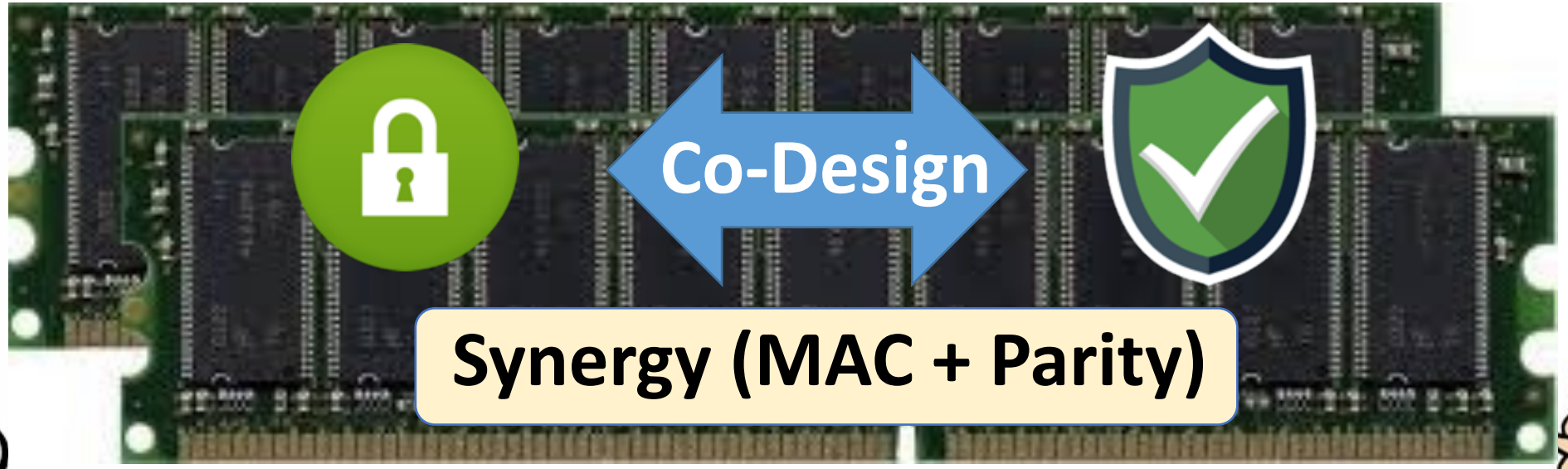
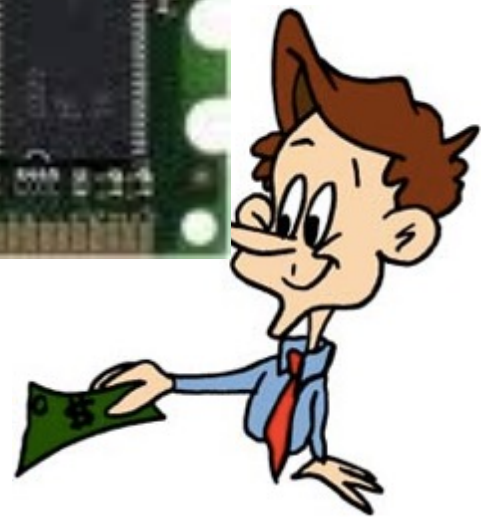
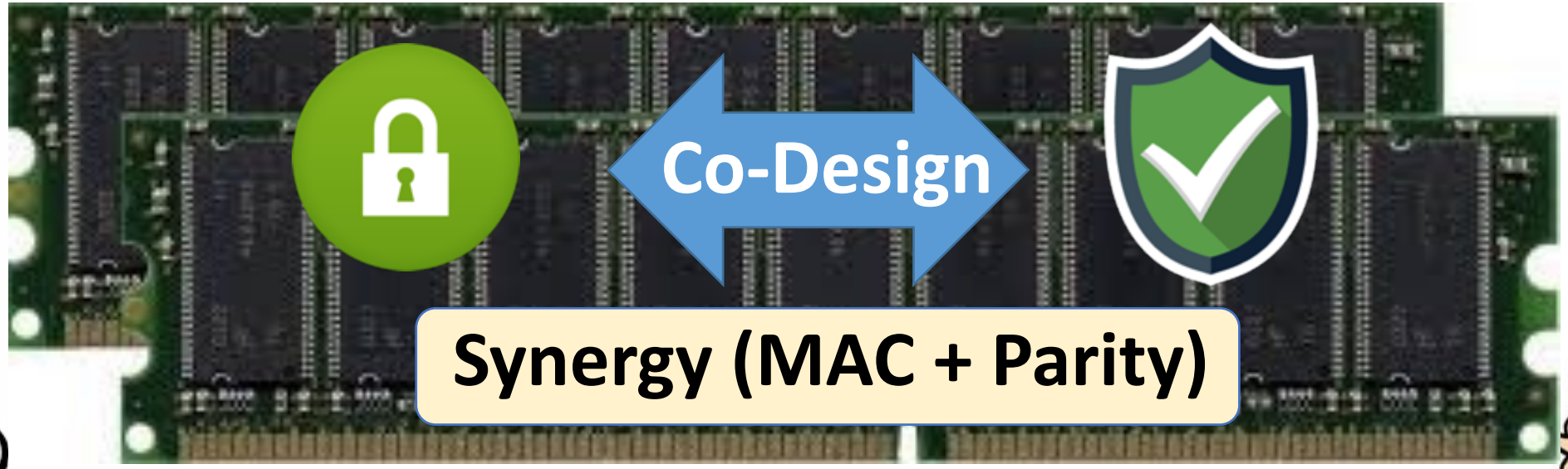


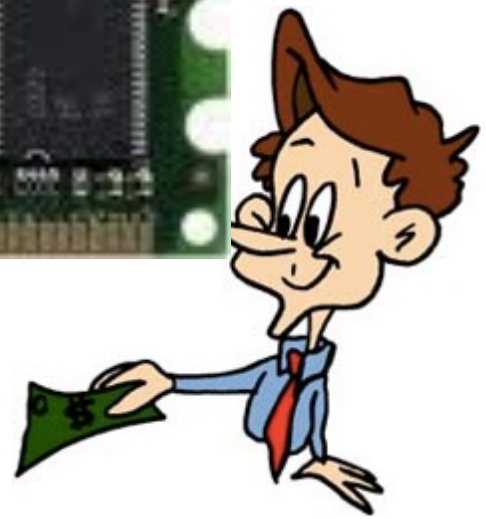
Conclusion





Conclusion





SYNERGY improves Performance by 20% and Reliability by 185x

Thanks and Questions

“The whole is greater than the sum of its parts” - *Aristotle*