Randomized Row-Swap: Mitigating Row Hammer By Breaking Spatial Correlation Between Aggressor and Victim Rows

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DRAM Scaling for Increased Capacity



DRAM Scaling for Increased Capacity More Inter-Cell Interference



DRAM Scaling for Increased Capacity More Inter-Cell Interference

DRAM (old)



DRAM Scaling for Increased Capacity More Inter-Cell Interference



DRAM Scaling for Increased Capacity More Inter-Cell Interference









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NETFLIX

DESIGNATED SURVIVOR

Mitigation in Commercial DDR4

Targeted Row Refresh (TRR) in DDR4 (2015)



Mitigation in Commercial DDR4

Targeted Row Refresh (TRR) in DDR4 (2015)

1 Track Aggressor Rows



Mitigation in Commercial DDR4



Mitigation in Commercial DDR4: Broken!



Recent Victim Focused Mitigations



Recent Victim Focused Mitigations



Arms Race in Rowhammer



Arms Race in Rowhammer



Arms Race in Rowhammer



Need New Mitigative Action Resilient to Current and Emerging Attack Patterns (preferably without requiring knowledge of DRAM mapping function)

Key Idea: Remap Aggressor Rows to Break Spatial Correlation with Victim Rows



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TRH=4800 → Minimum Activations in 64ms on Row for Rowhammer via Any Pattern (Single-sided, Double-Sided, Half-Double)

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Random

Guess?

Buckets and Balls Problem

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Buckets and Balls Problem

Continuous Remapping of Aggressor Rows Provides Principled Security for Years of Attack

Guess?

Implementation of Randomized Row Swap



Problem: The tracking structures can be overwhelmed by repeated accesses



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Conflicts in tracking structures \rightarrow targeted row addresses to be expelled \rightarrow Lose tracking of some rows

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Solution: Leverage Power of Two Choices [MIRAGE – USENIX SEC'21]



Additional Ways + Multiple Hashes + Load Balancing + Random Replacement





With 14 Demand Ways and 6 Extra Ways \rightarrow 10³⁰ installs are needed to create a conflict

Solution: Leverage Power of Two Choices [MIRAGE – USENIX SEC'21]



Additional Ways + Multiple Hashes + Load Balancing + Random Replacement

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Additional Ways + Multiple Hashes + Load Balancing + Random Replacement

RIT and HRT use the CAT to avoid collisions \rightarrow Prevents Conflict-Based Attacks

Implementation of Randomized Row Swap



Implementation of Randomized Row Swap



SRAM Storage Overheads (RIT, HRT) \rightarrow 45 KB Per DRAM Bank x 16 Banks \rightarrow 720 KB of SRAM

Performance Impact of Row Swaps

Frequency of Row Swaps Per 64ms

(1.5 microseconds per swap)





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Negligible Performance Impact

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Randomized Row Swap has negligible performance impact due to infrequent swaps

Comparison with Prior Aggressor Focused Mitigation

Blockhammer [HPCA'21]

Rate-Throttles Aggressors at Blacklist Point (Earlier Than RTH) For Entire 64ms



Comparison with Prior Aggressor Focused Mitigation

Blockhammer [HPCA'21]

Rate-Throttles Aggressors at Blacklist Point (Earlier Than RTH) For Entire 64ms



Randomized Row Swap Incurs Much Lower Worst-Case Slowdowns vs Blockhammer (mitigation is less expensive and hence adds less overheads in benign workloads)

Takeways from Randomized Row Swap



New Aggressor-Focused Mitigation – Swaps Aggressors with Random Destinations & Successively Remaps --> No Row Crosses Rowhammer Threshold

Randomized Row Swap incurs modest costs (0.4% slowdown, ~40KB SRAM/bank) while providing security against years of continuous attack

Resilient to TRResspass [SP'20], Half-Double (2021), Blacksmith [SP'22] attacks & potentially future attacks?